



# NA62 GTK

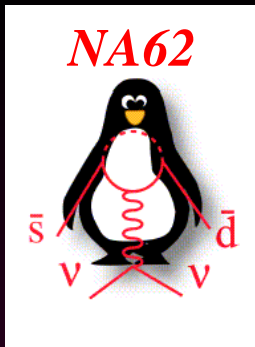


## A Silicon Pixel Readout ASIC with 100 ps time resolution for the NA62 Experiment

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G. Mazza<sup>a</sup>, A. Rivetti<sup>a</sup>, R. Wheadon<sup>a</sup>*

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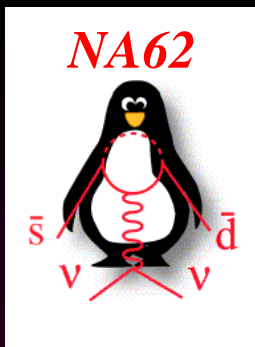
<sup>b</sup> *DFS Università di Torino, Italy*



# Outline



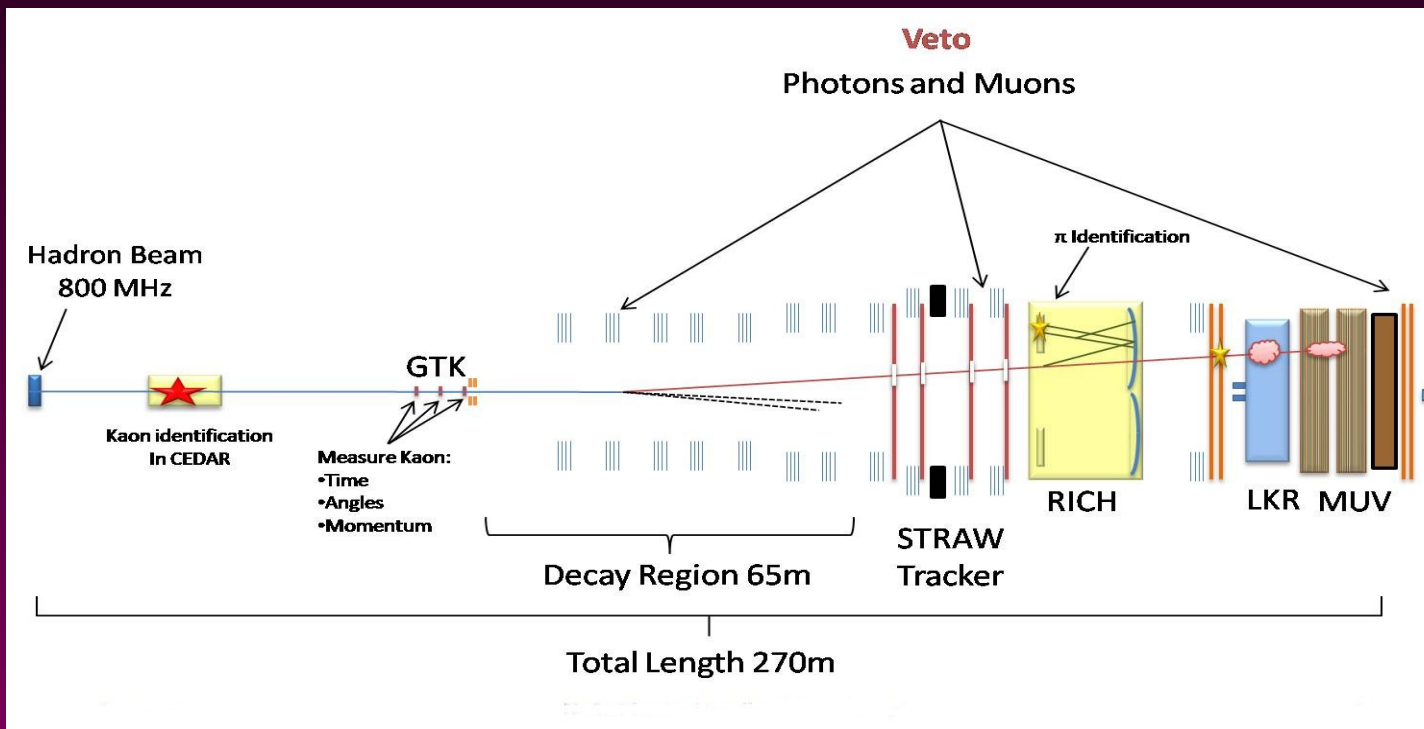
- \* The NA62 GigaTracker detector
- \* Readout requirements and architectural options
- \* On-pixel TDC option ( pTDC)
- \* Test results
- \* Conclusions



# The NA62 experiment



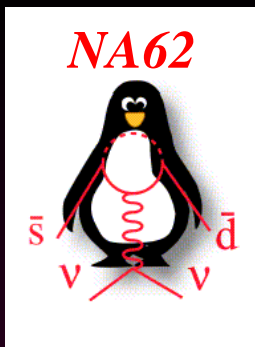
Goal : study of the rare decay  $K^+ \rightarrow \pi^+ \nu \bar{\nu}$



20%  $K^+$  decays in the vacuum region, only  $10^{-11}$  is of interest.

Only ~80 events expected in 2-3 years of data taking .

To match tracks between the GTK and the straw Tracker @  $0.8 \cdot 10^9$  particles/s, a 150 ps r.m.s. time resolution is required.



# NA62 Gigatracker

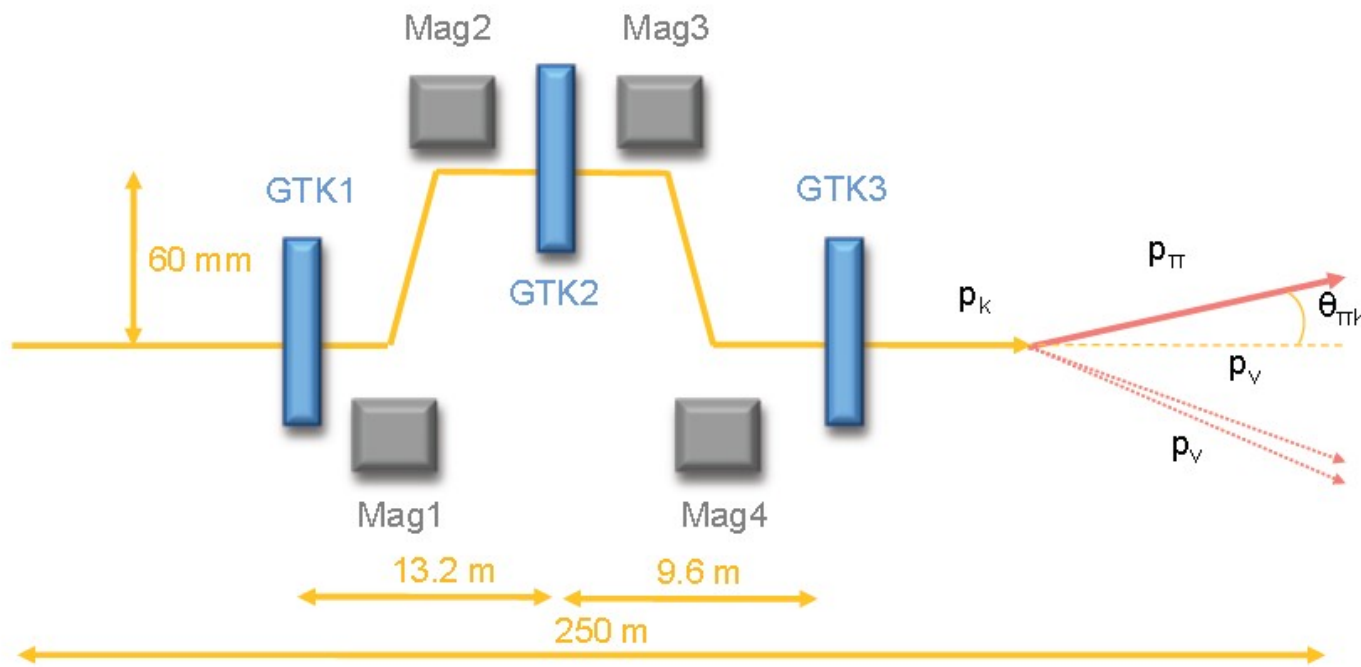


The GTK consists of 3 stations of hybrid pixel sensors operating in vacuum.

Station size : 60 mm × 27 mm

Pixel size : 300 μm × 300 μm

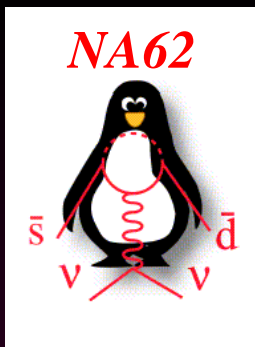
Max beam intensity (central region) :  $1.5 \cdot 10^6$  particles/(mm<sup>2</sup>·s)



Spatial resolution :  
± 150 μm

Time resolution :  
200 ps per station  
150 ps total

Material budget :  
0.5%  $X_0$



# F/E specifications



Station readout :  $2 \times 5$  F/E chips  
 F/E active area :  $12.1 \text{ mm} \times 13.5 \text{ mm}$   
 Pixel size :  $300 \mu\text{m} \times 300 \mu\text{m}$   
 Pixel matrix : 45 rows  $\times$  40 columns

Input signal :  $0.6 \div 10 \text{ fC}$

Max rate/chip :  $130 \cdot 10^6 \text{ particles/s}$

Max rate/pixel :  $140 \cdot 10^3 \text{ particles/s}$

Data rate (avg) :  $4.2 \text{ Gb/s}$

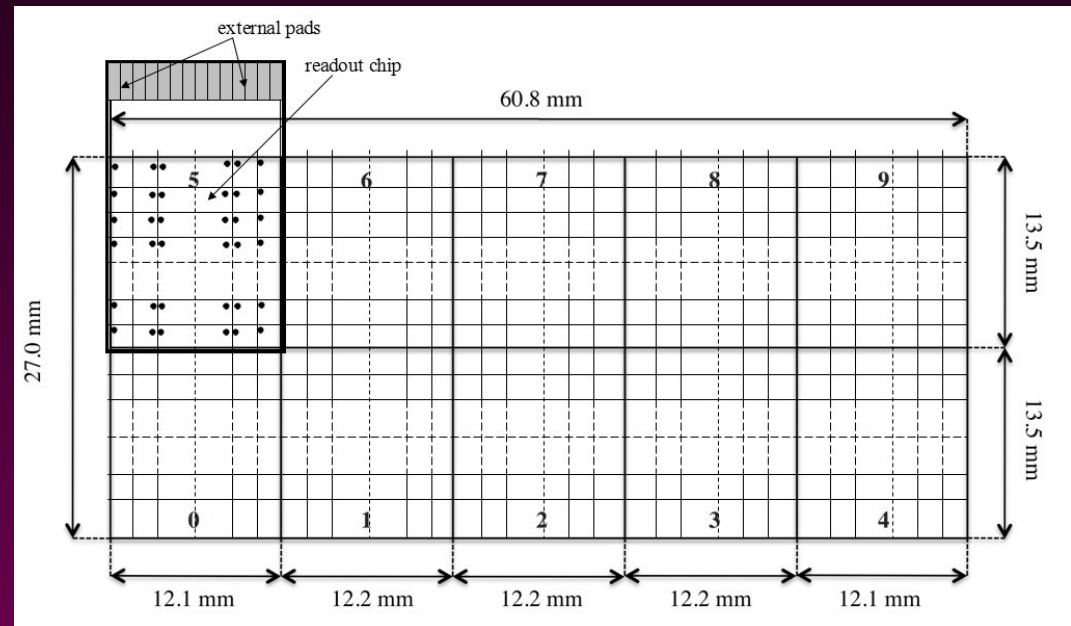
Data rate (max) :  $6 \text{ Gb/s}$

Total dose :  $10^5 \text{ Gy/year}$

Power budget :  $< 2 \text{ W/cm}^2$

Operating temperature :  $< 5 \text{ }^\circ\text{C}$

Trigger latency :  $< 1 \text{ ms}$



Main challenges for electronic R/O :

- time-walk compensation
- required n. of TDCs
- data transmission



# Readout options



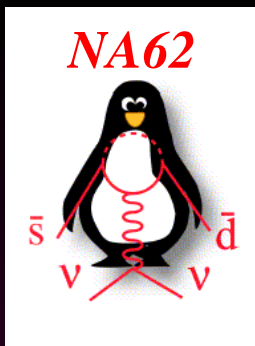
Two approaches have been investigated :

- \* pTDC :

- \* time walk compensation via CFD
- \* TAC-based on pixel TDC
  - *this presentation*

- \* EocTDC :

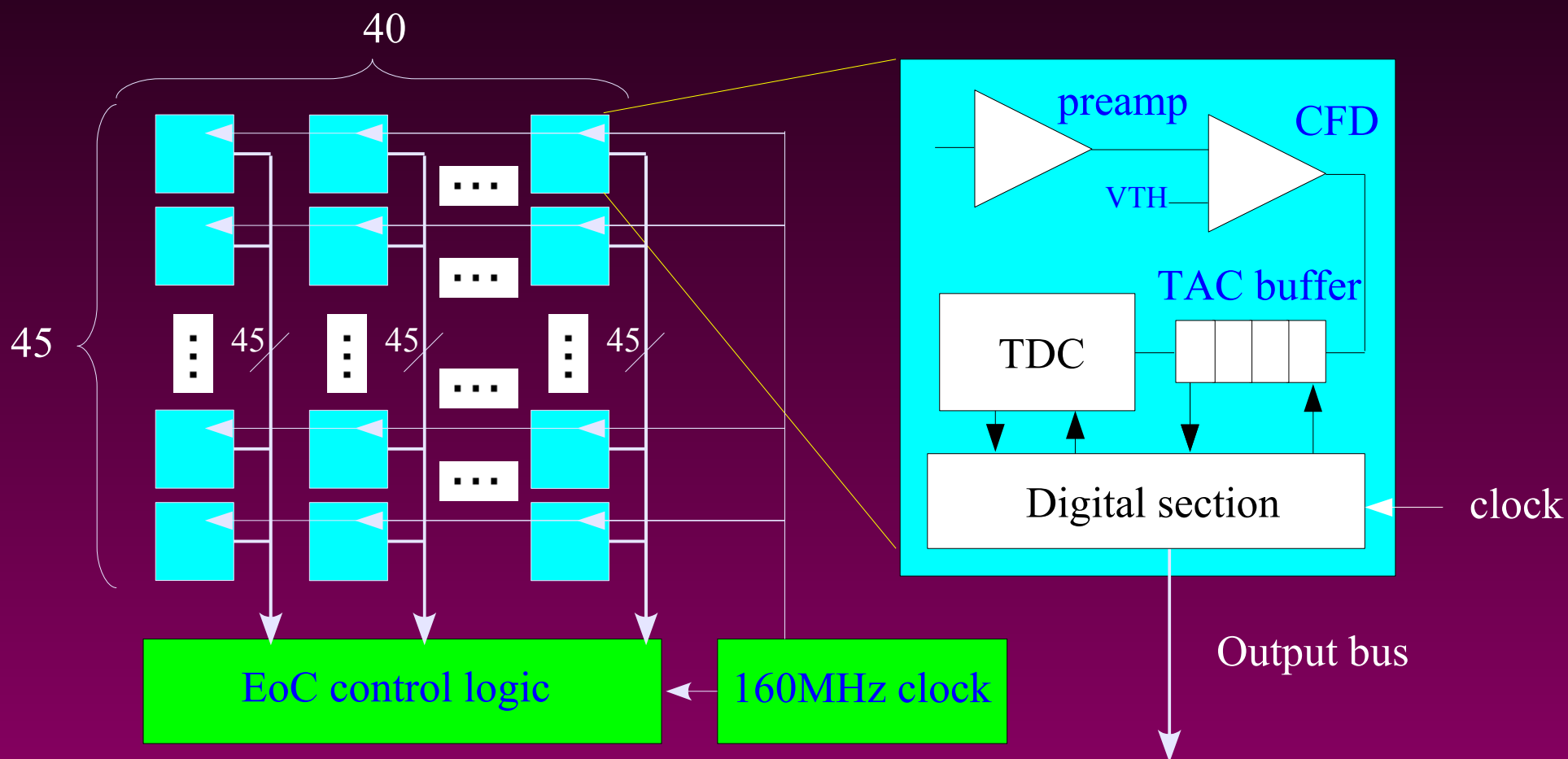
- \* time walk compensation via ToT correction
- \* DLL-based TDC at the end of the column
  - *M. Noy presentation ( later in this session )*



# pTDC architecture



Sezione di Torino



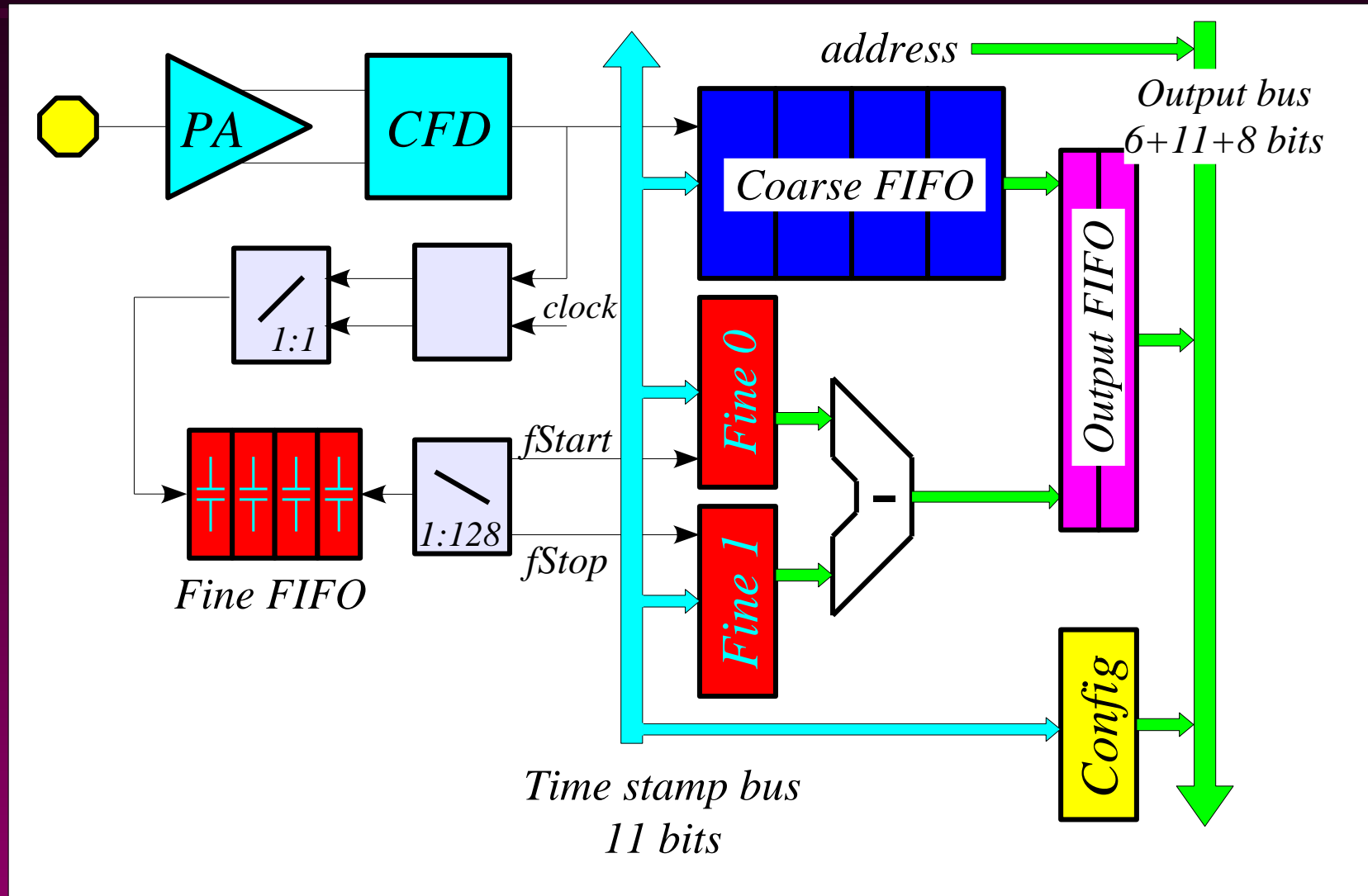
NA62



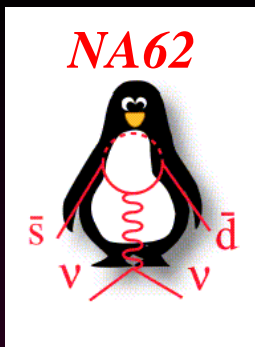
# Pixel schematic



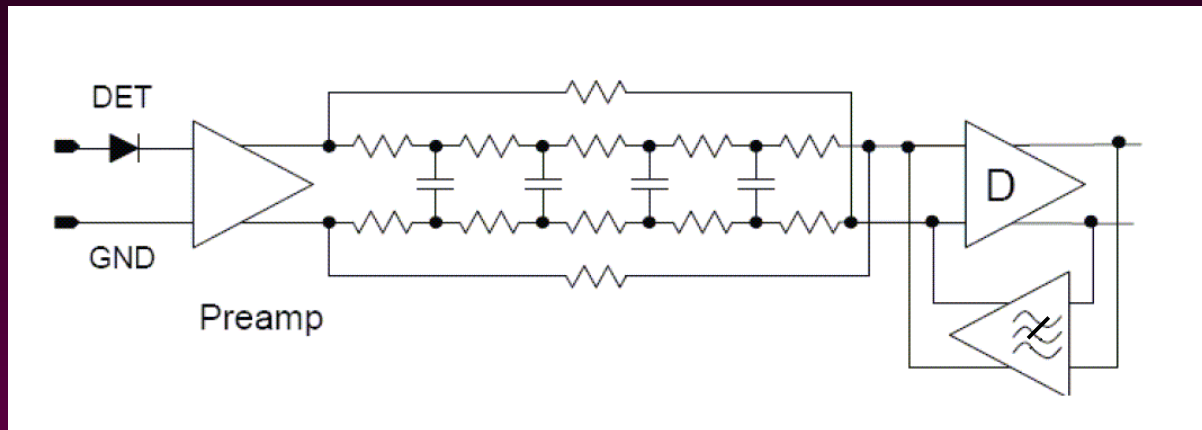
Sezione di Torino



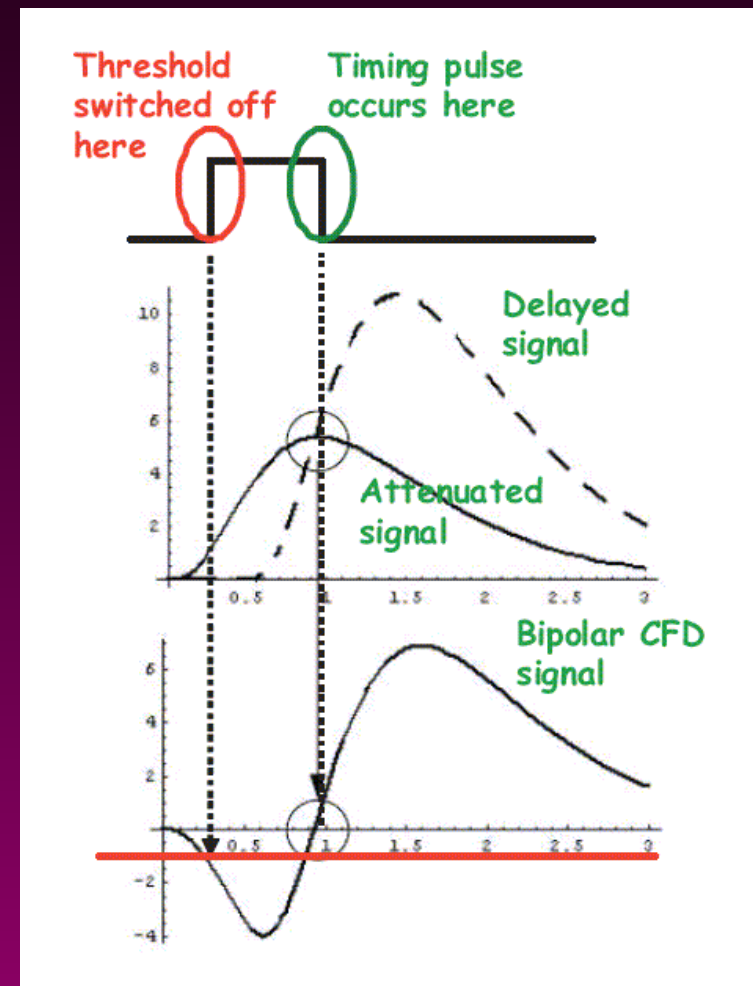




# CFD



- Fully differential implementation
- RC passive net to implement delay
- Attenuation factor : 0.3 or 0.5

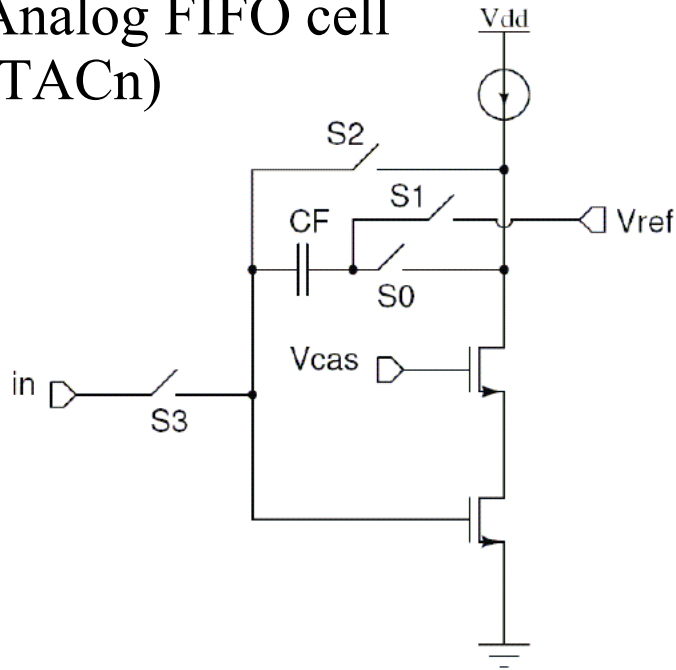




# TAC-based TDC

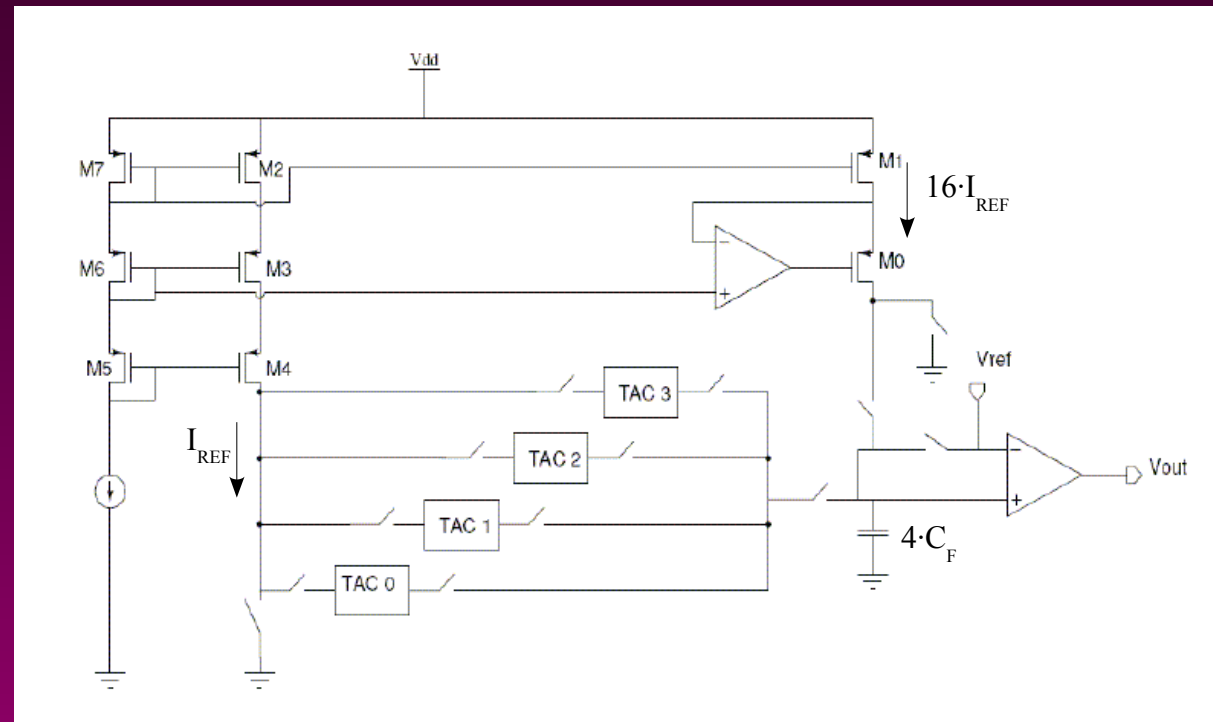


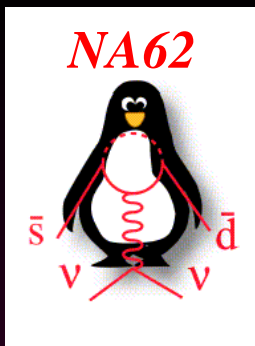
Analog FIFO cell (TACn)



$S_0, S_3$  OFF,  $S_1, S_2$  ON : reset  
 $S_0, S_3$  ON,  $S_1, S_2$  OFF : operation

	$T_{RAMP\_UP}$	$T_{RAMP\_DOWN}$	Count
MIN	6.25 ns	400 ns	64
MAX	18.75 ns	1.2 $\mu$ s	192

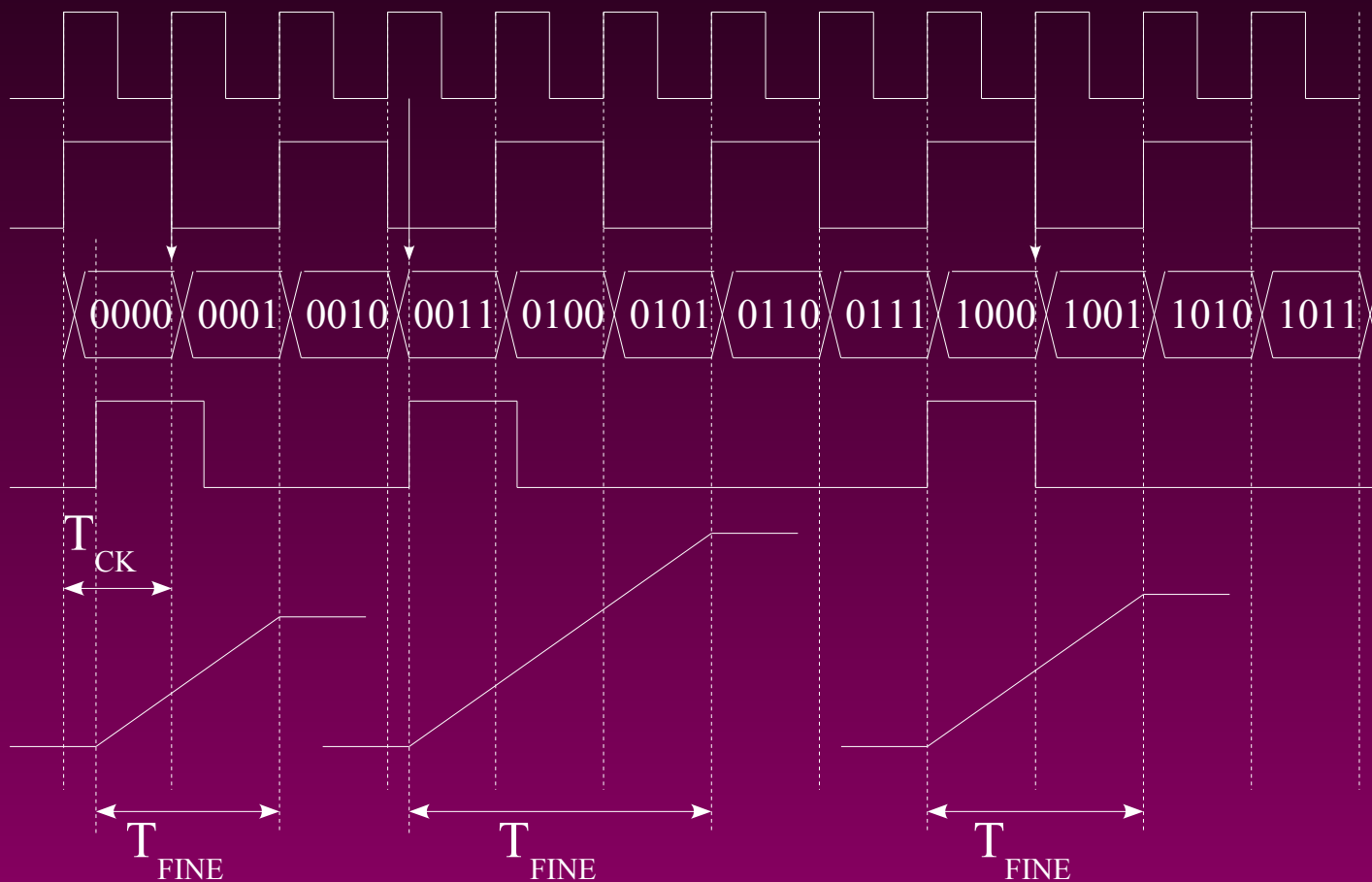


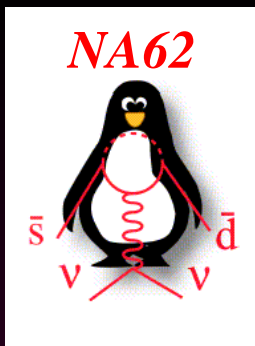


# Time measurement



Sezione di Torino

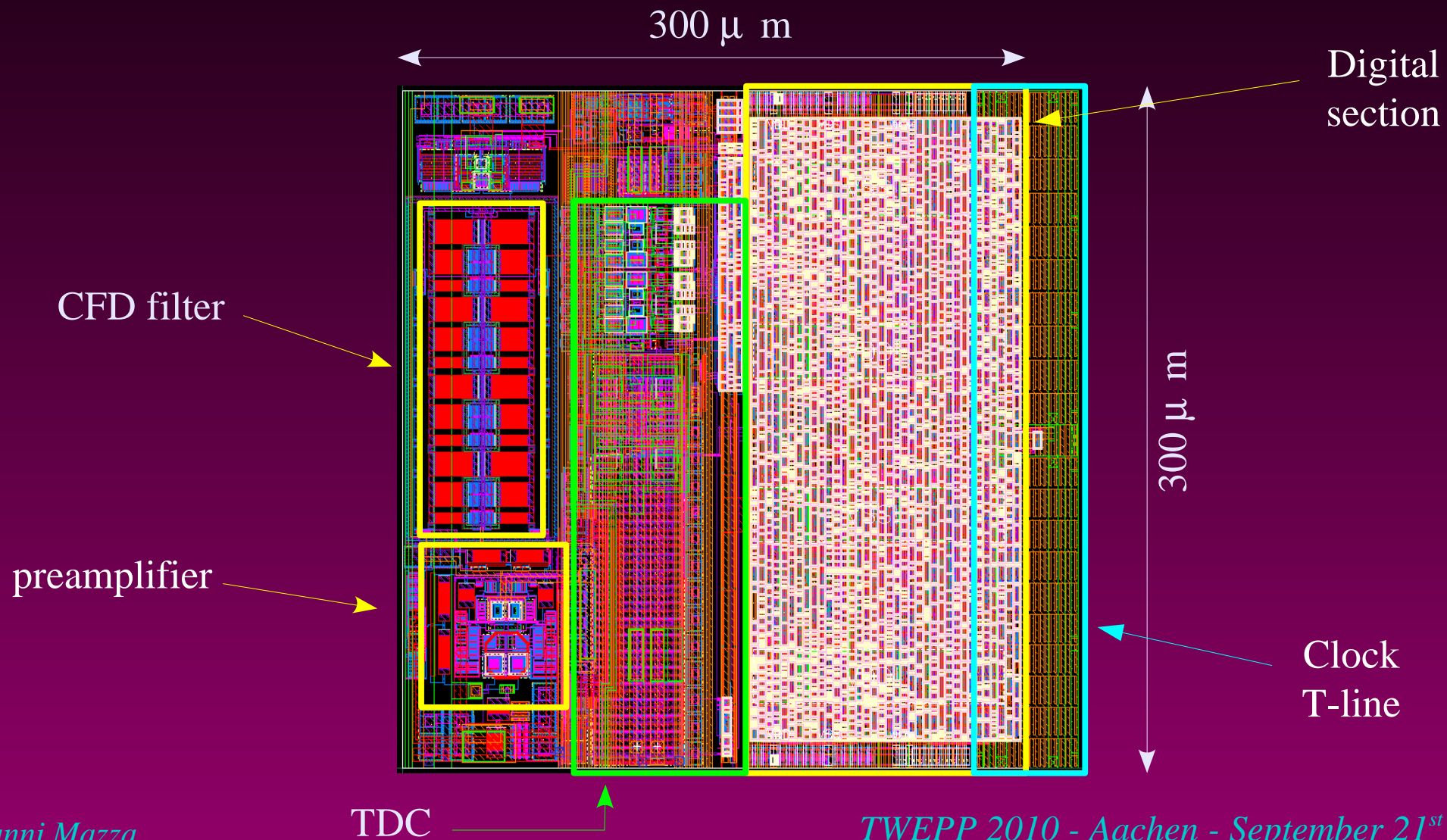




# Cell layout



Sezione di Torino



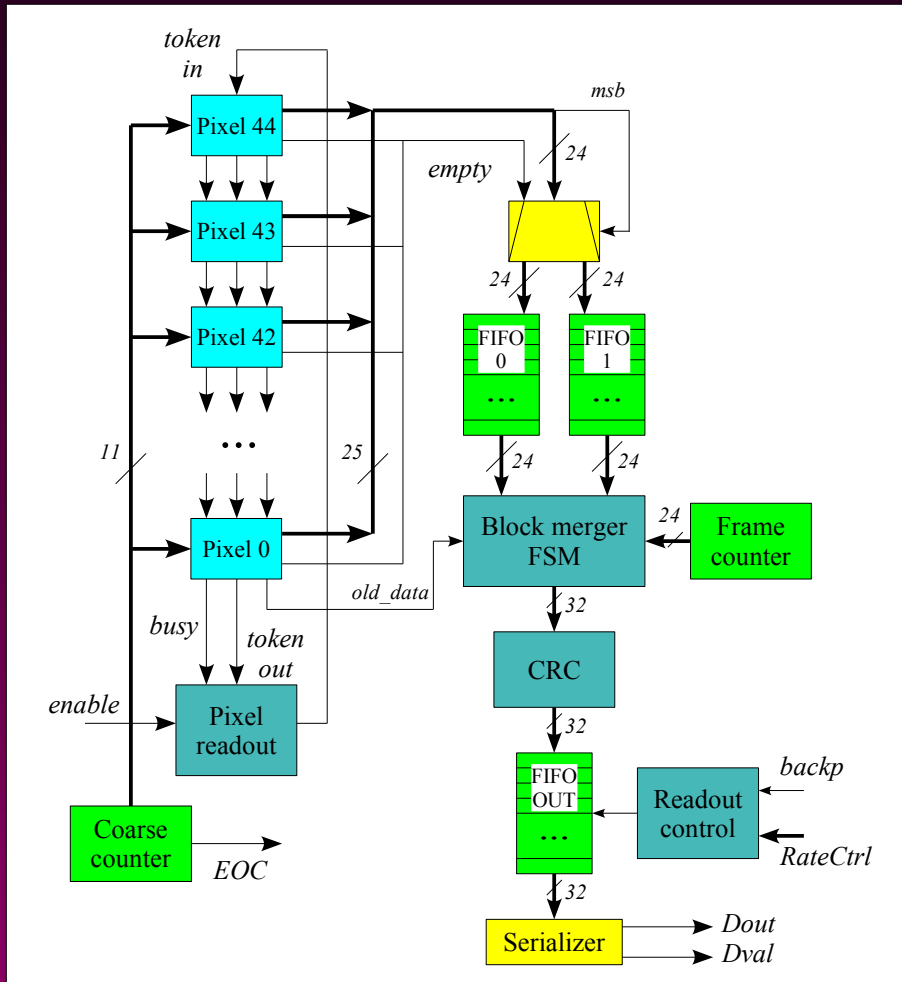
NA62



# End of column logic



Sezione di Torino



## Output packet format :



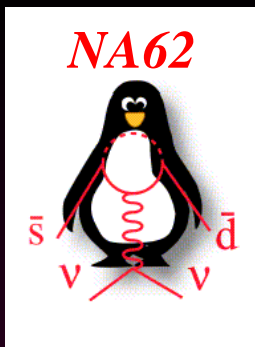
	Range	Resolution
Fine time	6.25÷18.75 ns	98 ps
Coarse time	6.4 μs	6.25 ns
Frame	107.3742 s	6.4 μs



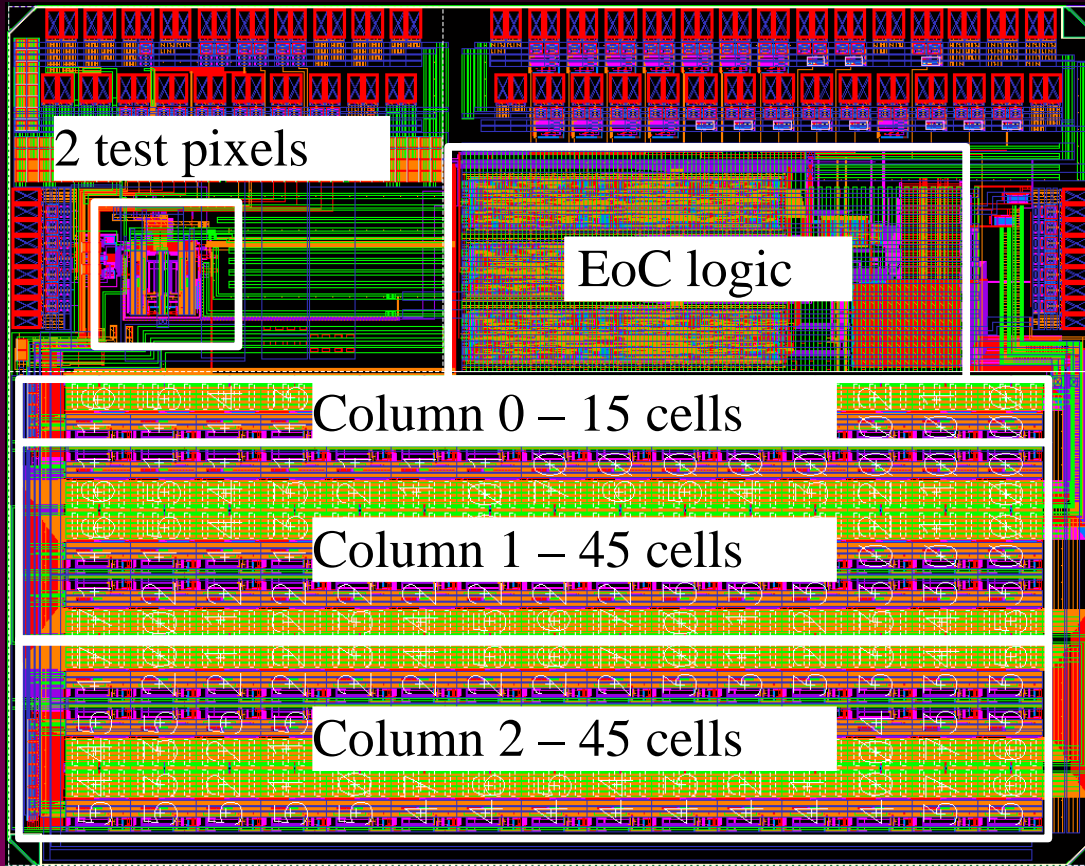
# GtkTo prototype



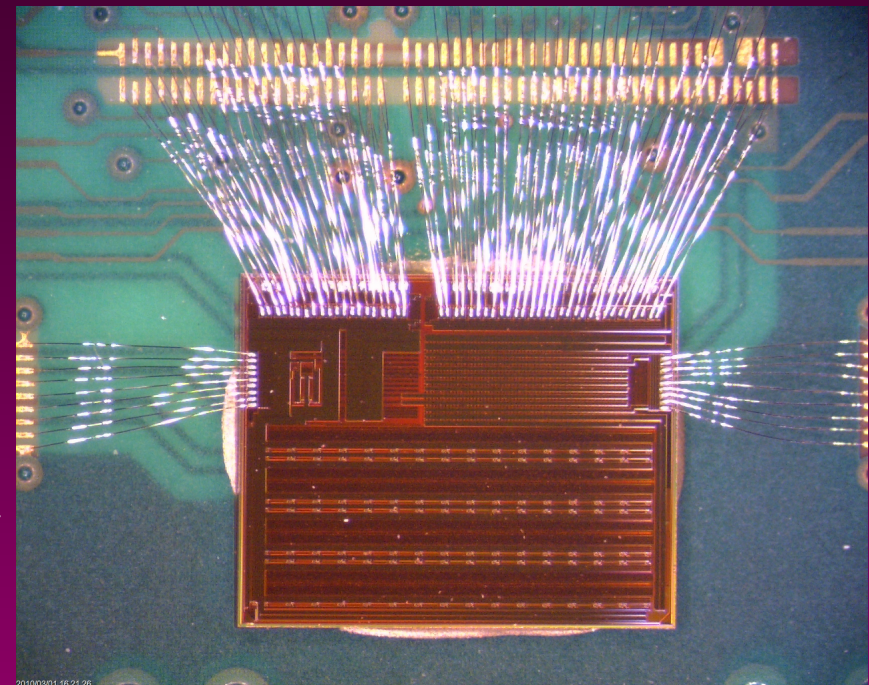
- \* Two 45-cells column + one 15 cells column
- \* Full pixel cell with bump bonding pad
- \* Full end of column buffers and readout
- \* SEU protection via Hamming encoding
- \* Technology CMOS 0.13  $\mu\text{m}$
- \* Die size 4 mm  $\times$  5 mm
- \* *High speed serializer not yet implemented*



# Prototype layout



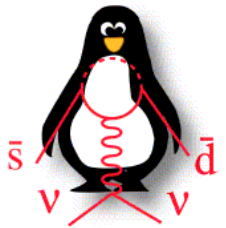
4 mm



20100301\_16 21 26

5 mm

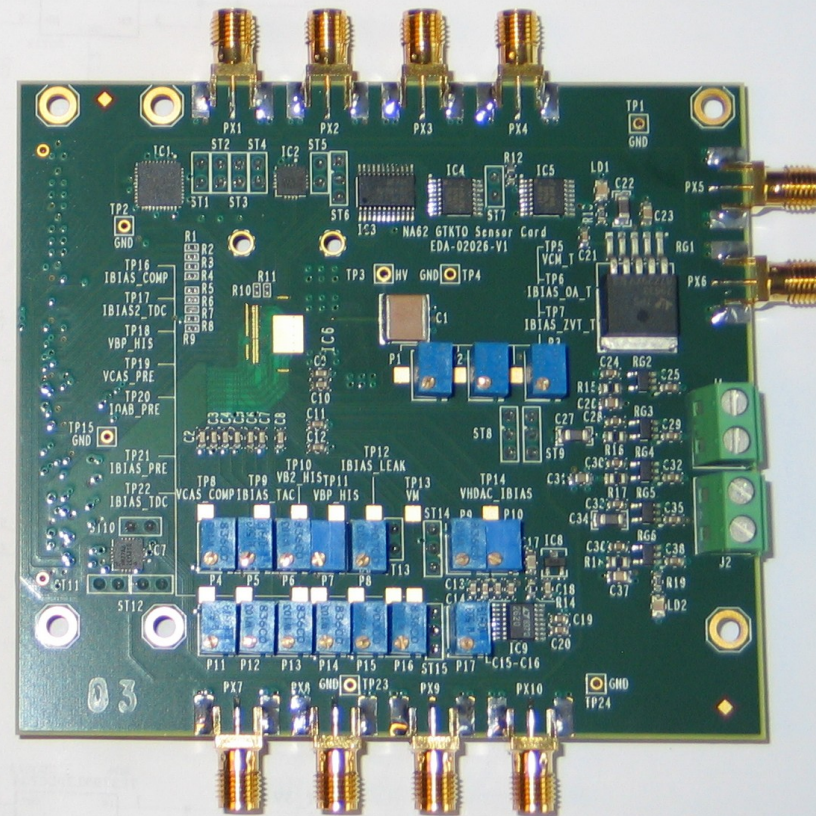
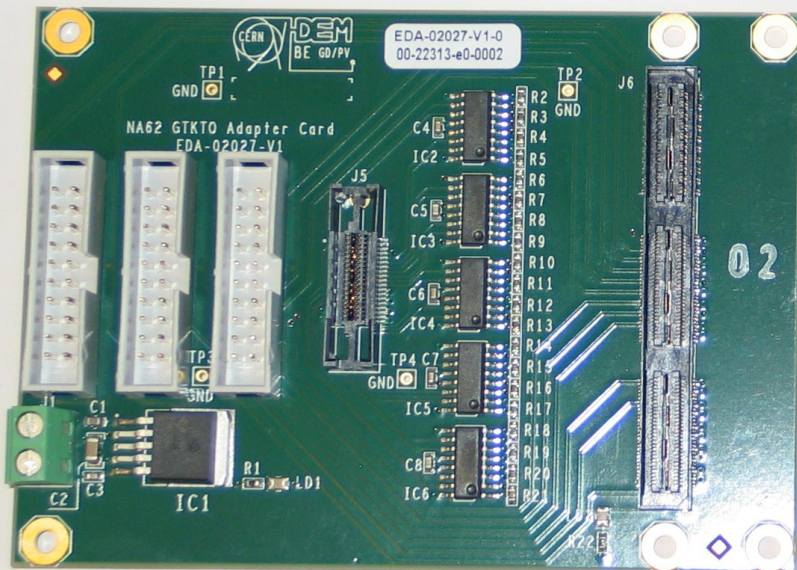
NA62



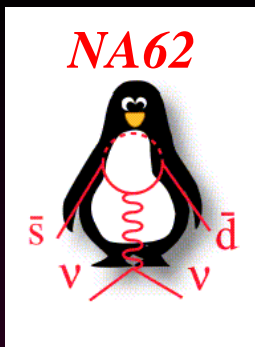
# Test boards



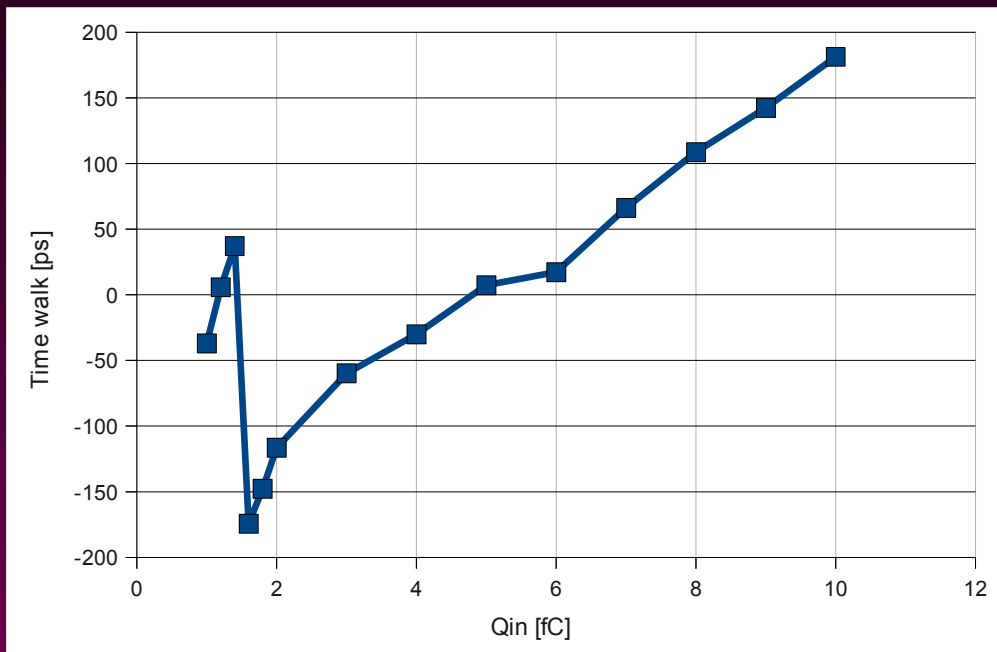
Sezione di Torino



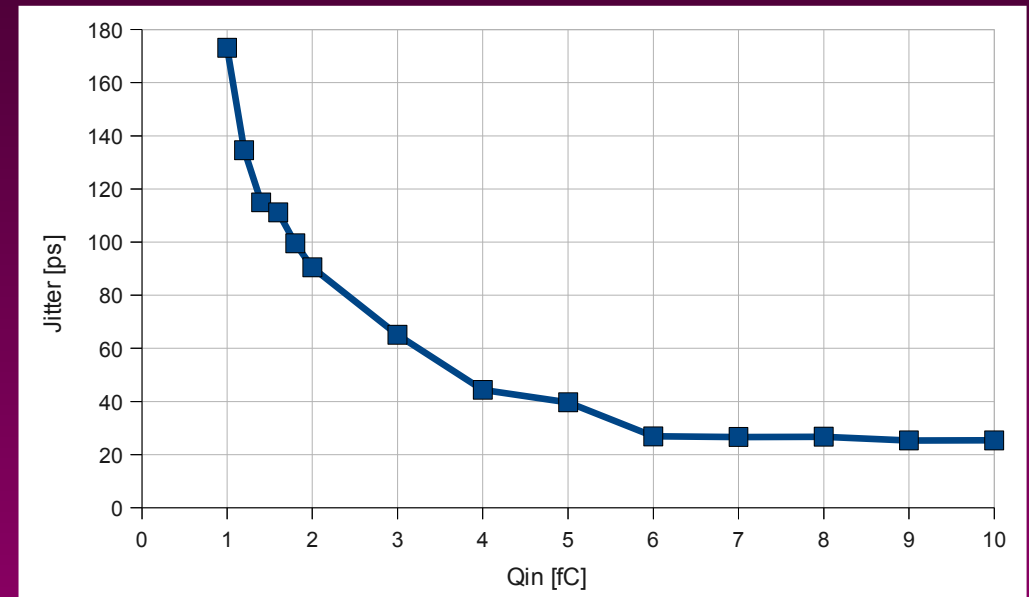


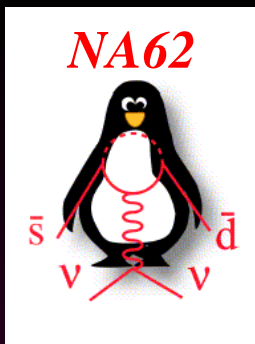


# CFD results

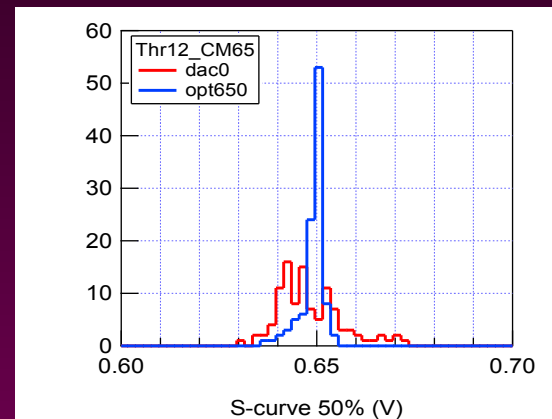
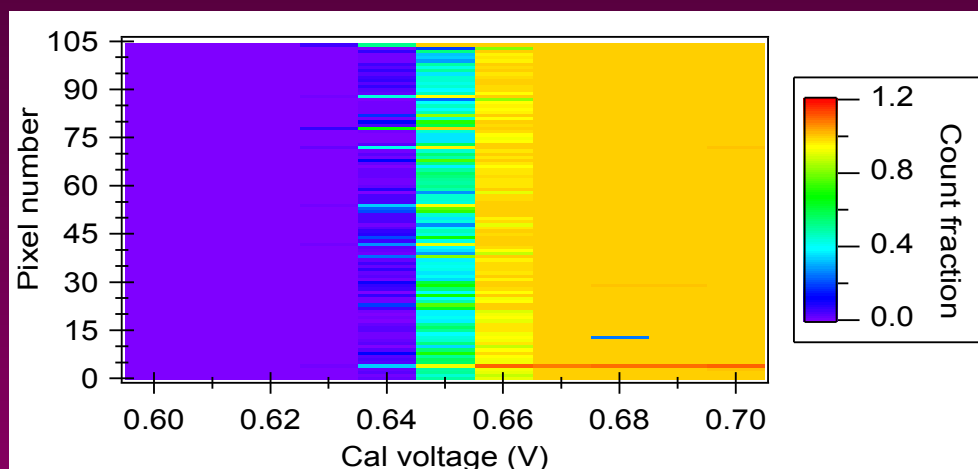
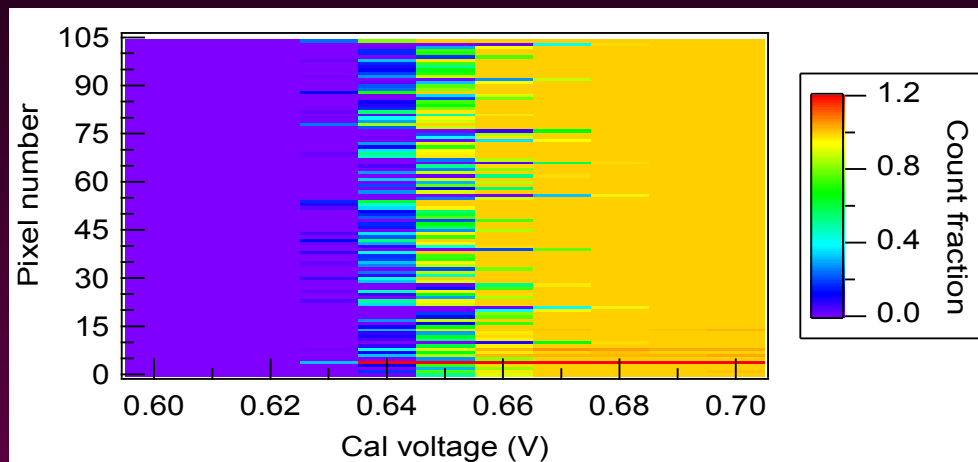


Time walk contribution (rms) : 103 ps  
 Jitter contribution : < 180 ps



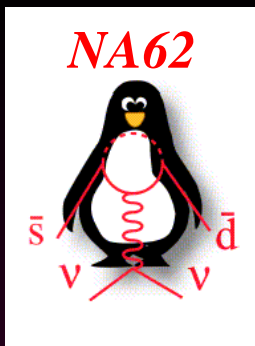


# Efficiency



Pixel efficiency before and after calibration (via on pixel DAC)

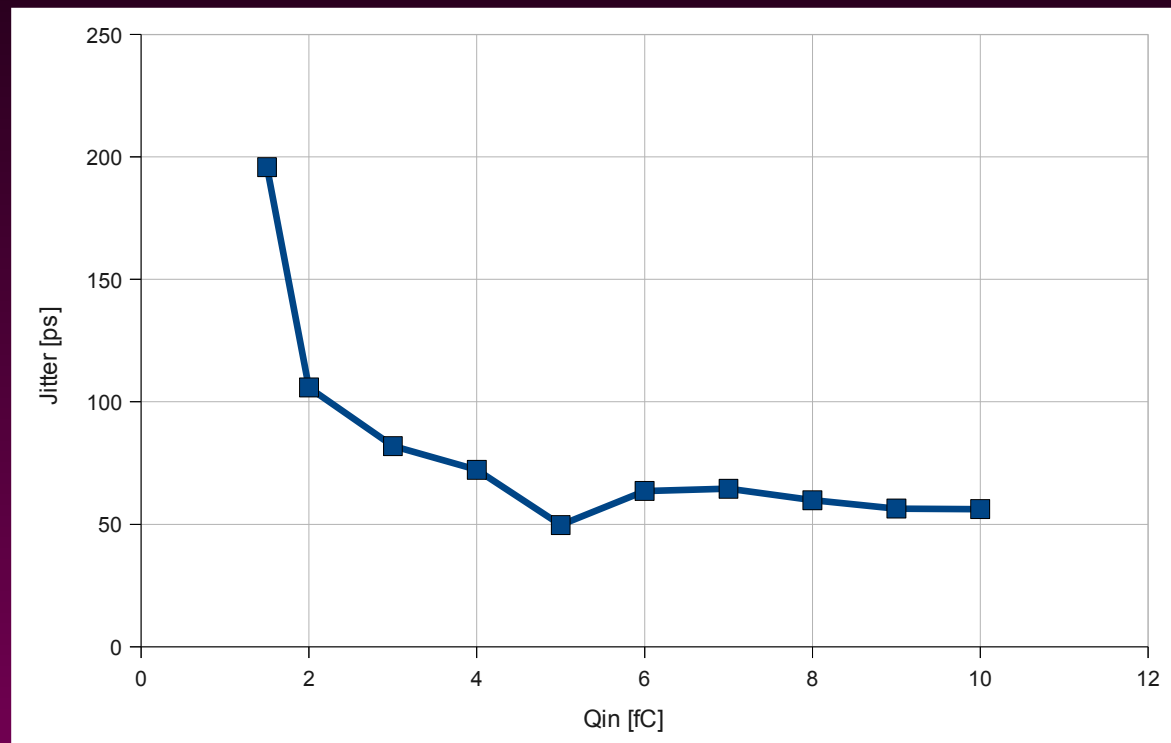
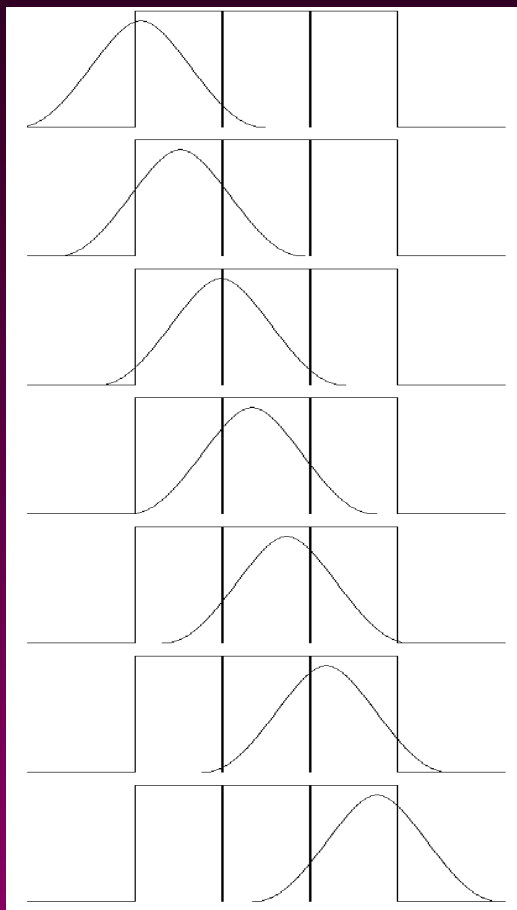
$1 \text{ fC} \approx 45 \text{ mV}$



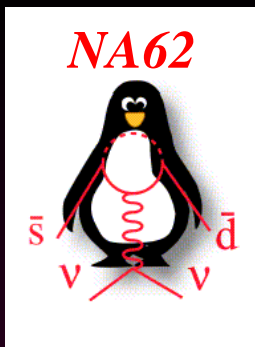
# Jitter



time bin:  $i-1$   $i$   $i+1$



Test pulse moved in steps of 20 ps  
CFD output signal counted  
Jitter : rms value of the obtained distribution



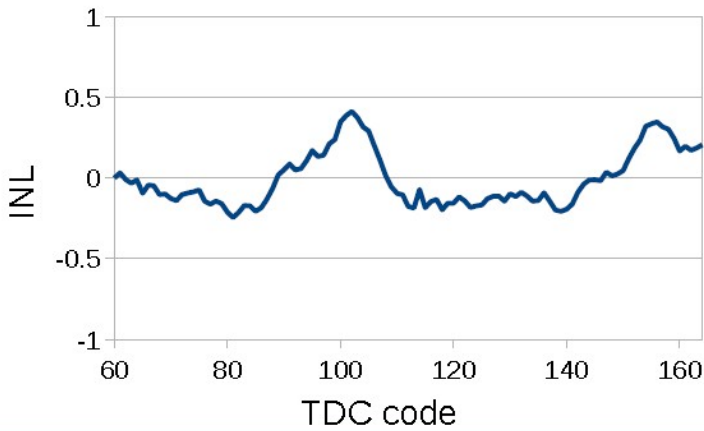
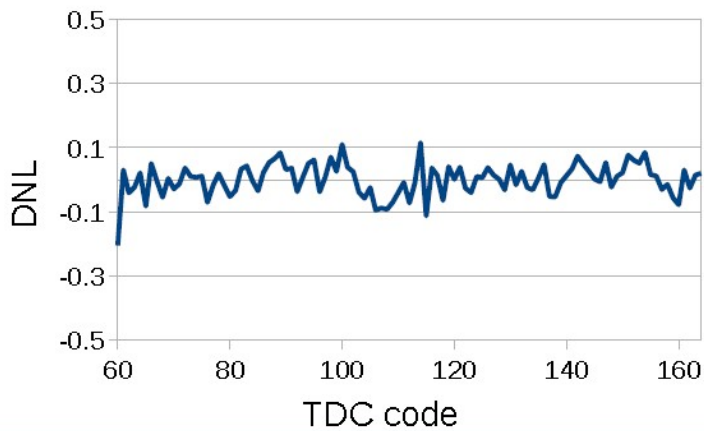
# TDC performances



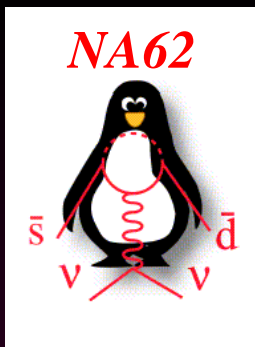
$10^5$  random test pulses

TDC range (theor.) :  
64-191

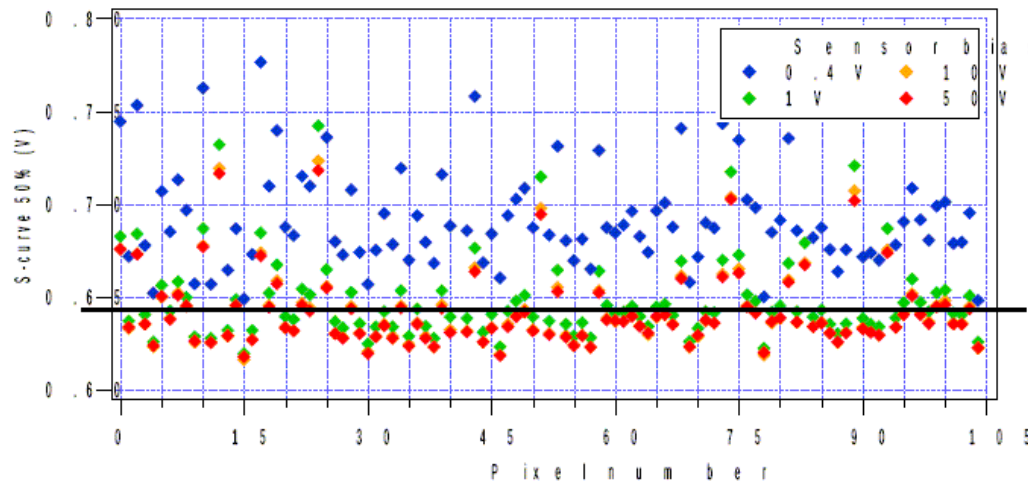
TDC range (meas.) :  
59-162



→ Gain error due to  
a systematic offset  
*to be corrected in the  
next version*



# Preliminary tests with detector

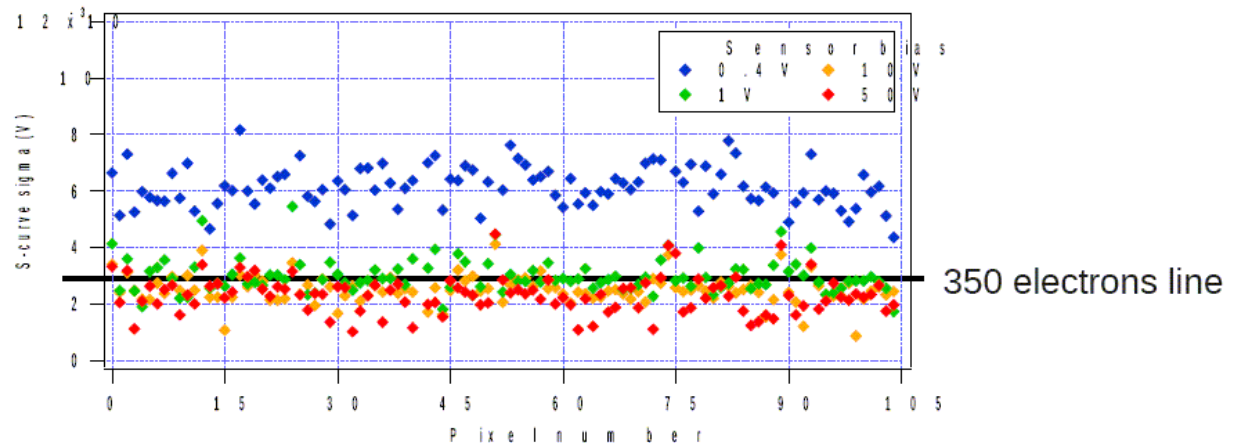


- no failure in bump bonding
- no sign of oscillations

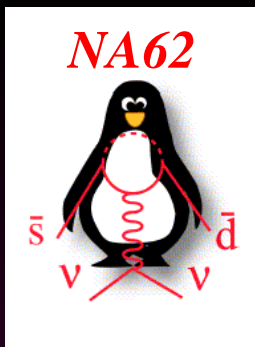
*still work in progress :*

- no threshold equalization here
- no bias equalization

- noise decreases sharply with sensor bias
- no improvement above 50 V



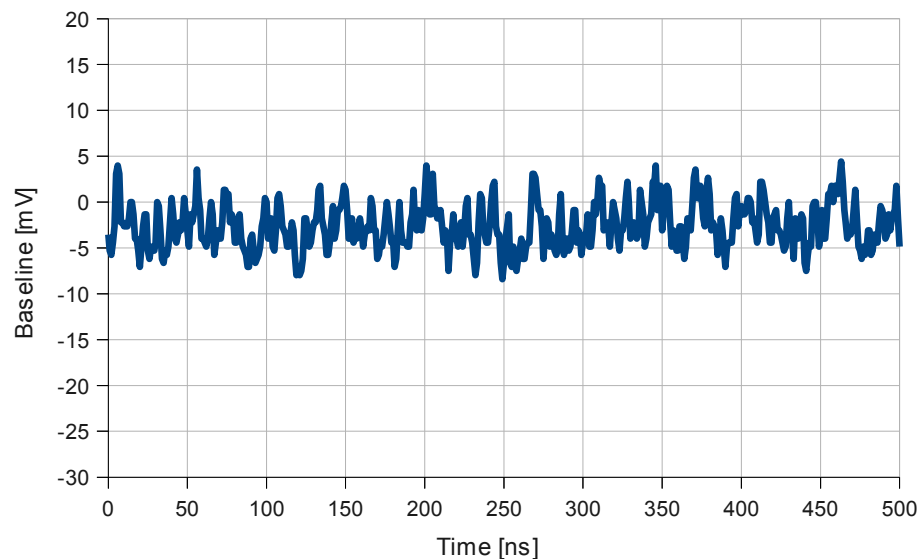
*A beam test is ongoing right now...*



# Baseline variations



Counter OFF

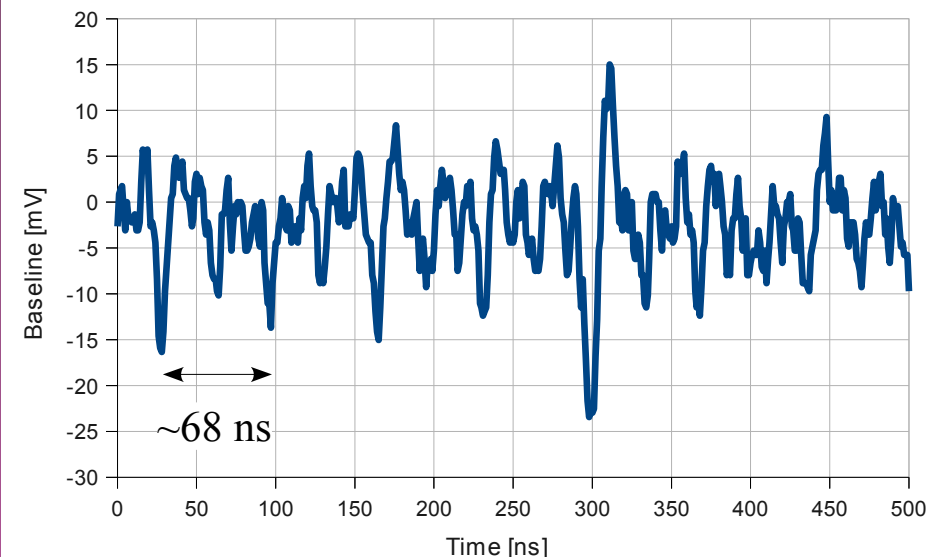


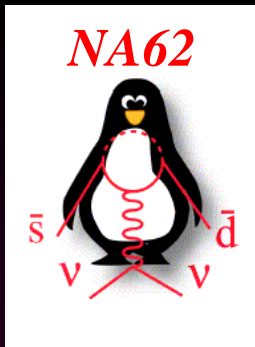
Counter OFF : baseline variation  $\sim 12$  mV (pk-pk)  
Counter ON : baseline variation  $\sim 40$  mV (pk-pk)

Digital noise substrate coupling is an issue.  
To alleviate the problem :

- separate bulk from drain in digital nMOS
- triple well nMOS for bus drivers

Counter ON





# Conclusions



- \* A SPD readout architecture with 100 ps rms time resolution based on one TDC per pixel has been proposed
- \* A reduced scale prototype in a CMOS 0.13  $\mu\text{m}$  technology has been designed and tested
- \* Overall results shows that the proposed architecture can achieve the required resolution
- \* A substrate noise problem has been identified and will be corrected in the next version
- \* Tests with detector ongoing.



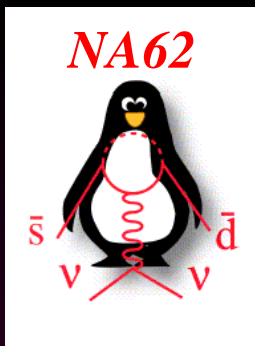
# Backup slides



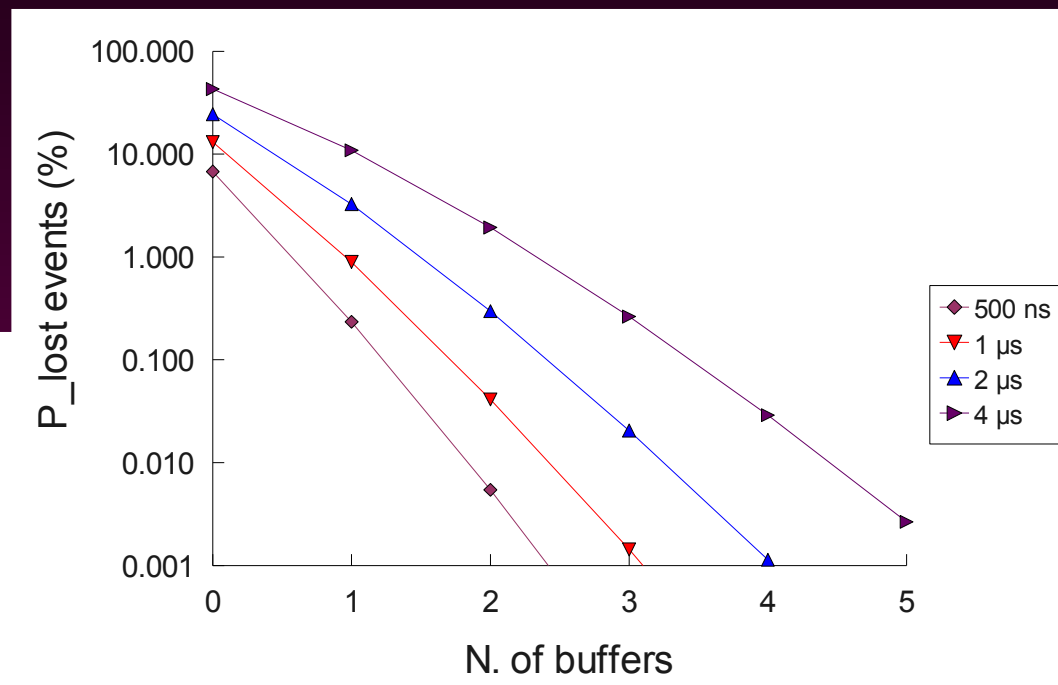
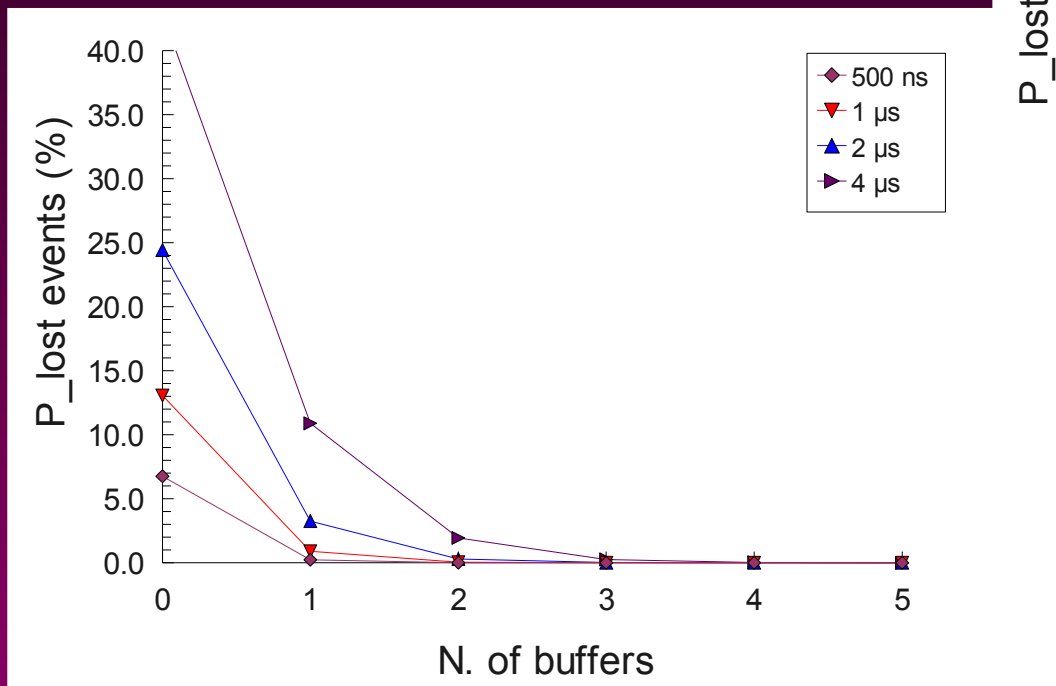
Sezione di Torino

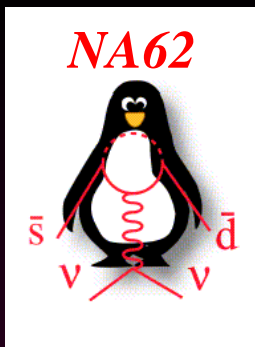
*Backup slides*





# Multi-event buffering



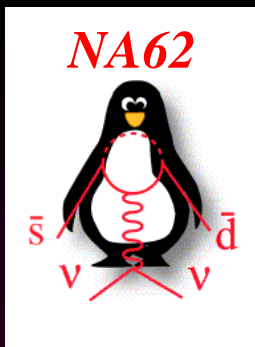


# Simulations



VHDL simulation of the architecture with  $1 \cdot 10^4$  events

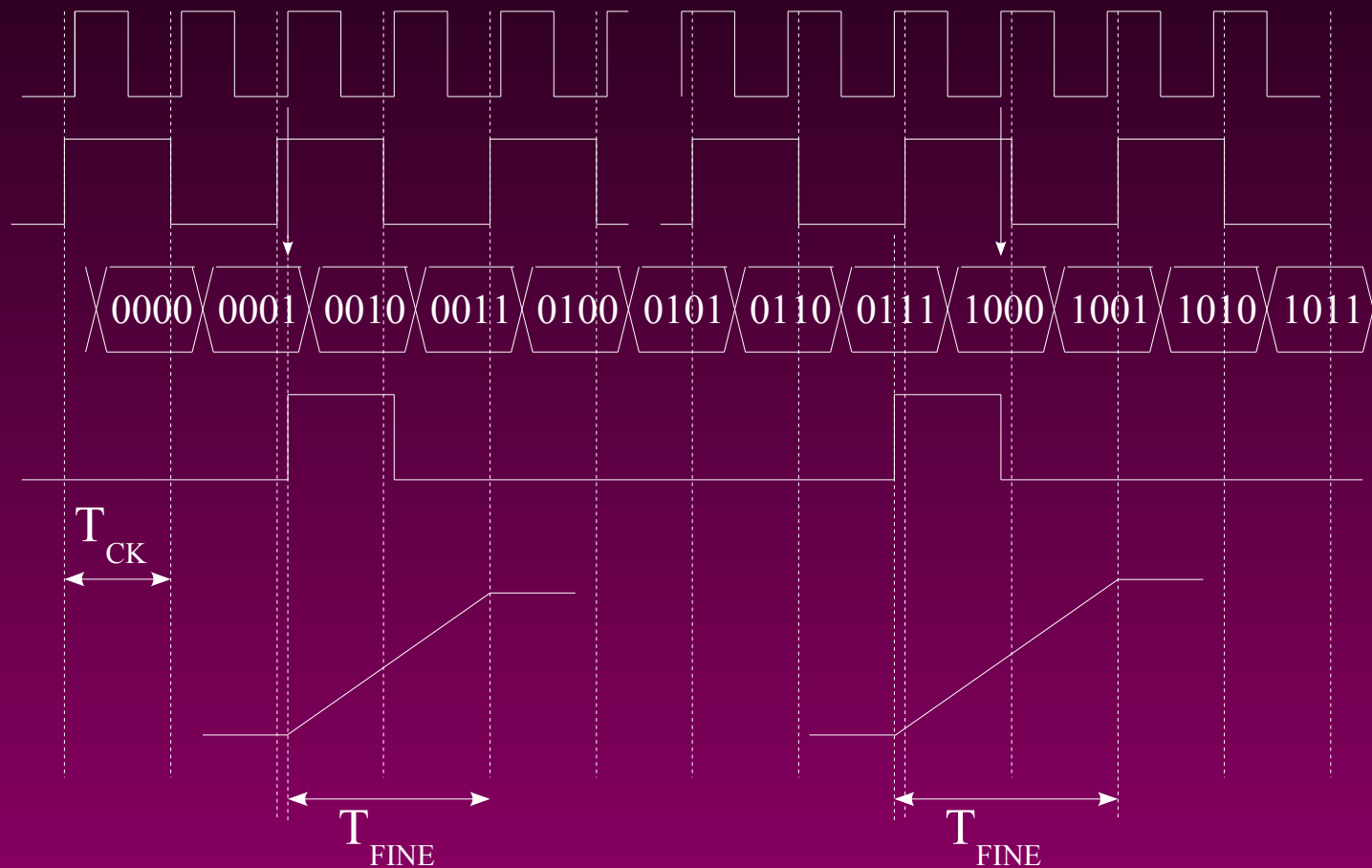
<i>Hit rate [<math>\times 10^3</math>]</i>	<i>Dead time lost events</i>	<i>Coarse FIFO lost events</i>	<i>Output FIFO lost events</i>
140	18	0	0
160	18	0	0
180	19	0	0
200	25	1	0
220	22	0	0
240	26	1	0
260	28	3	0
280	31	4	0

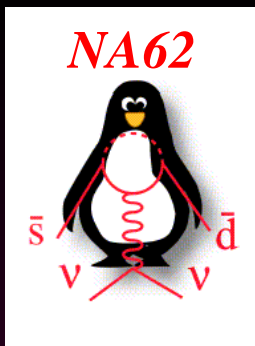


# Time correction



Sezione di Torino



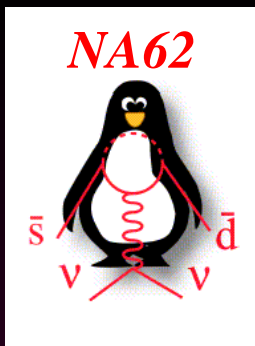


# Correction table



Sezione di Torino

<i>Coarse LSB</i>	<i>Fine MSB</i>	<i>Fine Counter</i>	<i>Time</i>
0	0	$FC < 128$	$T = T_{COARSE} + 2 \times T_{CK} - T_{FINE}$
1	1	$FC \geq 128$	$T = T_{COARSE} + 3 \times T_{CK} - T_{FINE}$
0	1	$96 \leq FC < 160$	$T = T_{COARSE} + 2 \times T_{CK} - T_{FINE}$
1	0	$96 \leq FC < 160$	$T = T_{COARSE} + 3 \times T_{CK} - T_{FINE}$
1	0	$FC < 96$	$T = T_{COARSE} + T_{CK} - T_{FINE}$
0	1	$FC \geq 160$	$T = T_{COARSE} + 4 \times T_{CK} - T_{FINE}$



# TDC uniformity



Sezione di Torino

