SEE effects in deep submicron technologies

F.Faccio, S.Bonacini

CERN-PH/ESE

SEE sensitivity of 130-90nm nodes

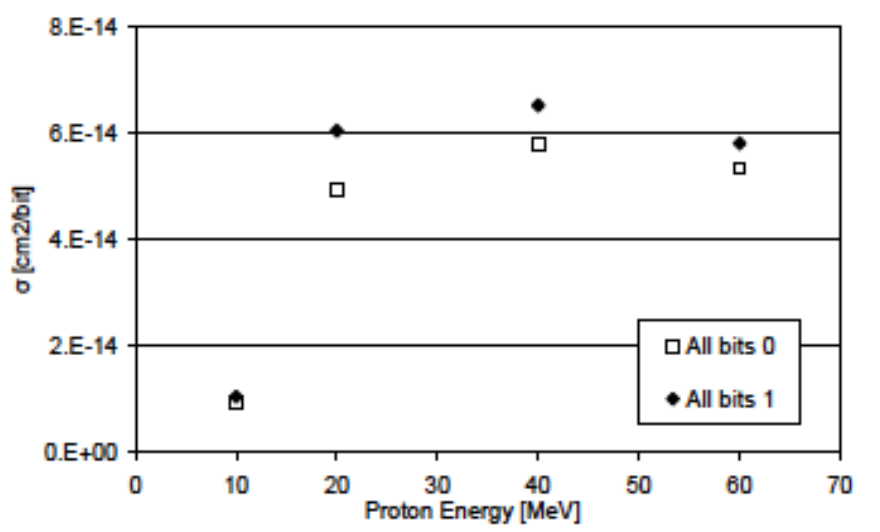
- What do we know today on the SEE sensitivity of 130-90nm nodes, and which consequences can we expect for our design methodology?
  - SEU: With the decrease of both Vdd and the node capacitance, we expect larger sensitivity to SEU in 130nm with respect to what we used to see in 250nm (where we used ELTs and guardrings!)
    - Do our data confirm that?
    - What is the influence of the applied Vdd?
    - What can we do to make our circuits ‘robust’?
  - SEL?

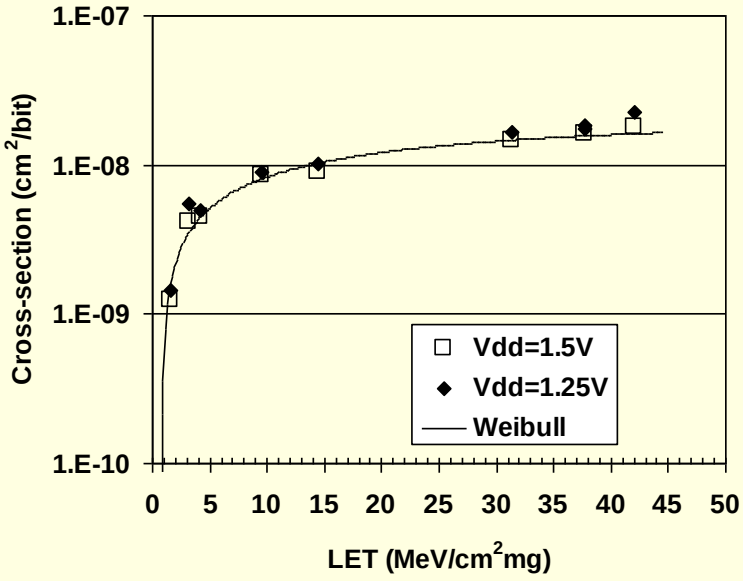
Outline

- Available SEE data on ‘standard’ cells in 130nm, and comparison with the 0.25um used for LHC
  - SRAM and Flip-Flop
- Extrapolation of an error rate in LHC-SLHC
  - Can we live with this rate?
- Cells/strategies to protect registers against SEU
- Are we safe against SEL?
- Work in progress in PH-ESE

Available radiation data for “standard” SRAM

- SRAM cells designed in 130nm either by the Foundry or custom using a SRAM generator from a commercial provider



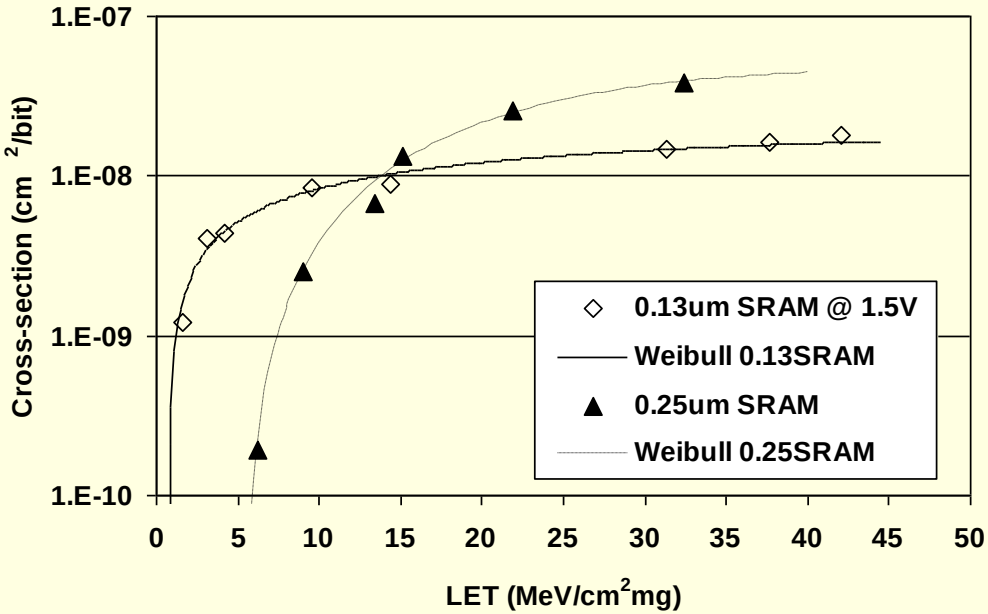


Irradiation done by CERN at PSI (CH) in 2002/2003 on Foundry-provided 16k x16 SRAM samples. Vdd=1.5V.
Sigma increases by 20-30% when decreasing Vdd to 1.26V

Irradiation done by CERN at LNL (It) in 2005 on custom samples designed with commercial SRAM generator (size of the memory: 16kbytes). Effect of bias irrelevant in the explored range (1.5-1.25).

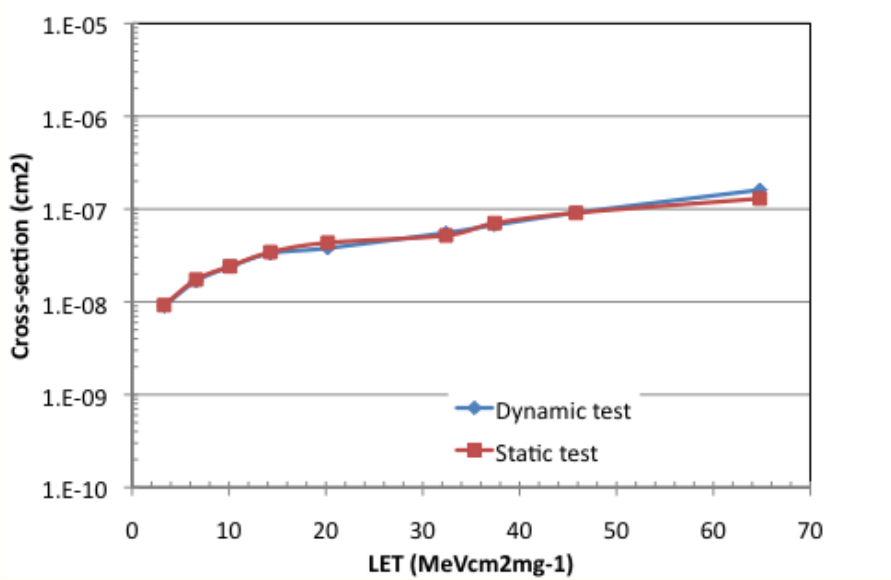
Comparison with 250nm memory

- Comparison with 0.25μm memory (rad-tol design typically used in LHC designs!!):
  - Cross-section of the commercial 130nm design 15-30 times larger in LHC environment



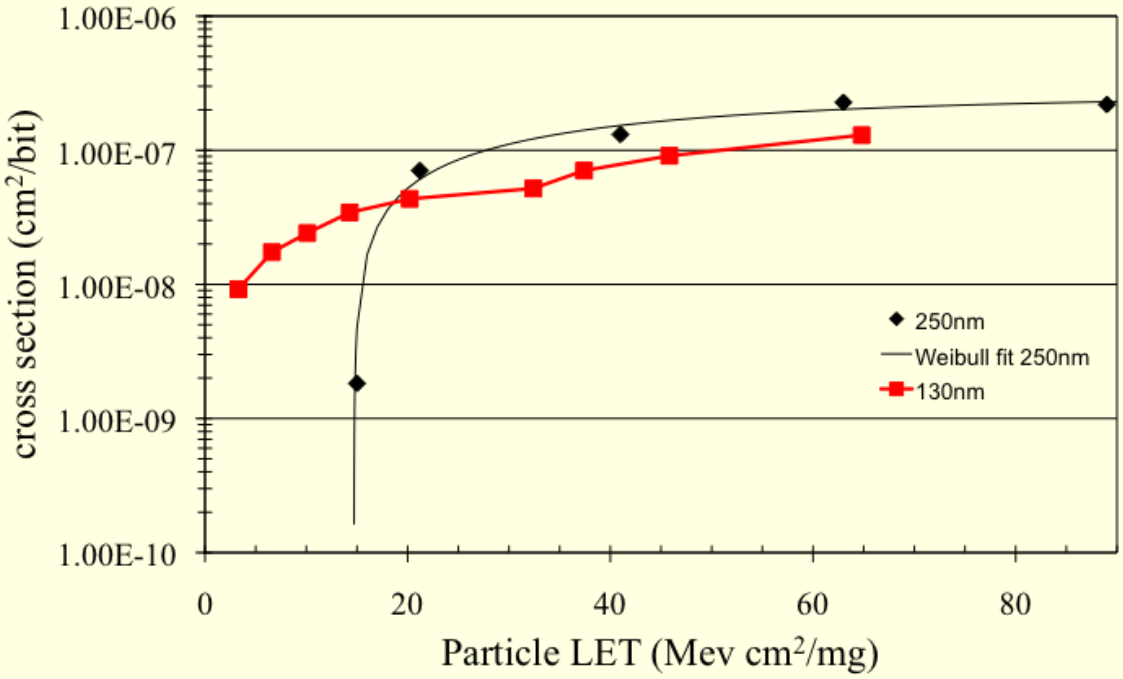
Available radiation data for “standard” FF cells

- Standard FF in 130nm
  - Results from the FNAL group presented by J.Hoff in May 2006. “Standard” FF from commercial library irradiated with monoenergetic protons (200MeV) at the Indiana University Cyclotron Facility, with devices operating as storage cells (no continuous clock). Measured cross section: $4.86 \cdot 10^{-14}$ $cm^{-2}bit^{-1}$
  - Results from the CERN ESE group presented at TWEPP07 and published in JINST. “Standard” FF from commercial library irradiated with Heavy Ions at UCL-CRC (Be), in static (no clock) or dynamic (clocked) conditions. Extrapolation of results to a mono-energetic 200MeV environment yields a cross section of $2 \cdot 10^{-14}$ $cm^{-2}bit^{-1}$



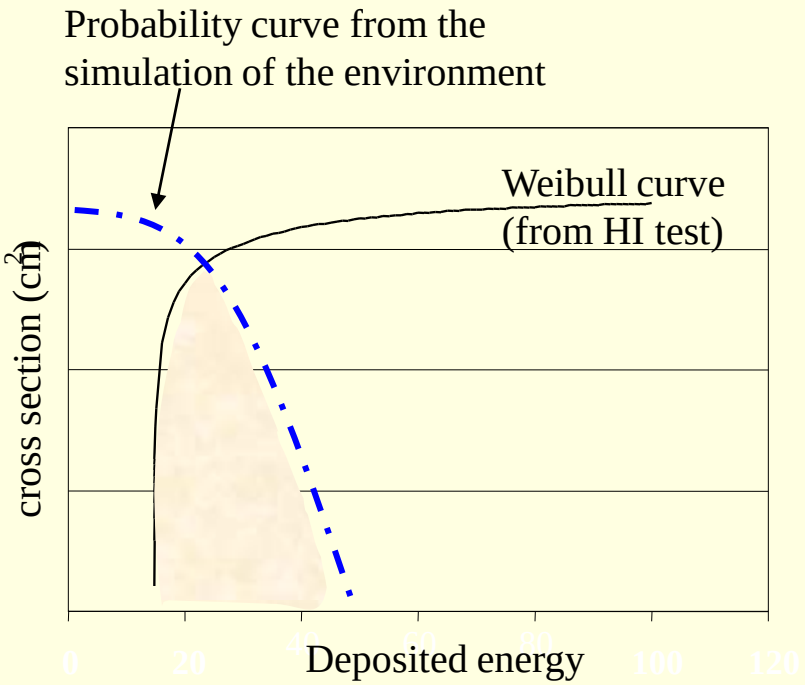
Comparison with 250nm FF

- Comparison with 0.25μm FF (using ELTs):
  - Cross-section of the commercial 130nm design orders of magnitude larger in LHC environment – the 0.25um design had a threshold close to the maximum LET possible from nuclear interaction in Si



Error rate projection for SRAM and FF (LHC/SLHC) (1)

It is possible to estimate the error rate in LHC by using the cross-section data measured using the Heavy Ion beam. This gives the information on the sensitivity of the circuit.
With this information and the estimate (from simulation) of the probability for energy deposition in LHC, it is possible to compute the “cross-section” of the SRAM and FF in the LHC environment. Detailed explanation of the procedure can be found in: M.Huhtinen and F.Faccio, NIM A 450 (2000) 155-172



	Estimate cross-section in LHC environment (cm^2/bit)	
	SRAM	FF
Pixel	2.9×10^{-14}	7.0×10^{-14}
Outer trk	2.5×10^{-14}	6.0×10^{-14}
Endcap ECAL	2.6×10^{-14}	6.3×10^{-14}
Exp hall	2.2×10^{-14}	5.2×10^{-14}

Error rate projection for SRAM and FF (LHC/SLHC) (2)

Error rate in different locations of LHC experiments (ATLAS, CMS)

Approximate at max luminosity, with cross-section = 2.8×10^{-14} cm^2/bit for the SRAM and 7×10^{-14} cm^2/bit for the FF

Barrel; radius =	Flux (all hadrons E>20MeV) particles/cm^2s	Error rate (SEU/bit s)	
		SRAM	FF
4 cm	5×10^7	1.4×10^{-6}	3.5×10^{-6}
12 cm	5×10^6	1.4×10^{-7}	3.5×10^{-7}
37 cm	2×10^6	5.6×10^{-8}	1.4×10^{-7}
52 cm	1×10^6	2.8×10^{-8}	7.0×10^{-8}
100 cm	5×10^5	1.4×10^{-8}	3.5×10^{-8}

For SLHC, multiply the error rate by 5-10 depending on luminosity increase.
For example:
for a circuit with 100 bits, at 12 cm, we estimate about 1-2 errors/hour in SLHC

Interpretation

- Error rates of ‘standard’ cells in 130nm are much larger than what we had in our 0.25um designs (where we used ELTs)
- If the error rates figured out above are not acceptable for our application, we need to protect the registers/memories with some technique
  - This could just work as well irrespective of the applied Vdd
- If the error rates are instead marginally acceptable, a change of Vdd might increase them (by a factor of ?) and make it unacceptable