SEU WORKING GROUP

GOALS

Define Level and Types of SEE Problems

Appropriate Mitigation

What's already done

needs Study

Provide Repository for Results

TWEPP 2010

Mitigation of Single Event Effects

SEE Domains

- ASIC Design → Today's topic
- FPGA Design → J. Christiansen announcement

Determine Mitigation requirements

Acceptable rates of

- Compromised of functional fidelity
- Loss of data integrity

What Level of mitigation is required?

Which ASIC Technology ?

SEE sensitive Parameters to Understand / Study / Investigate

- Sensitive node spacing
- Relevant time frame (SEE lifetime)
- Supply sensitivity
- CC sensitive volume → Triple Well, T3, Substrate resistivity
- Enclosed Gate SEE advantages
- Power / Real estate / Development time costs of mitigation
- More??

CAD friendly Approach → Use Standard Digital Library parts

DICE, TMR Time delay

- Device spacing
- Supply Sensitvity

→ Integrate custom part into Digital Library ??

→ Analog Approach for small special purpose blocks

-- encoder / decoder counters pwr up reset etc.