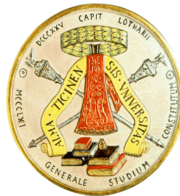
A 3D vertically integrated deep n-well CMOS MAPS for the SuperB Layer0

G. Traversi[a], L. Gaioni[c], M. Manghisoni[a], L. Ratti[b], V. Re[a]



[a]Università degli Studi di Bergamo and INFN Pavia

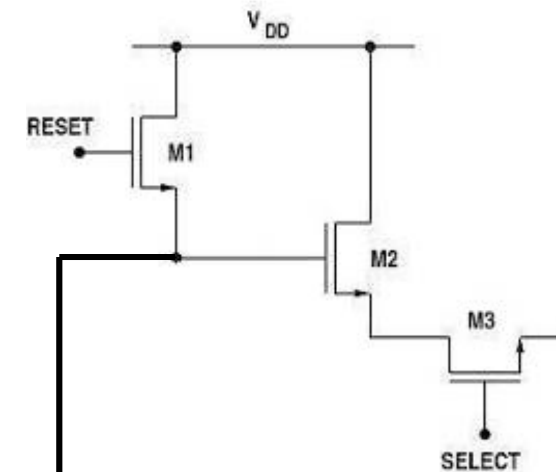
[b]Università degli Studi di Pavia and INFN Pavia

[c]INFN Pavia

CMOS Monolithic Active Pixel Sensors

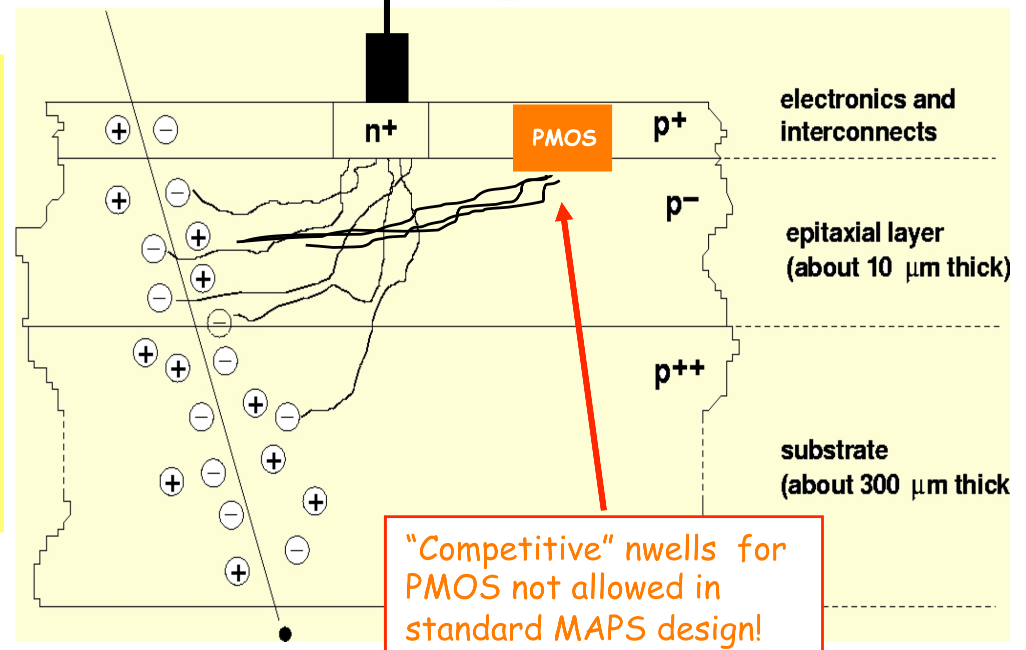
Principle of operation

- The undepleted epitaxial layer acts as a potential well for electrons
- Signal (~1000 e-) collected through diffusion by the n-well contact
- Charge-to-voltage conversion provided by the sensor capacitance → small collecting electrode
- Simple in-pixel readout (additional nwells for PMOS not allowed in standard MAPS design!) → sequential readout

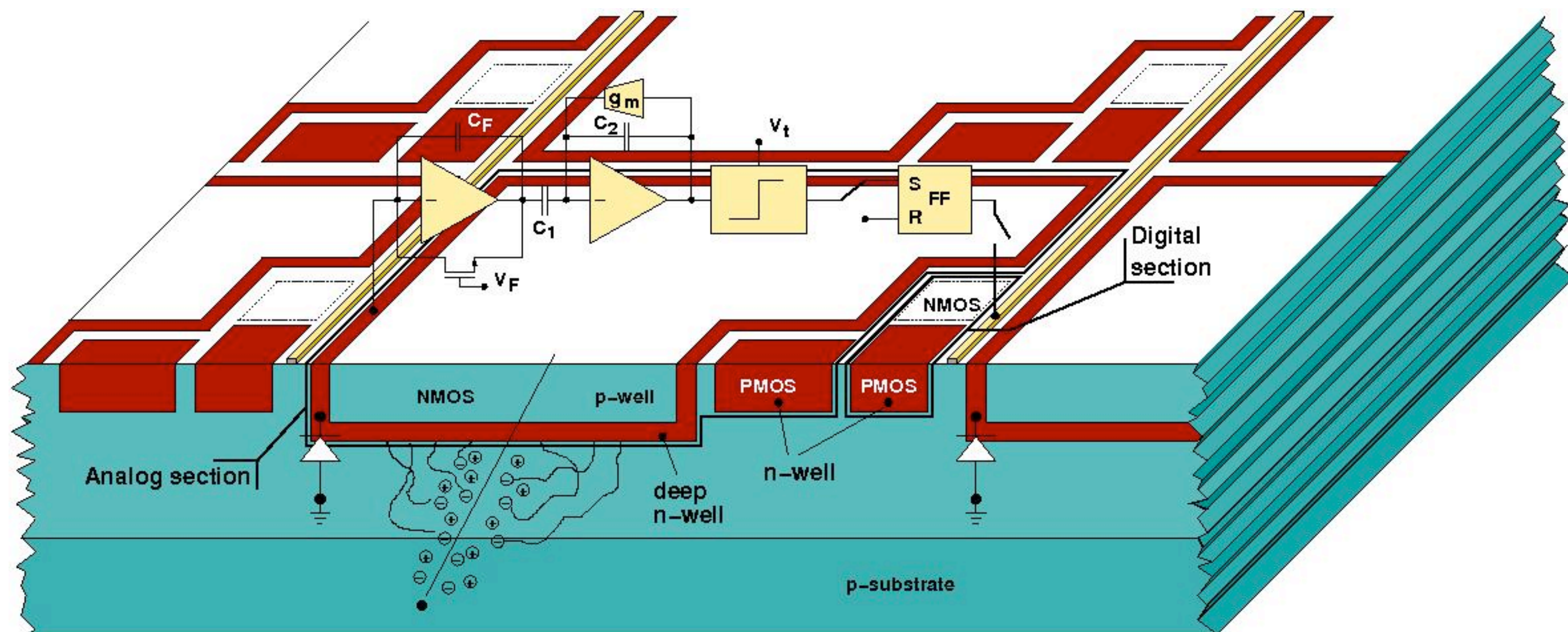


Several reasons make them very appealing as tracking devices :

- detector & readout on the same substrate
- wafer can be thinned down to few tens of um
- radiation hardness (gate oxide ~nm thick)
- high functional density and versatility
- low power consumption and fabrication costs



Deep N-Well (DNW) sensor concept



- ✓ New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential
- ✓ Large scale of integration of deep sub micron CMOS processes is exploited to perform signal processing at the pixel level
- ✓ Deep n-well (DNW) is used to collect the charge released in the substrate
- ✓ A standard readout channel for capacitive detectors is used for Q-V conversion
- ✓ NMOS devices of the analog section built in the deep n-well
- ✓ Bias to the DNW is provided by the preamplifier input
- ✓ If the DNW takes a large fraction of the cell, PMOS devices can be safely included in the design

DNW MAPS R&D activity

Chip	Description
TEST_STRUCT	ST 130 Process characterization
APSEL0	Preamplifier characterization
APSEL1	Improved F-E 8x8 Matrix
APSEL2M	Cure thr disp. and induction
APSEL2T	Accessible pixel Study pix resp.
APSEL2_90	ST 90nm characterization
APSEL2D	Test digital RO architecture
APSEL2_CT	Test chips for shield, xtalk
APSEL3D	8x32 matrix. Shielded pixel - Data Driven sparsified readout
APSEL3_T1, T2	Test chips to optimize pixel and FE layout
APSEL5T	Shaperless front-end, smart sensor layout

APSEL4D

32x128 pix - 50 μm pitch

perif & spars logic

- 4k pixel (32x128, 50um pixel pitch)
- In-pixel sparsification and timestamping + data driven readout
- Pixel cell and matrix: full custom design and layout
- Sparsification logic synthesized with sdt. cell from VDHL model
- Beam test in Sept. 2008
- Radiation test up to 10 MRad

APSEL4D: 4096 pixel matrix with data driven sparsified readout + timestamp

The implemented architecture was designed with special attention to minimize:

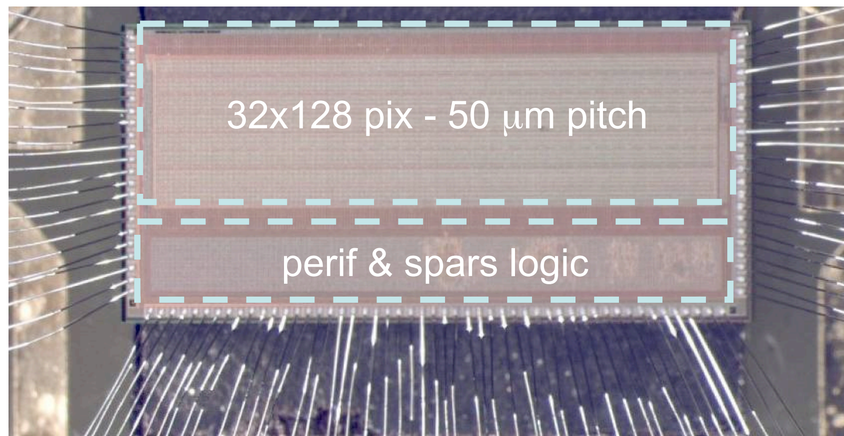
- In-pixel PMOS (competitive nwells) to preserve the collection efficiency
- Digital lines crossing the sensor area
- Dead time of the detector

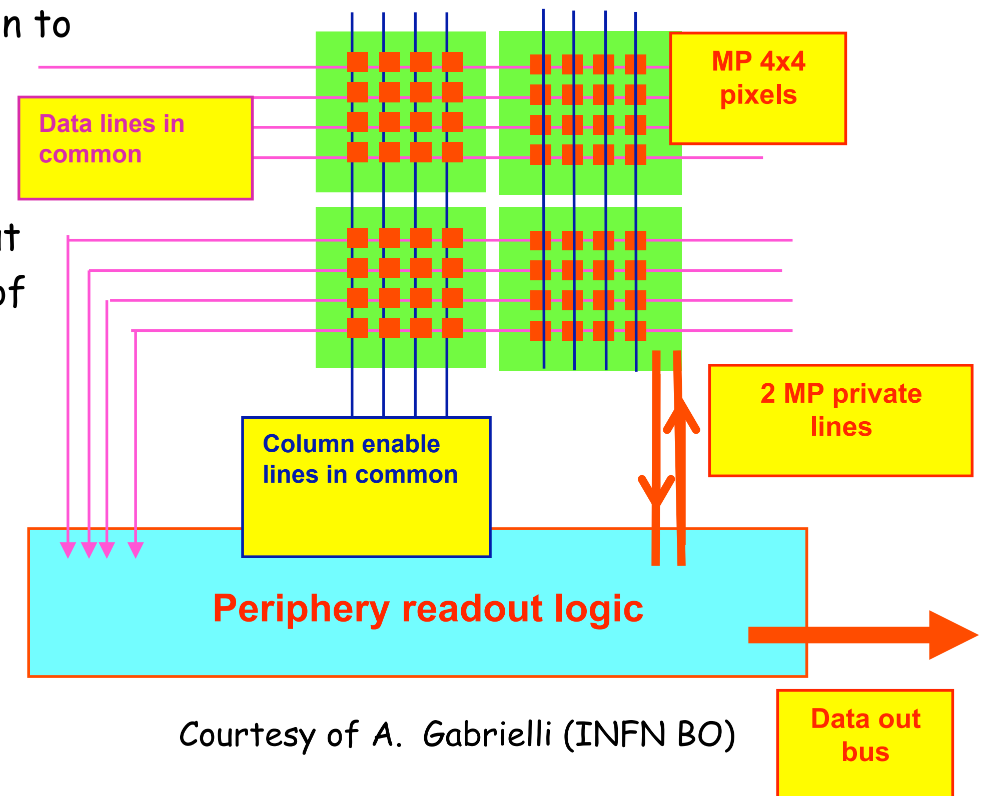
✓ S/N up to 25 with power consumption ~ 30 uW/ch

✓ 4K(32x128) 50x50 um^2 matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic

Periphery readout logic:

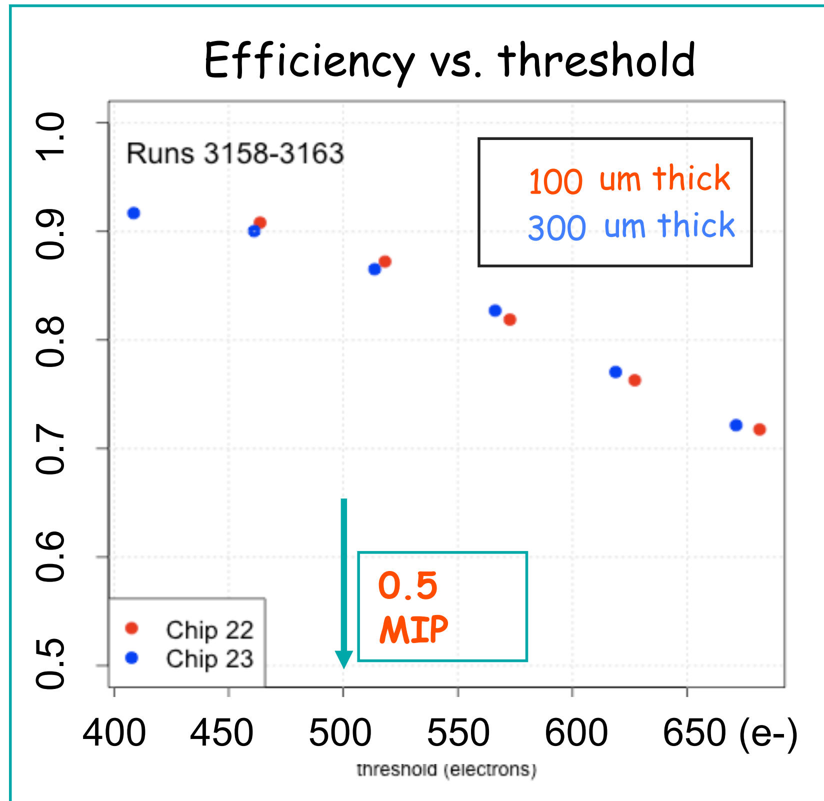
- ✓ Register hit MP & store timestamp
- ✓ Sweeps the matrix contin. enabling MP readout
- ✓ Receive, sparsify, add TS and send data out of the chip





Courtesy of A. Gabrielli (INFN BO)

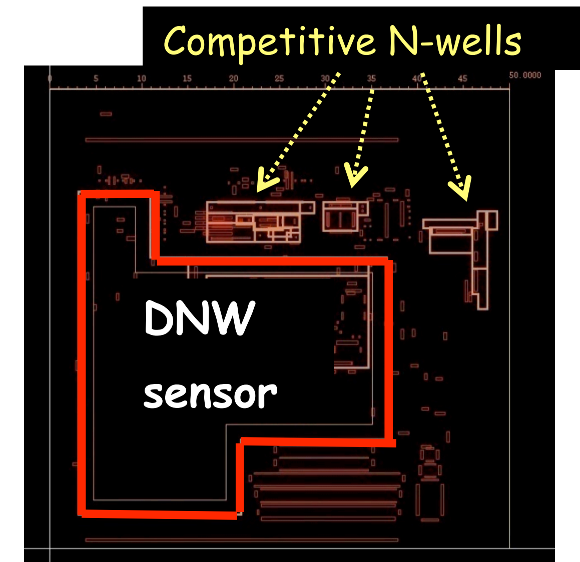
APSEL4D: Hit Efficiency measured in a CERN beam test



Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

- ✓ MAPS hit efficiency up to 92% with threshold @ 400e- (~ 4σ_noise+2σ_thr_disp)
- ✓ 300 and 100um thick chips give similar results
- ✓ Intrinsic resolution ~ 14um compatible with digital readout

Competitive N-wells (PMOS) in pixel cell can steal charge reducing the hit efficiency

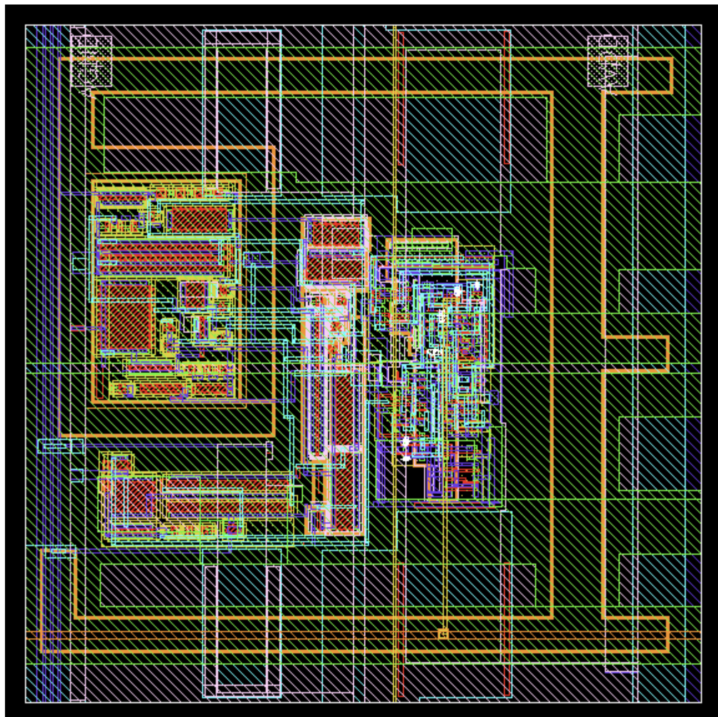


Optimization of the sensor layout

Small size prototype module with functionalities and cooling/mechanics close to SuperB specifications needs a **128x128 (or 320x80) MAPS chip (APSEL5D)** with 40um x 40um pixel cells

- ✓ With respect to APSEL4D, scaling to larger matrix size dictates to remove the shaper stage to make room for additional macropixel private lines and to reduce the pixel pitch
- ✓ Inside the pixel cell, sensor layout has to be changed (wrt APSEL4D) to increase detection efficiency

Apsel5T pixel layout



- ✓ Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- ✓ Optimized cell with **annular shape layout** (left): efficiency ~ 99% from TCAD, promising results from laser test, beam test in 2011.

Charge collecting electrode with annular shape

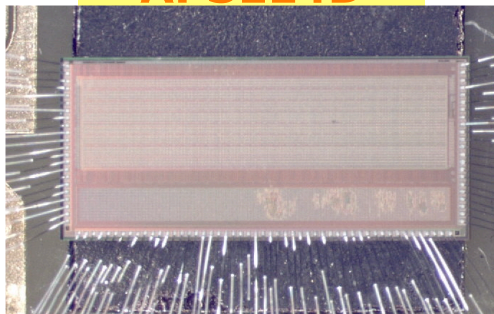
Sensor area: 480um^2
NW-PMOS area: 70um^2
Fill Factor: 0.87

After 5 years of R&D….

130 nm DNW MAPS: CMOS sensors with in-pixel sparsification and time stamping

(130 nm STM CMOS process)

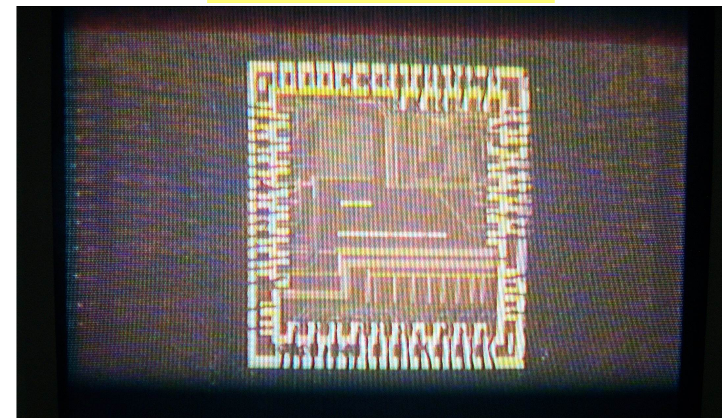
APSEL4D



32x128 matrix.
Data Driven,
continuously
operating sparsified
readout
Beam test Sep. 2008

50x50 μm pitch

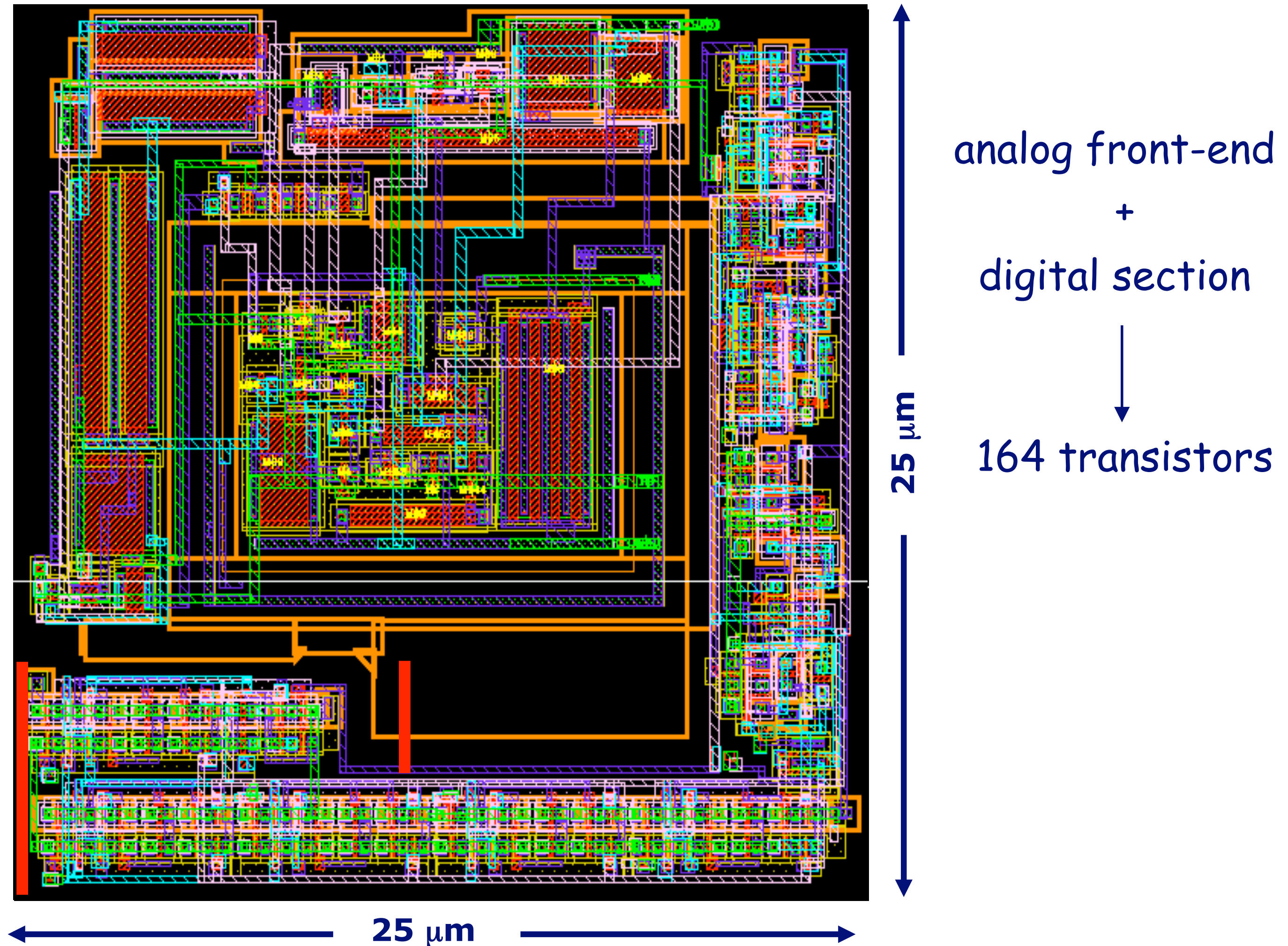
SDR0



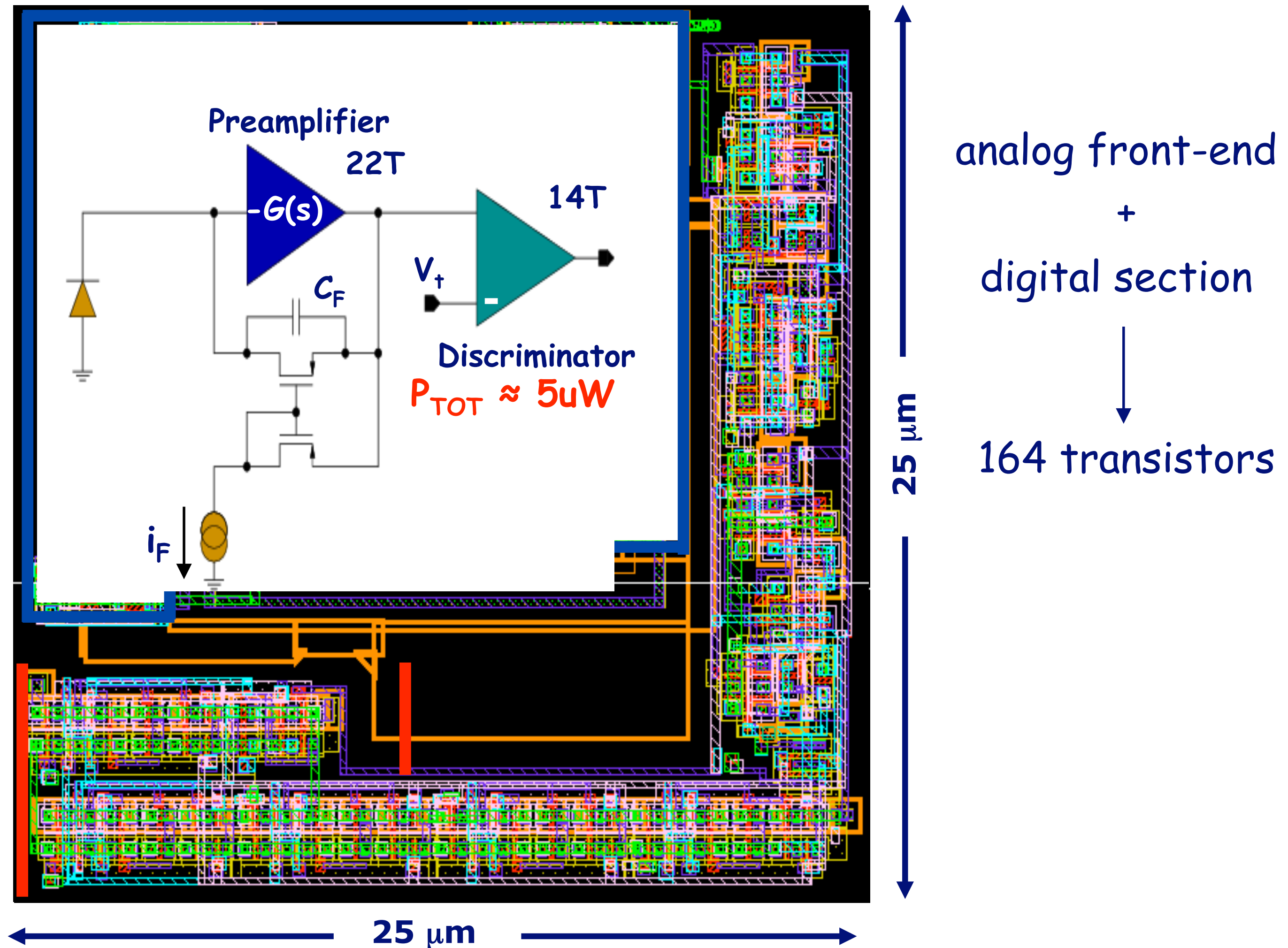
16x16 matrix + smaller test structures. Intertrain sparsified readout

25x25 μm pitch

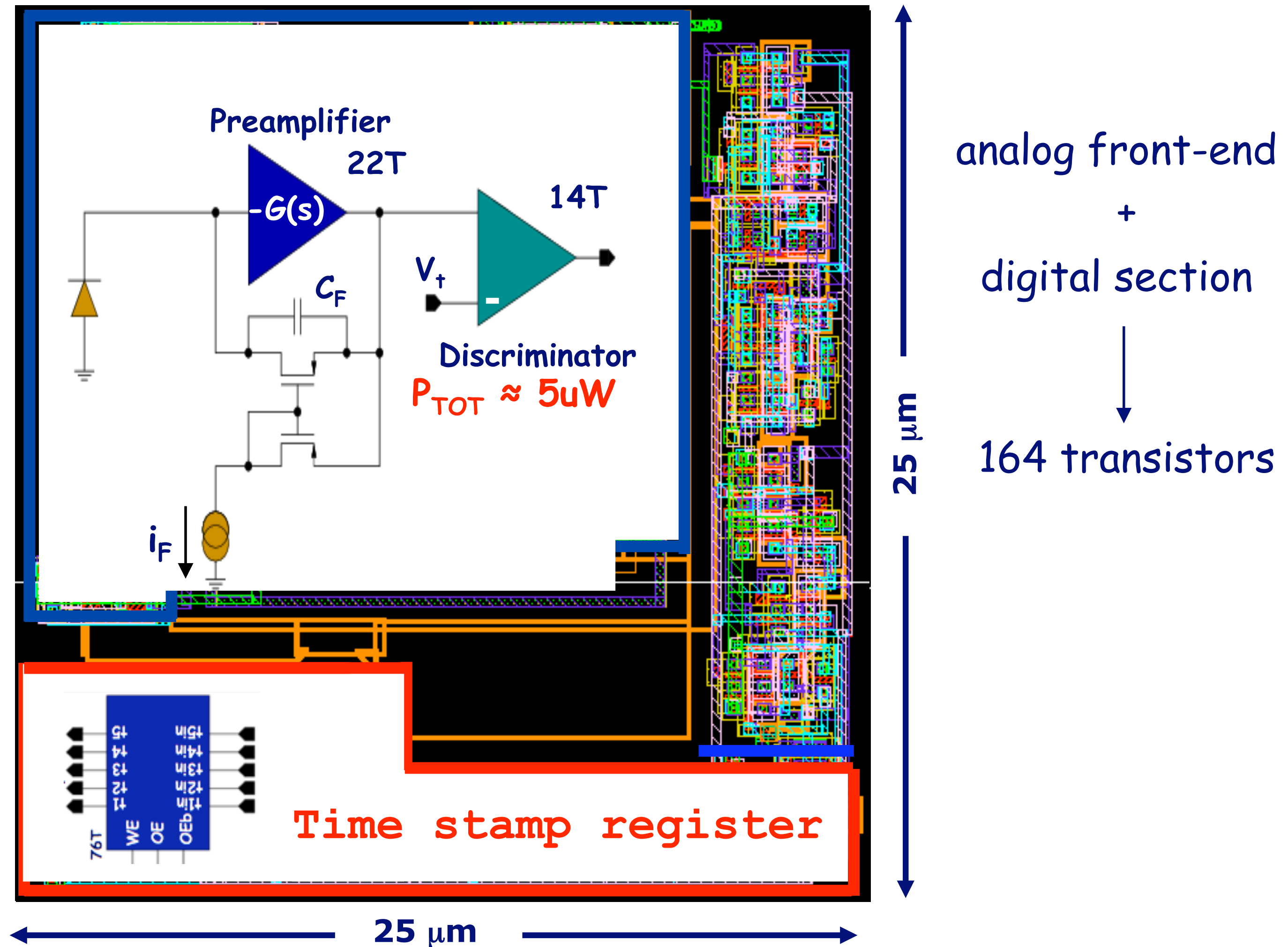
The SDR0 pixel



The SDR0 pixel

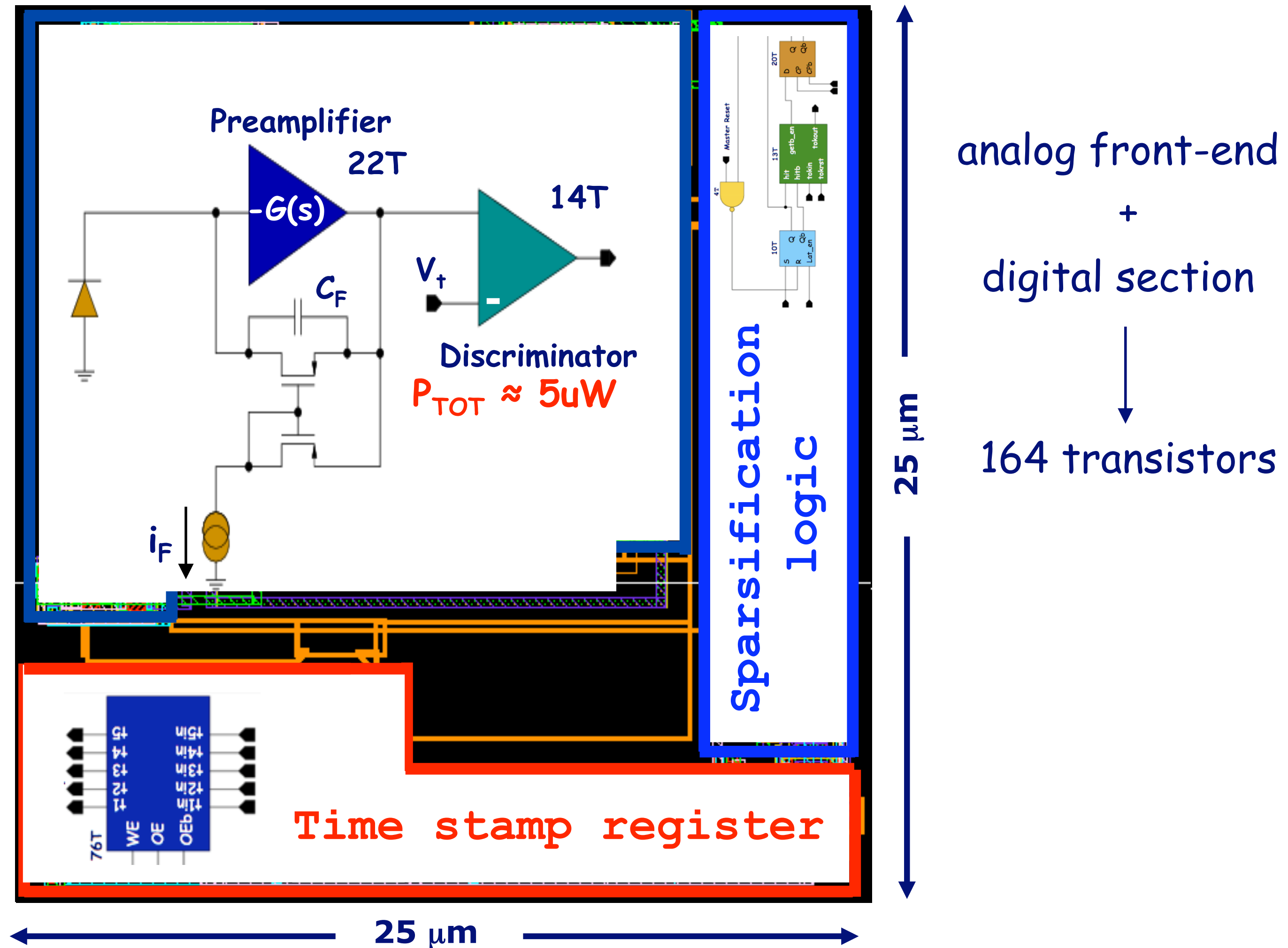


The SDR0 pixel



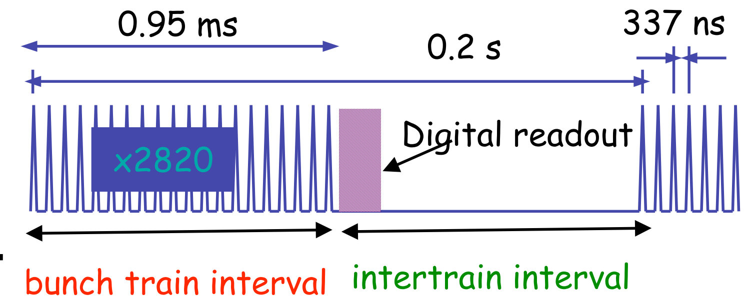
analog front-end
+
digital section
↓
164 transistors

The SDR0 pixel



Intertrain Readout Architecture for "ILC" MAPS (SDR0 chip)

Suggested by FNAL IC design group, first implemented in the VIP chip



Readout CK

MUX

X Y T

Serial data output

Cell CK

X=1 X=2 X=1

Time Stamp Buffer 1

Time Stamp Buffer 2

Time Stamp Buffer 16

First token in

Cell (1,1) Cell (1,2) Cell (1,16)

Cell (2,1) Cell (2,2) Cell (2,16)

Cell (16,1) Cell (16,2) Cell (16,16)

gXb TS Tkin Tkout gYb

Y=1 Y=2 Y=16

Last token out

gXb=get_X_bus

gYb=get_Y_bus

TS=Time_Stamp

Tkin=token_in

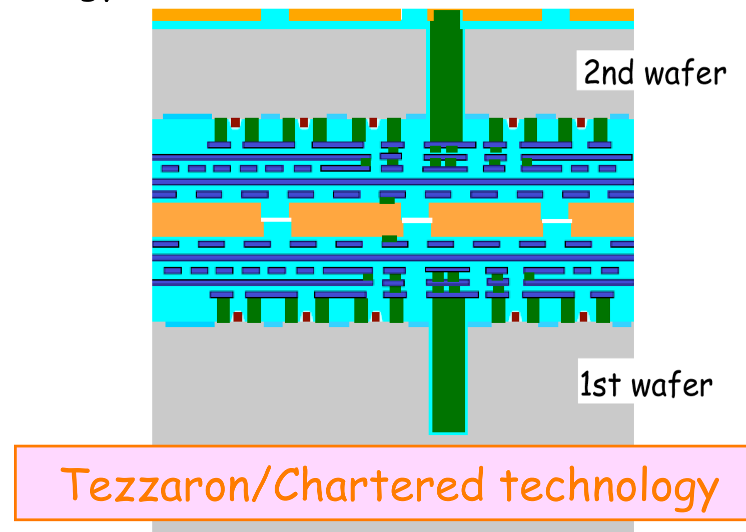
Tkout=Token_out

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

3D IC Multi-Project Wafer Run

3DIC Consortium:

- ✓ In late 2008 a large number of international laboratories and universities with interest in high energy physics joined in a consortium leaded by Fermilab for the development of 3D integrated circuits (presently comprised by 17 institutions from 7 countries)
- ✓ This Consortium, as a first step, is going to investigate 3D devices based on two layers ("tiers") of the 130 nm CMOS technology by Chartered Semiconductor, vertically integrated with the Tezzaron interconnection technology

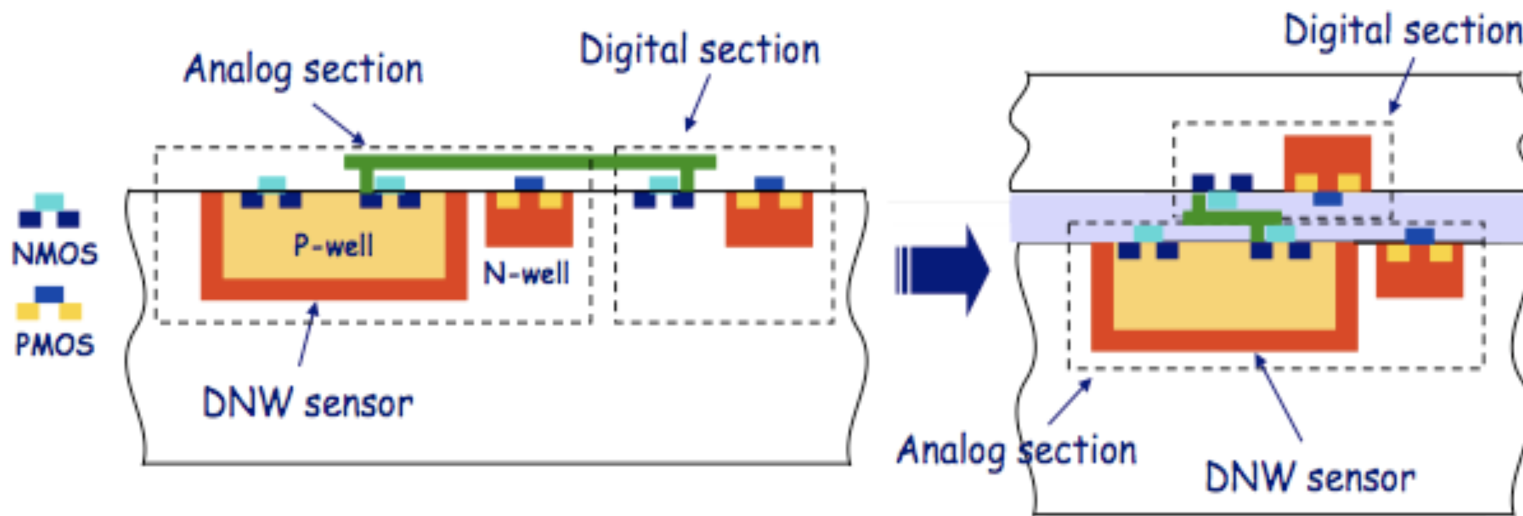


Tezzaron/Chartered technology

Tezzaron Vertical Integration Process:

- ✓ multi-tier chip
- ✓ standard CMOS process by Chartered Semiconductor, Singapore
- ✓ Vias are very small
- ✓ Vias can be placed close together

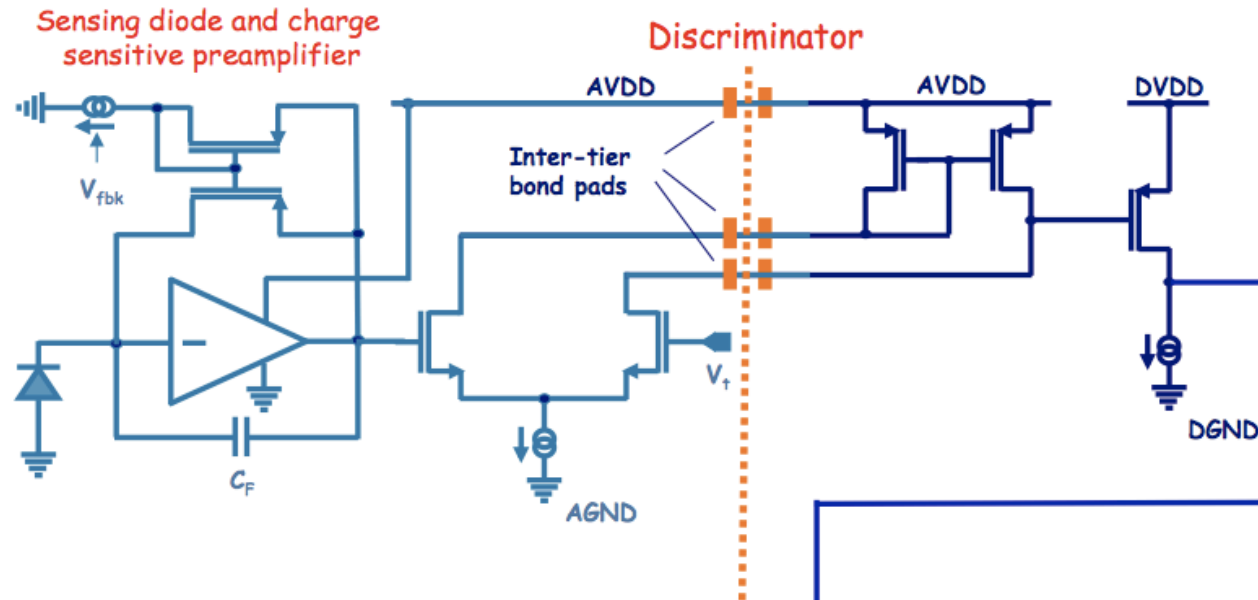
The first 3D CMOS MAPS in the APSEL family



Separate analog from digital section to minimize cross-talk between digital blocks and sensor/ analog circuits

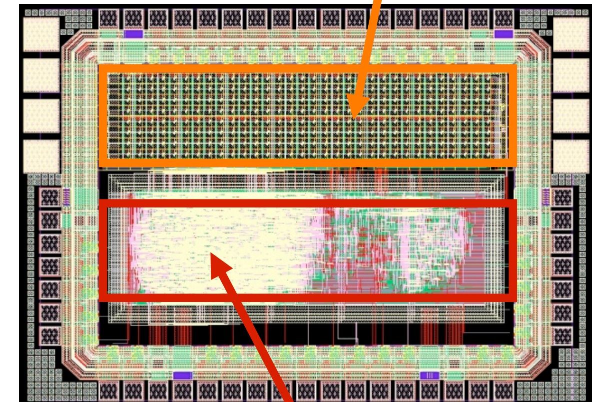
- Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator
- Tier 2: digital front-end (latch for hit storage, pixel-level digital blocks for sparsification) and digital back-end

3D MAPS pixel cell



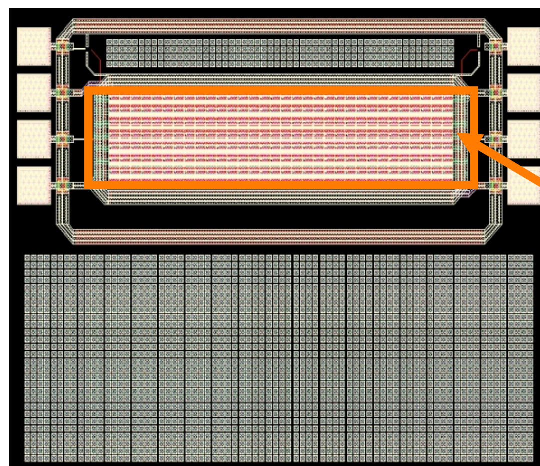
TIER 2 (TOP)

Pixel-level digital front-end (designed by INFN-Pisa)



Digital readout electronics (designed by INFN-Bologna)

TIER 1 (BOTTOM)

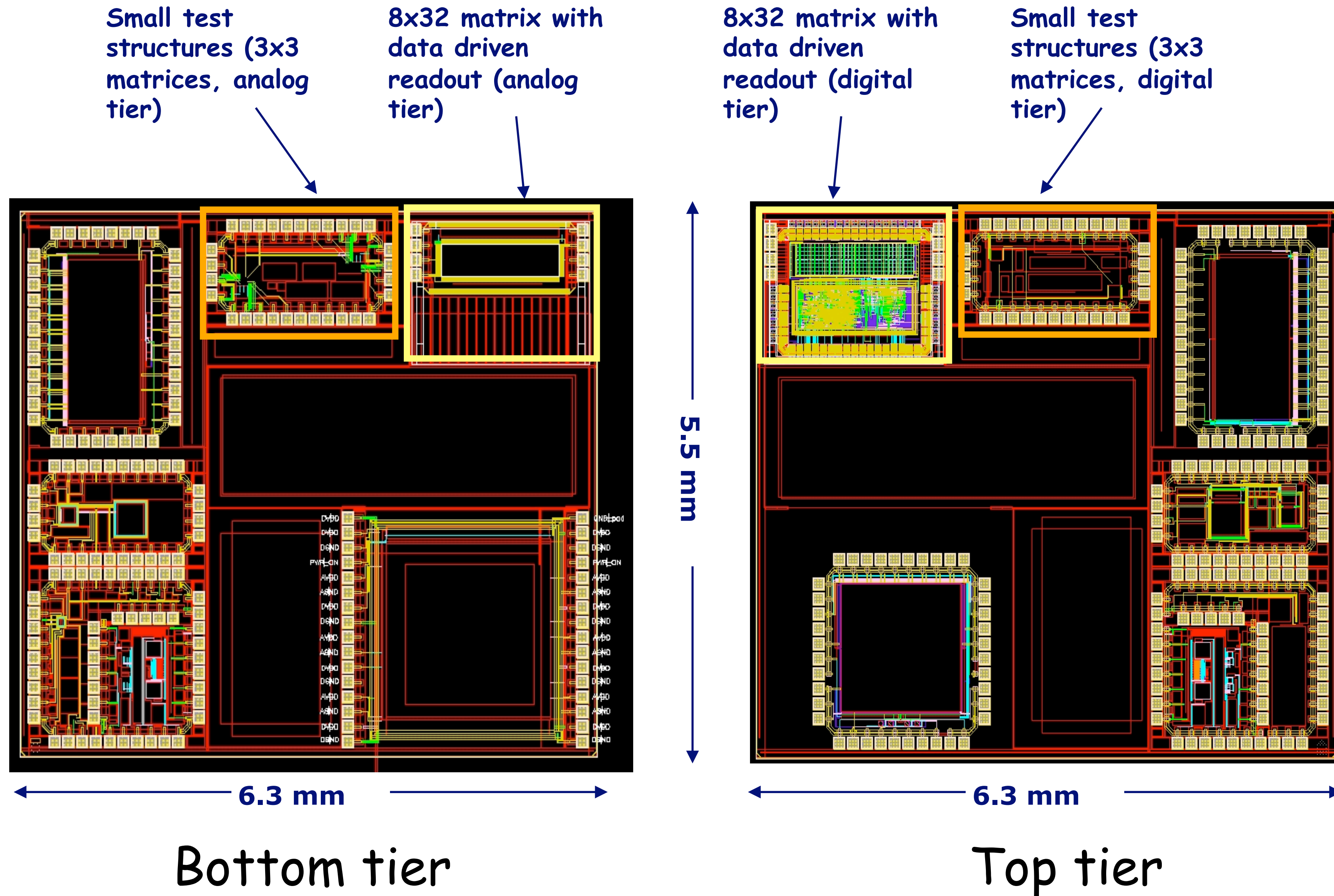


8x32 pixel matrix

Pixel-level sparsification logic

3D integration removes layout constraints and will allow for an improved readout architecture (no macropixel) in future chips

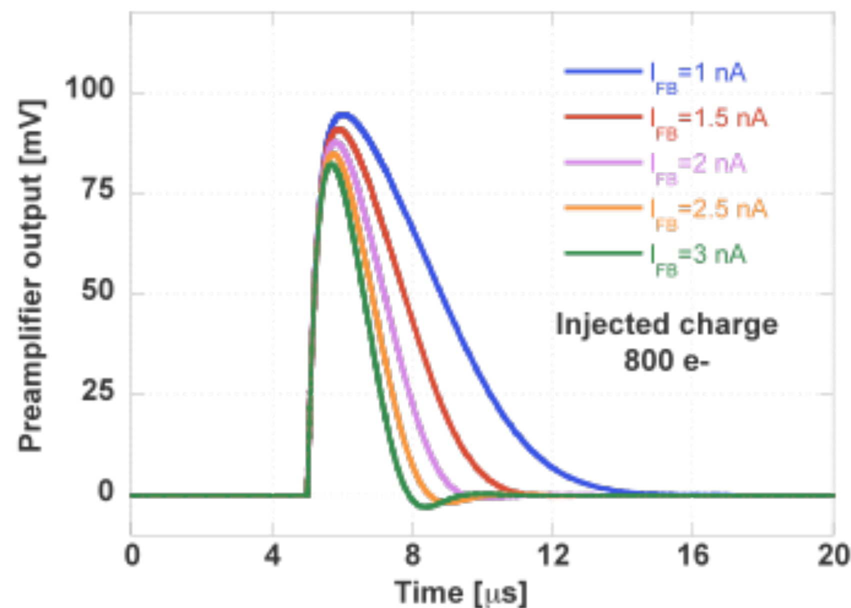
Test structure chip layout

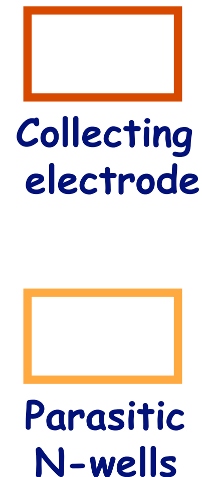


Exploiting 3D integration: pixel pitch and sensor efficiency

Main design features and simulation results

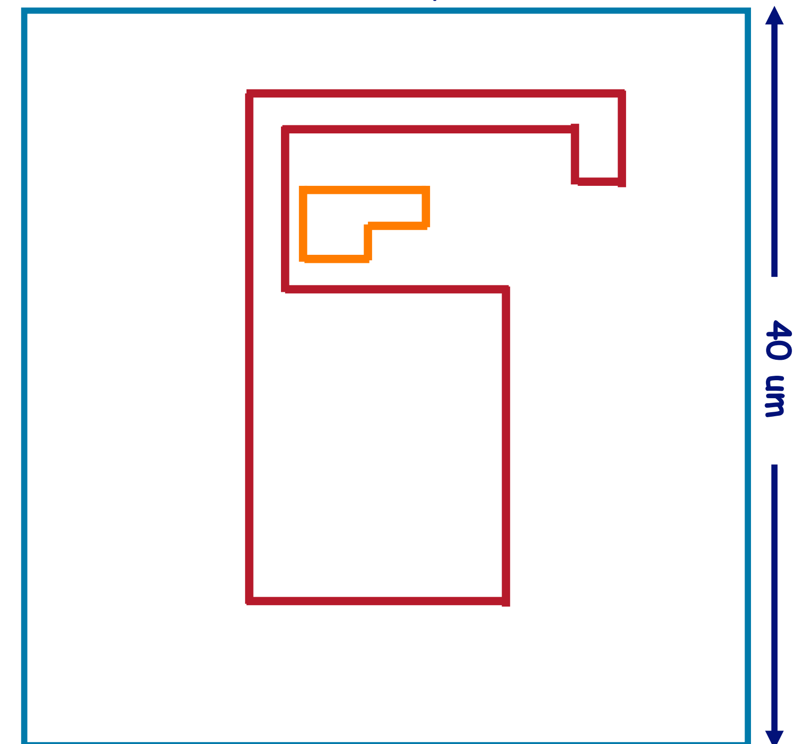
- ✓ W/L=30/0.3
- ✓ C_D=250 fF
- ✓ ~1 us peaking time
- ✓ Charge sensitivity: 750 mV/fC
- ✓ Equivalent noise charge (ENC): 33 e rms
- ✓ Threshold dispersion: 40 e rms





3D Tezzaron-Chartered technology

Sensor layout

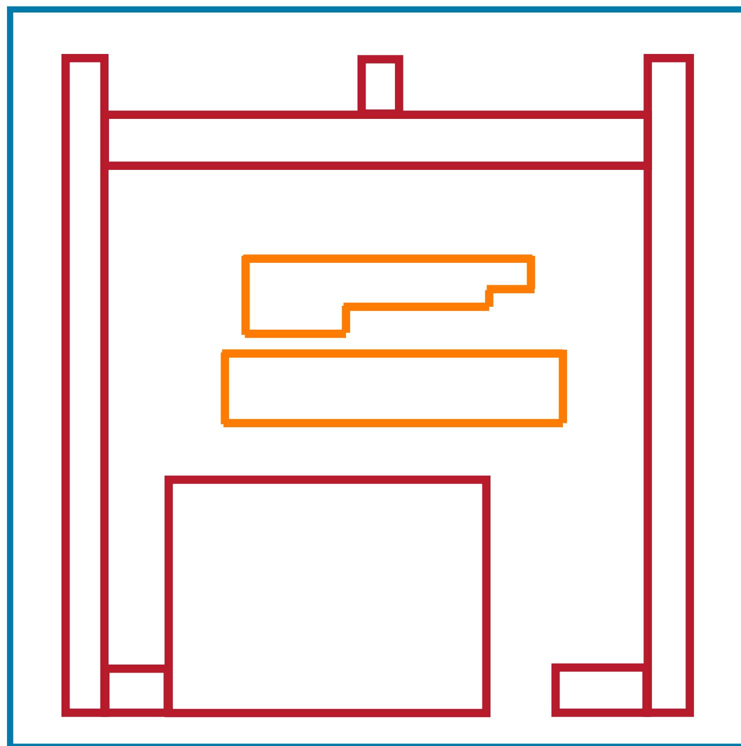


Sensor area: 346mm^2
NW-PMOS area: 22mm^2
Fill Factor: 0.94 (0.87 in the "2D" version)

Exploiting 3D integration: pixel pitch and sensor efficiency

A three-dimensional technology makes it possible to significantly reduce the area of charge stealing N-wells → significant improvement in charge collection efficiency expected

2D CMOS technology (Apsel5T cell)



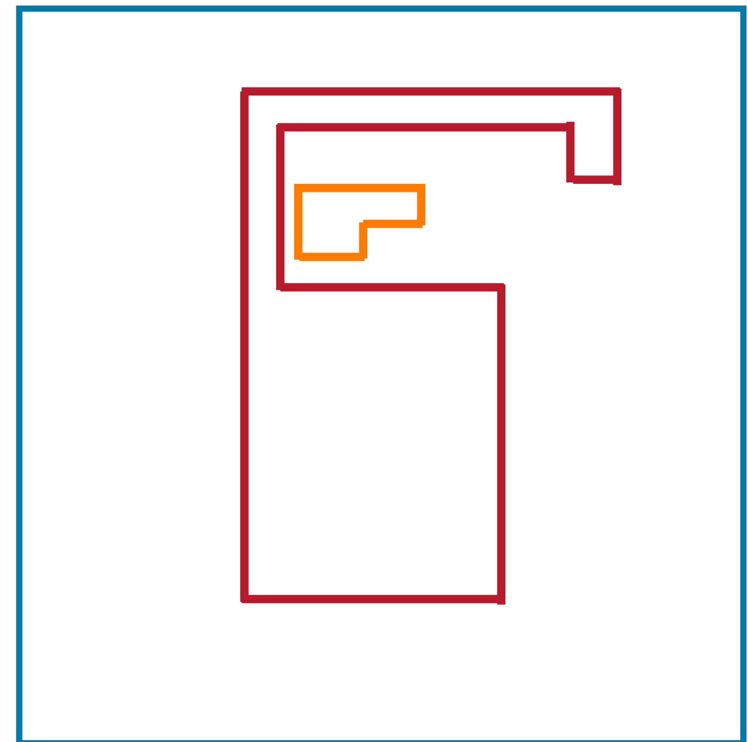
40 um

Collecting electrode

Parasitic N-wells

3D Tezzaron-Chartered technology

Sensor layout



40 um

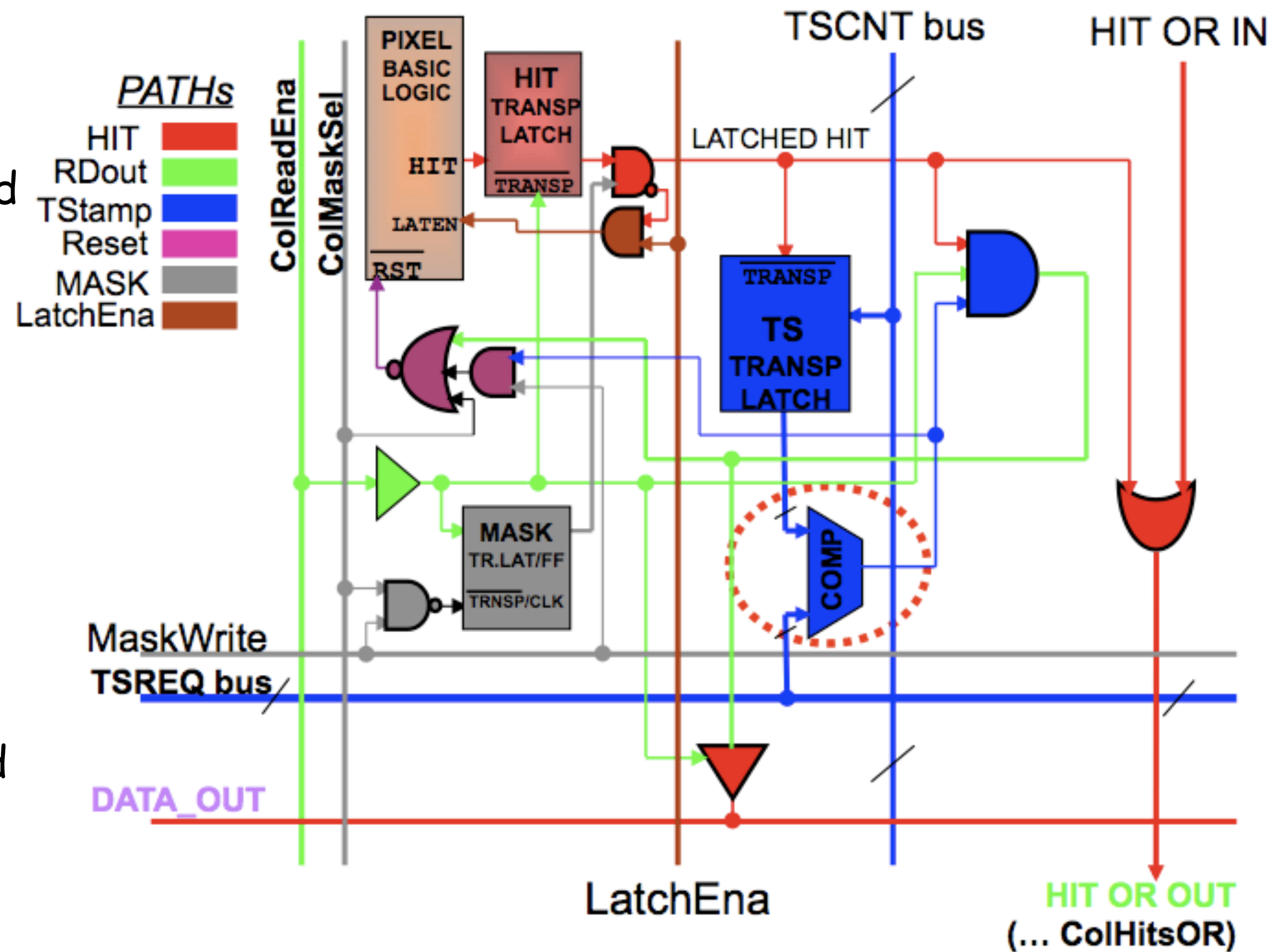
Sensor area: 346mm^2

NW-PMOS area: 22mm^2

Fill Factor: 0.94 (0.87 in the "2D" version)

Exploiting 3D integration: pixel-level logic with time-stamp latch and comparator for a time-ordered readout

- ✓ A readout time stamp enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that time stamp
- ✓ A column is read only if HIT-OR-OUT=1
- ✓ DATA-OUT (1 bit) is generated if the active column has hits associated to a selected time stamp

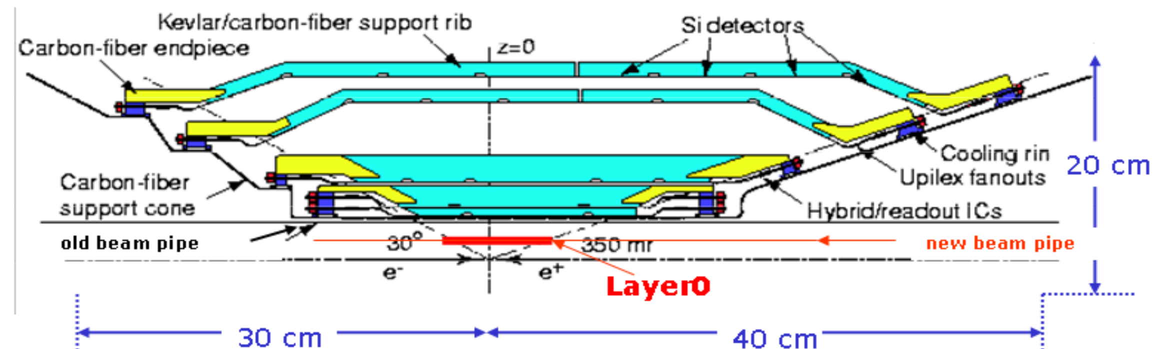


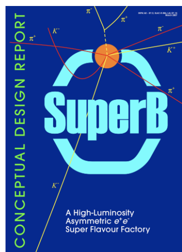
Courtesy of F. Morsani (INFN PI)

A possible application of DNW MAPS: SuperB SVT Layer0

- ✓ The SuperB accelerator concept allows to reach the luminosity threshold $L=10^{36}$ cm^{-2} s^{-1}
- ✓ Need a new SVT (very similar to the 5 layer BaBar SVT) supplemented by a new Layer 0 to measure the first hit as close as possible to the production vertex. Goal is coverage to 300mrad both forward and backward.

- ✓ Layer0 very close to the IP (≈1.5cm)
- ✓ Low material budget (<1% X_0)
- ✓ Fine granularity (≈ 50um pitch)
- ✓ High radiation tolerance (>15MRad/yr)
- ✓ Large background (>100MHz/cm^2)





- ✓ Government approval expected very soon (SuperB is the first project in National Research Plan of the Italian Research Ministry)
- ✓ TDR: spring 2011
- ✓ Operation by 2015

SuperB SVT Layer0 technology options

➢ **Striplets:** thin double sided silicon sensor with short strips. Mature technology, not so robust against background occupancy. Marginal with background rate > 100MHz/cm^2

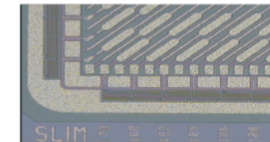
➢ **Hybrid Pixel (HP):** viable option but slightly marginal

- Reduction of total material budget at 1% X_0 feasible
- Reduction of front-end pitch to 50x50um^2
- Fabricated and tested front-end prototype chip with 50x50um^2 pitch with fast data push readout (4k-pixels, 32x128)
- Pixel detectors (high resistivity) fabricated by FBK-IRST, interconnection with FE chip by IZM (Munich) in progress
- **Thin pixels with Vertical Integration**: two tiers of FE chip + high resistivity sensor (interconnected by Ziptronics or Zycube)

➢ **DNW MAPS in a planar (2D) technology:** very promising technology, sensor & readout in 50um thick chip. Extensive R&D (SLIM5-Collaboration) on Deep N-Well devices. New sensor layout with improved charge collection efficiency fabricated and tested.

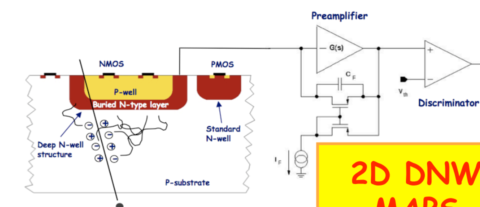
➢ **DNW MAPS in a vertically integrated (3D) technology:** 130nm CMOS technology provided by Chartered/Tezzaron semiconductor. First prototype with APSEL structures submitted.

Layer0 technology options



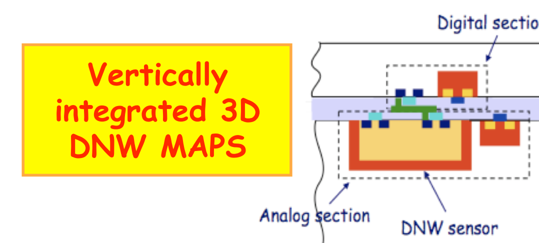
Striplets

Hybrid pixels



2D DNW MAPS

Vertically integrated 3D DNW MAPS



Lower material & improved performance

Conclusions

- Deep N-Well MAPS have the ambition of being monolithic devices with similar functionalities as hybrid pixels (e.g.: pixel-level sparsification and time stamping)
  - A first DNW MAPS matrix (APSEL4D) with in-pixel sparsification and timestamp has been tested with beams showing very encouraging results
- Their performance can greatly benefit from 3D vertical integration in terms of both electronics and sensors
  - First prototype with Apsel structures submitted in the first MPW run (by end 2010)
- They are candidates for the innermost layer of the Silicon Vertex Tracker at the high luminosity SuperB Factory
  - Plan to exploit the vertical integration both for DNW MAPS and hybrid pixel (front-end chip with two tiers of electronics)
  - Italian collaboration (VIPIX) is going to design in the next 3D MPW (spring 2011):
    - DNW MAPS: 128x100
    - FE chip for hybrid pixels: 32x128, 50um pitch

Acknowledgements

The SuperB SVT group and the VIPIX collaboration for providing information and useful discussion