Status Report on a MicroTCA Card for HCAL Trigger and Readout at SLHC

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R&D Goals

Upgrade of CMS HCAL:

Increase the ADC channel count by about 4x without an increase in the number of links from the HCAL Front End to the Back End.

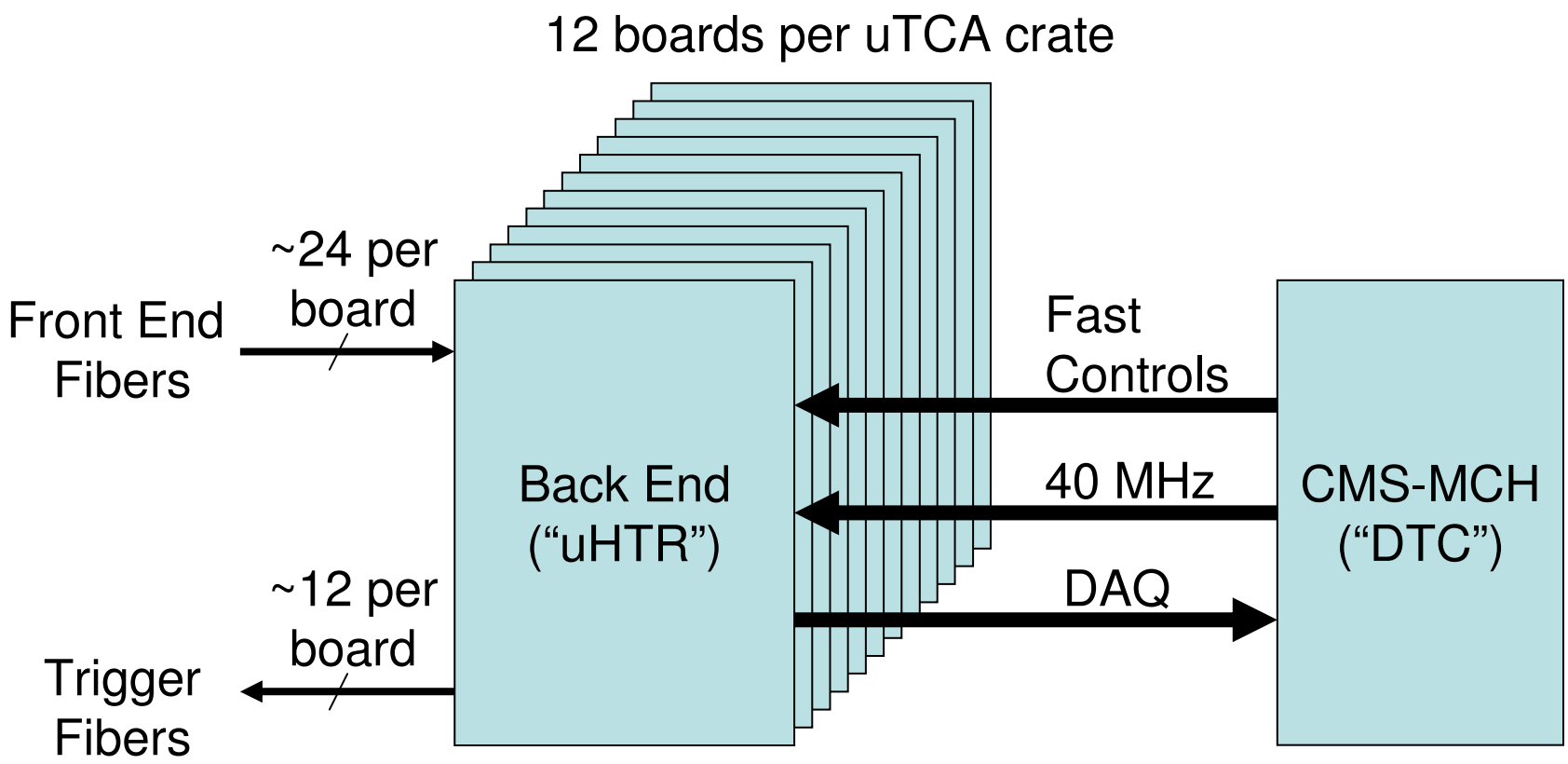
HCAL Data Philosophy: Every sample from the ADCs at the Front End goes to the Back End L1 pipelines and trigger primitives.

University of Minnesota R&D is involved in achieving the required speed and stability of communication links in the CMS environment.

Current data rate: 1.6 Gbps
Upgraded data rate target: 4.8 Gbps

(Upgraded data format is also slightly more compact.)

R&D Goals



HCAL Trigger and Readout Board – System Concept

MiniCTR2 is board built at UMN that evaluates the key elements of the uHTR System Concept, but with reduced link counts.

R&D Goals

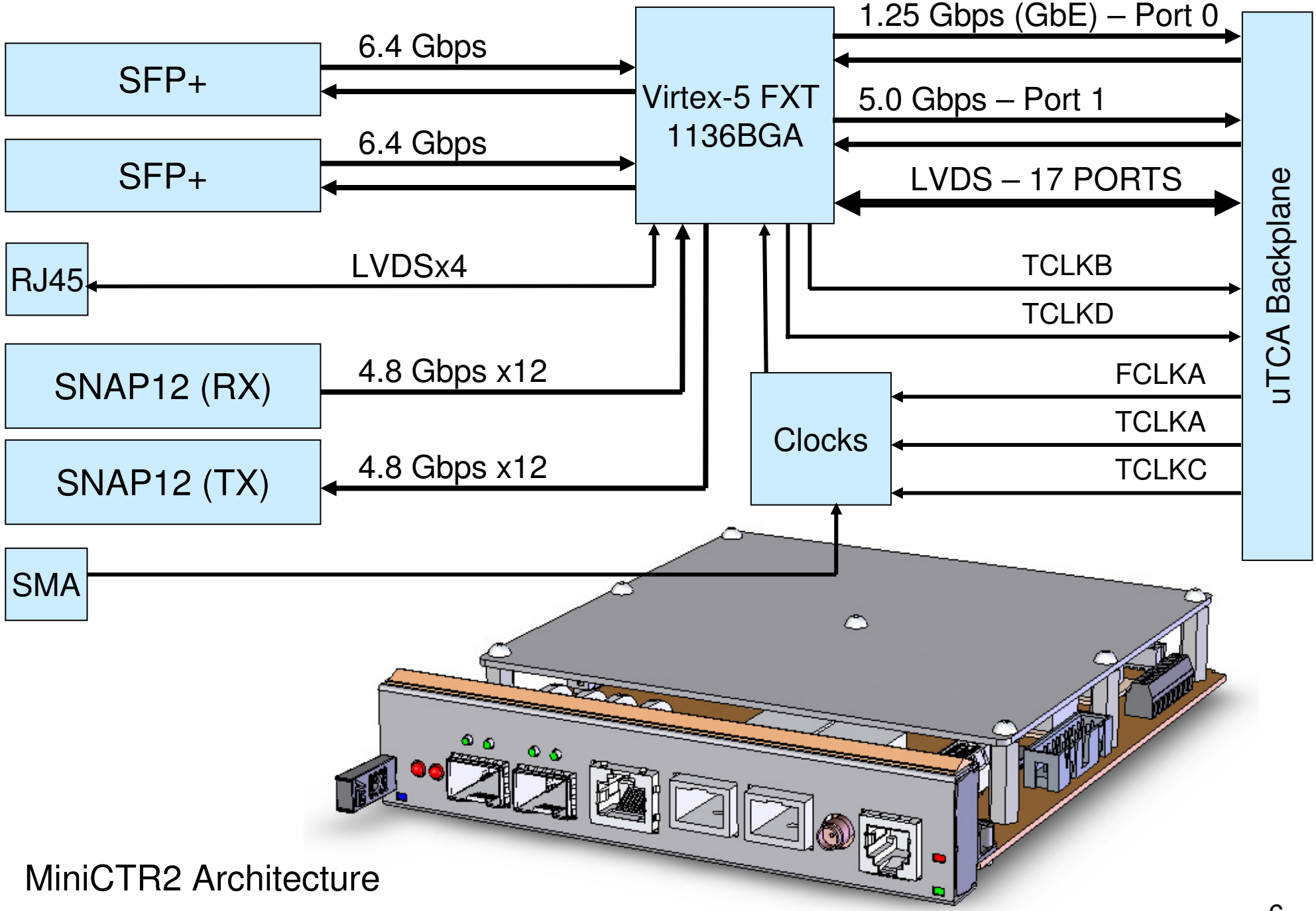
Discussion Topics:

- MiniCTR2 Architecture
- Bit Error Rate Tests
- 4.8 Gbps Serial Data Integrity Analysis
- “IPbus” Control Concept
- MiniCTR2b Architecture
- Communication with a Front End Prototype
- Communication with a CMS-MCH

  Successful integration of FPGA firmware from the CMS-MCH group (previous speaker). MiniCTR2 received 40 MHz Clock and Fast Controls from a CMS-MCH across a MicroTCA backplane.

MiniCTR2 Architecture

MiniCTR2 Architecture



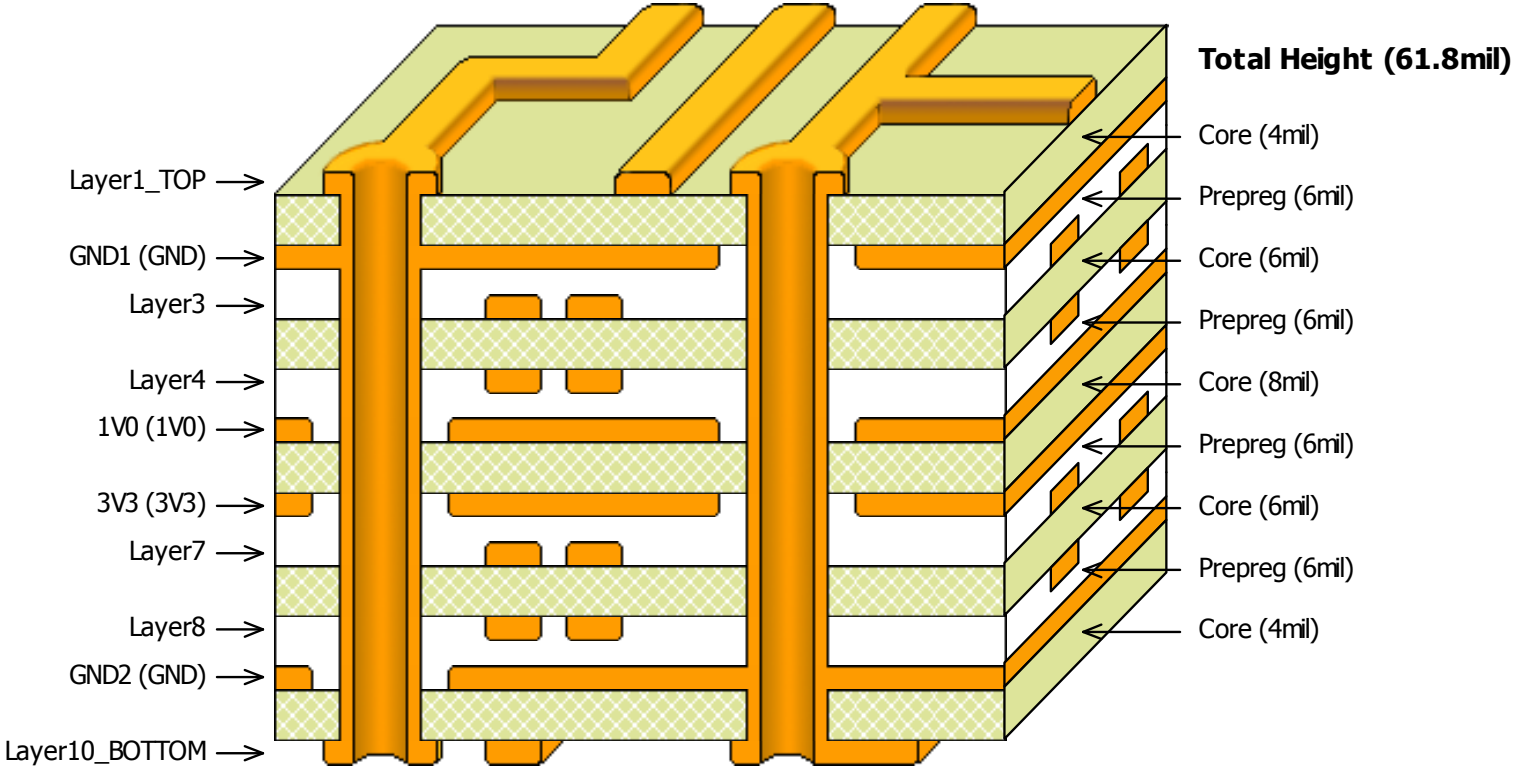
MiniCTR2 Architecture

MiniCTR2 Architecture

MiniCTR2 Features:

- Xilinx XC5VFX70T-1FFG1136C FPGA
  - 16 GTX high-speed serial links (datasheet says max. 4.25 Gbps)
- Two SFP+ Optical Transceivers (6.4 Gbps)
- SNAP12 12-channel Optical Transmitter (4.8 Gbps)
- SNAP12 12-channel Optical Receiver (4.8 Gbps)
- Flexible clock network with 6 clock sources.
- Jitter-attenuating Si5319 any-rate clock multiplier/synthesizer
  - Internal or external 40 MHz frequency reference clock
  - Generates 320 MHz GTX reference clocks

MiniCTR2 Architecture



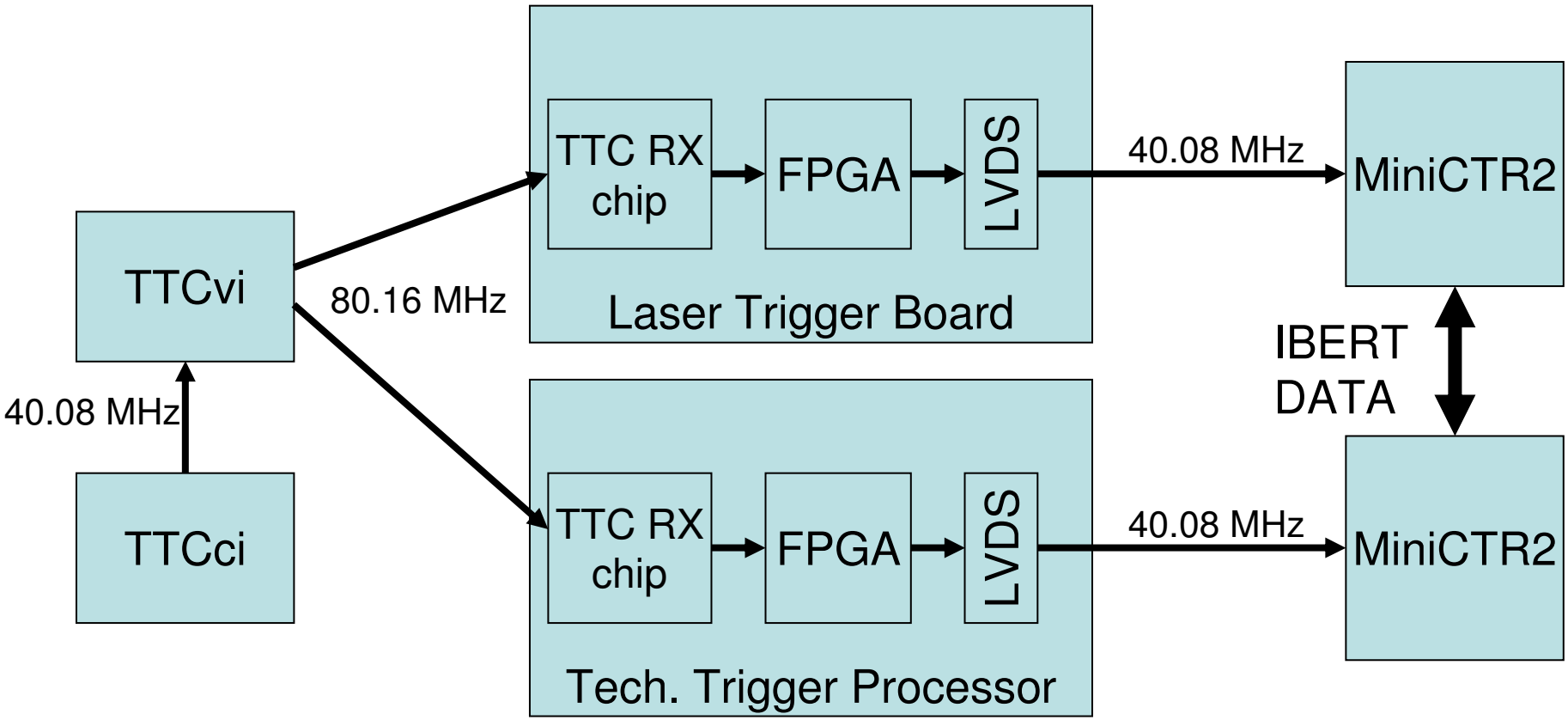
MiniCTR2 Printed Circuit Board Stackup

- 10 Copper Layers
- 5 mil lines, 4 mil spaces
- Top and bottom layer (stripline) 6 mil traces support 6.4 Gbps

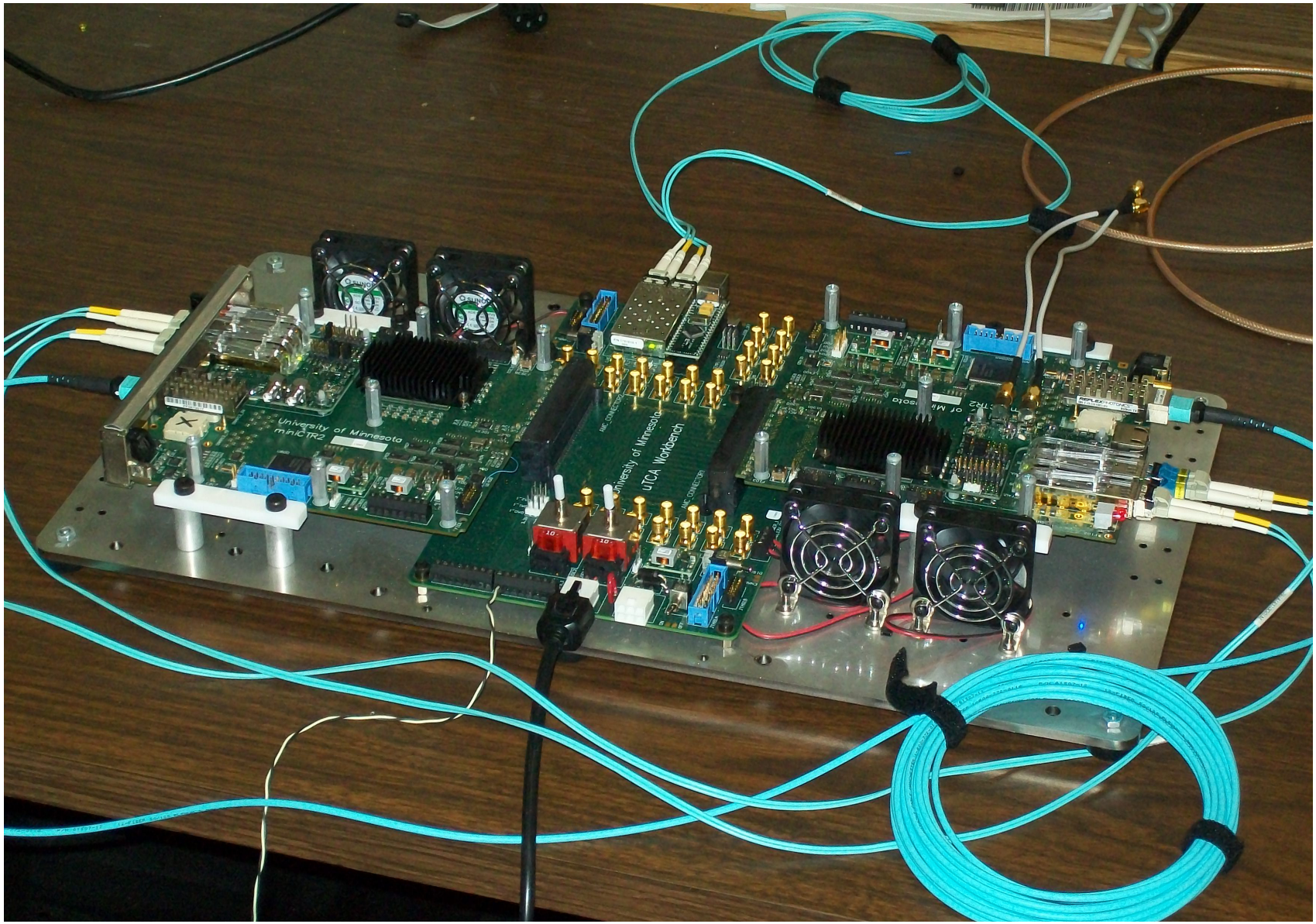
Bit Error Rate Test (BERT)

Bit Error Rate Test

- Board to Board communication via 850nm optics, multimode fiber
- Xilinx IBERT FPGA core
  - PRBS-31 data pattern (length 2^{31}-1)
  - 4.8 Gbps on SNAP12 (4 channels)
  - 6.4 Gbps on SFP+ (2 channels)
- Two different legs of a realistic (somewhat pessimistic) clock distribution example.



Bit Error Rate Test



MicroTCA Workbench – Board to Board Communication

Bit Error Rate Test

Silicon Laboratories Si5319

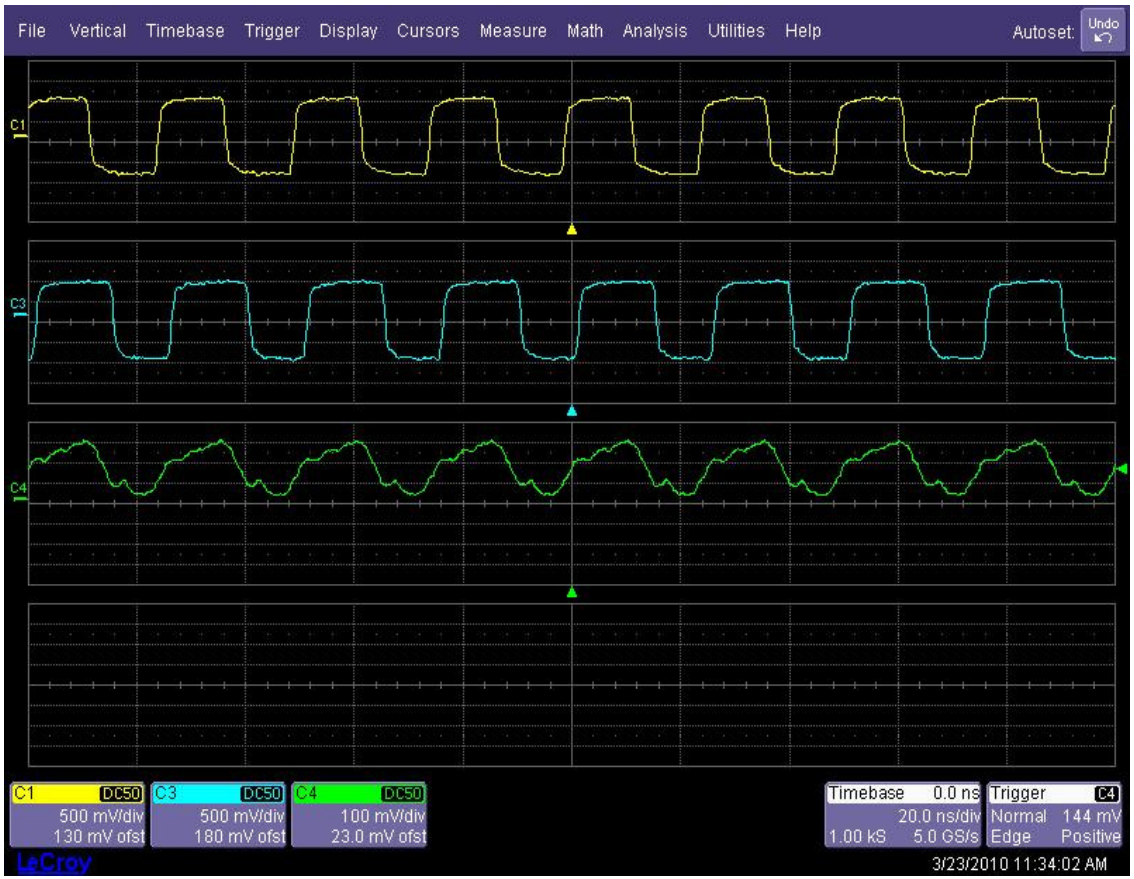
Locks on to external reference clock frequency.

Output clock phase is not specified.

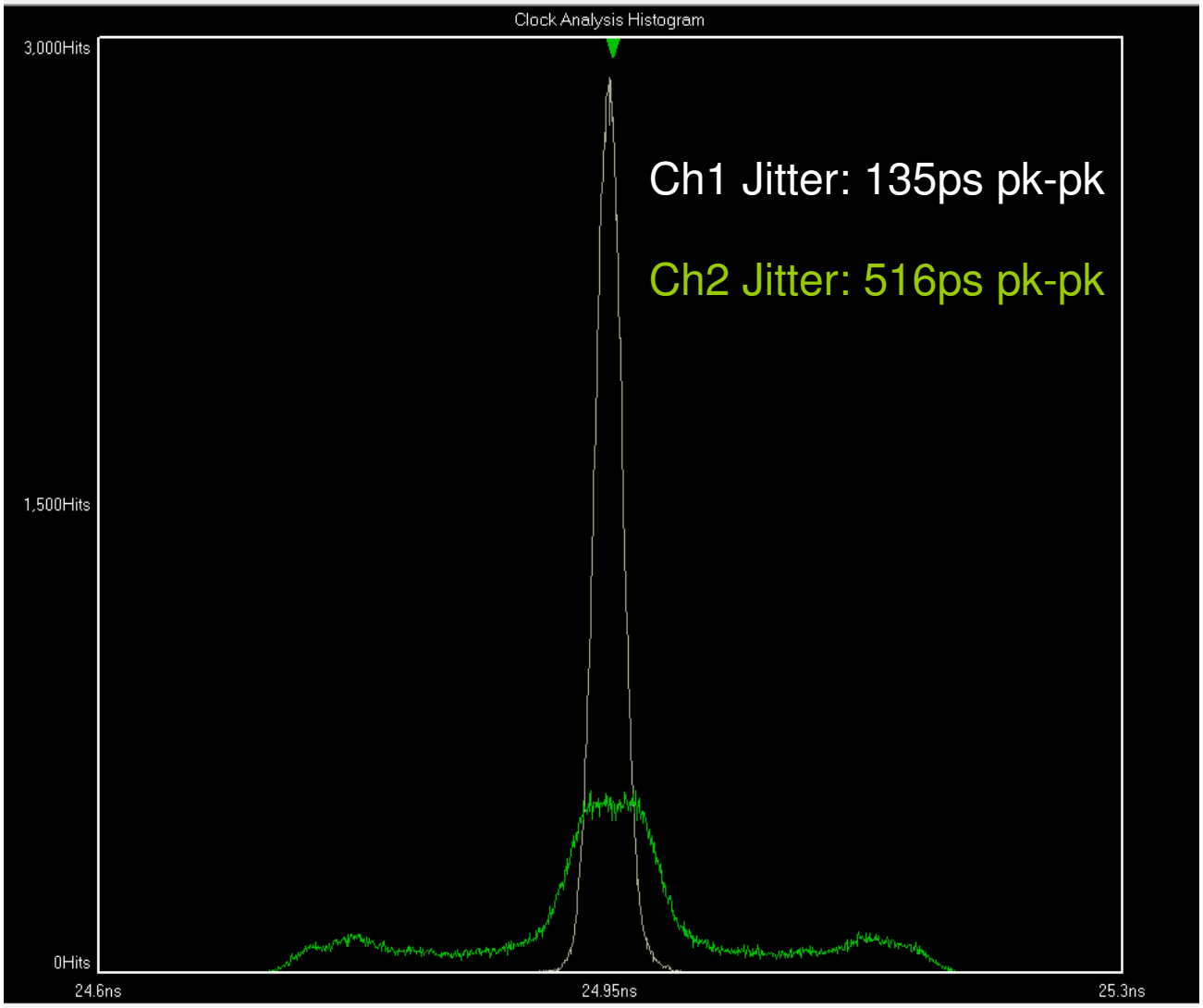
Output from Si5319 (divided by 8)

Input to Si5319

40.08 MHz Ref. Clock



Bit Error Rate Test

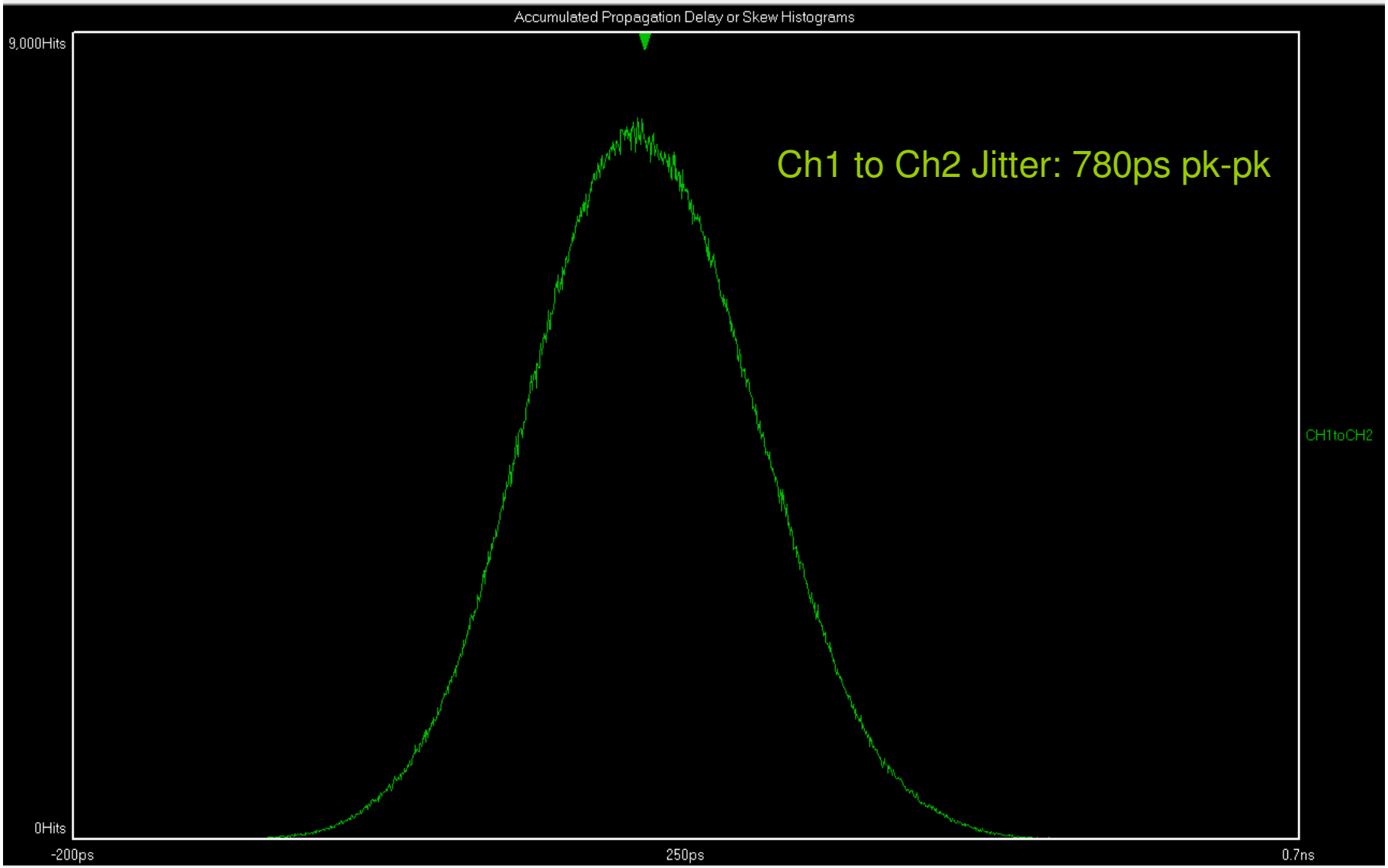


Clock Period Histograms for both 40.08 MHz clock distribution branches.

Measured using a Wavecrest SIA-4000

(Thanks to Brad Hegge, Gigamax Technologies, www.gigamaxtech.com)

Bit Error Rate Test

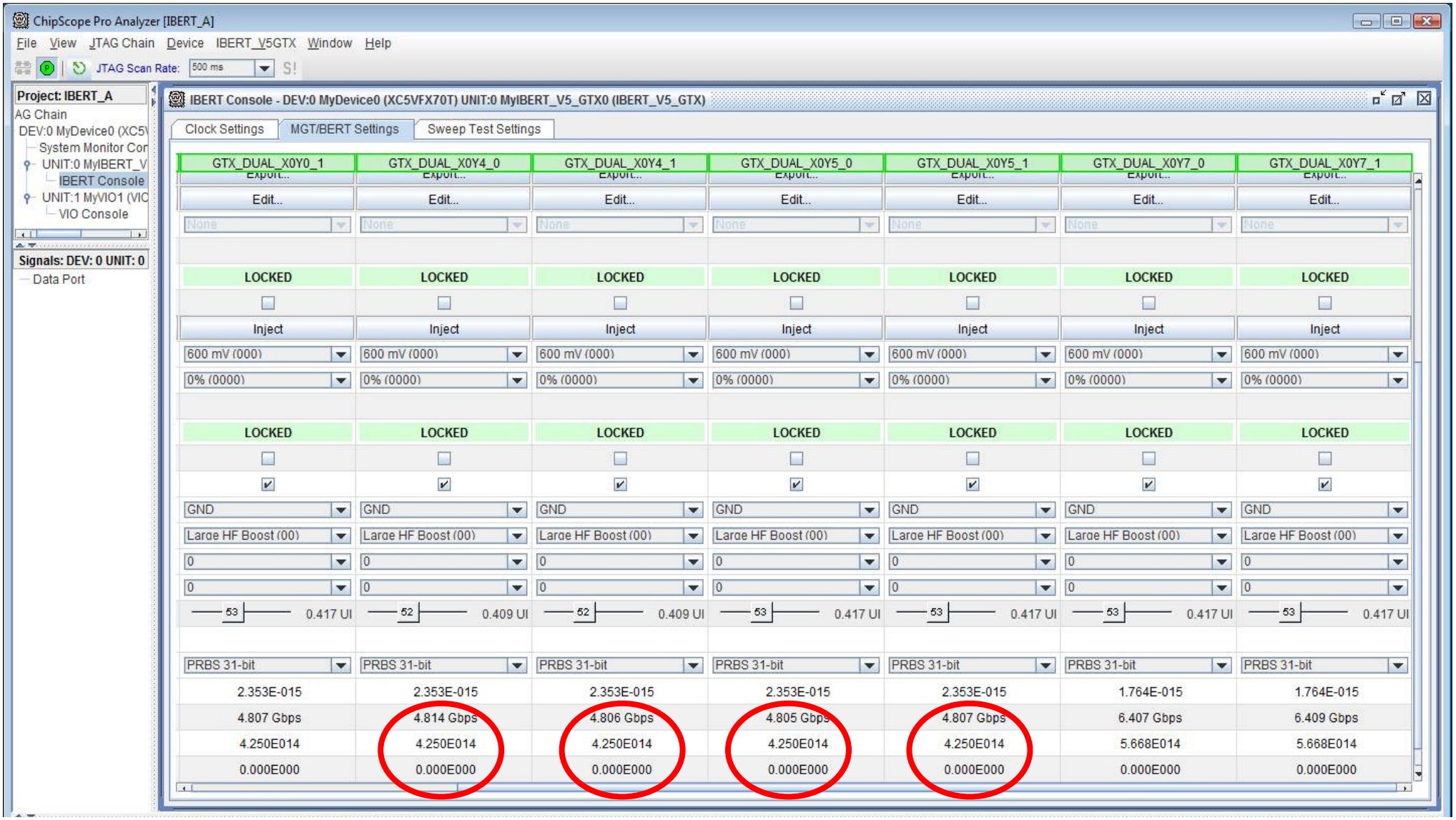


Clock Period Difference Histogram (Ch1 to Ch2)

Measured using a Wavecrest SIA-4000

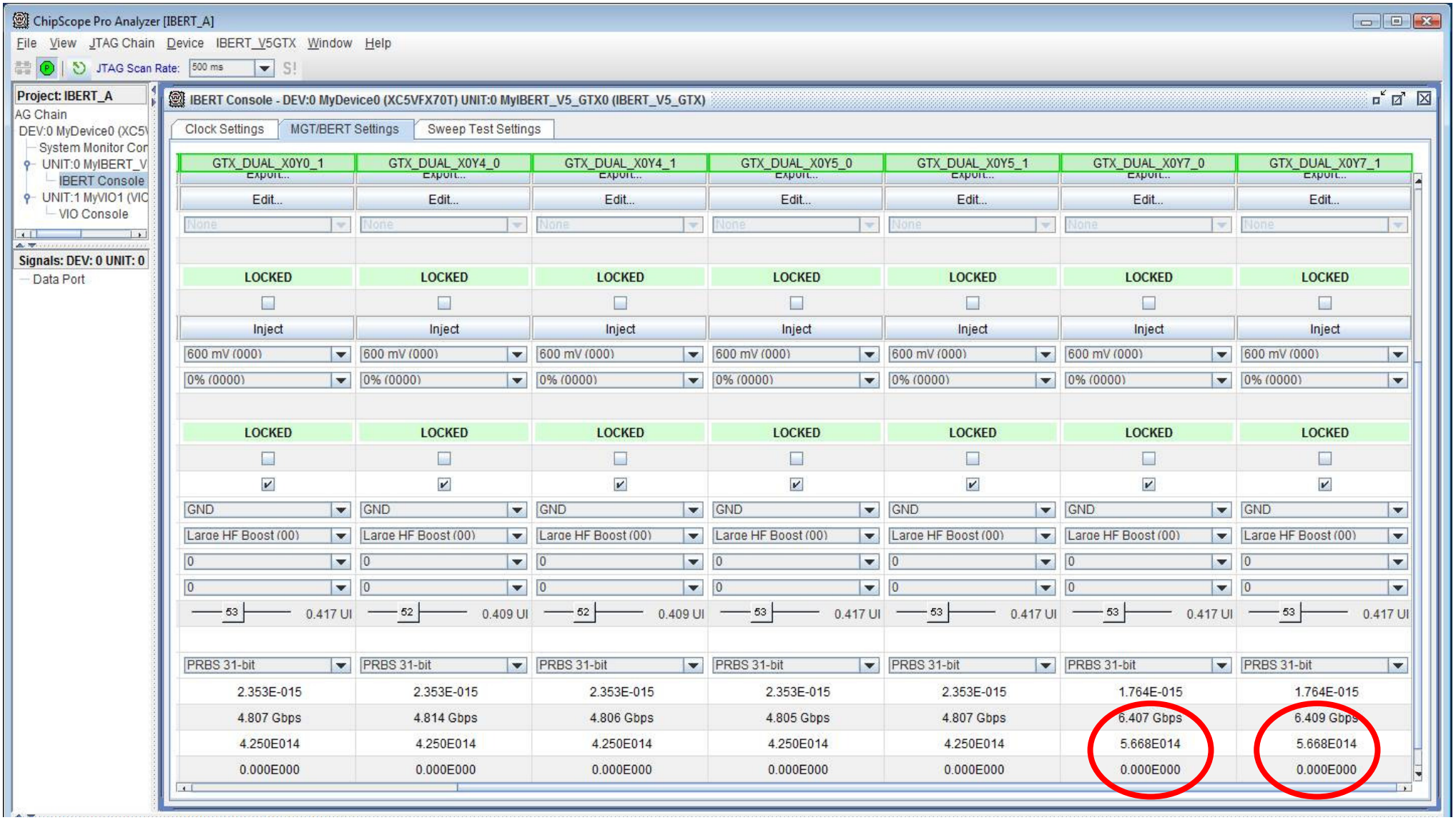
(Thanks to Brad Hegge, Gigamax Technologies, www.gigamaxtech.com)

Bit Error Rate Test



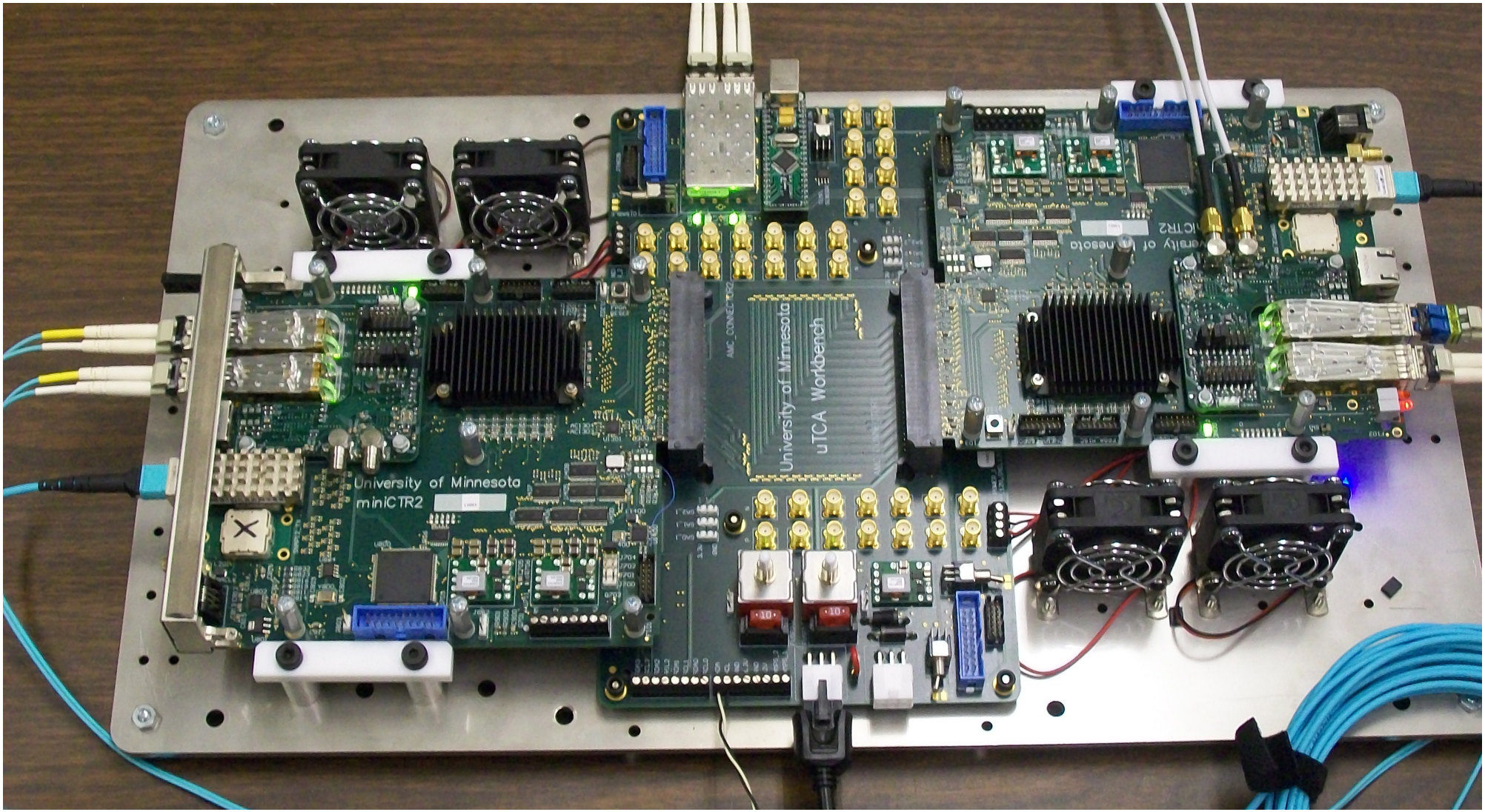
All 4 SNAP12 channels ran for more than 24 hours without a single error at 4.8 Gbps.

Bit Error Rate Test



Both SFP+ channels ran for more than 24 hours without a single error at 6.4 Gbps.

Bit Error Rate Test

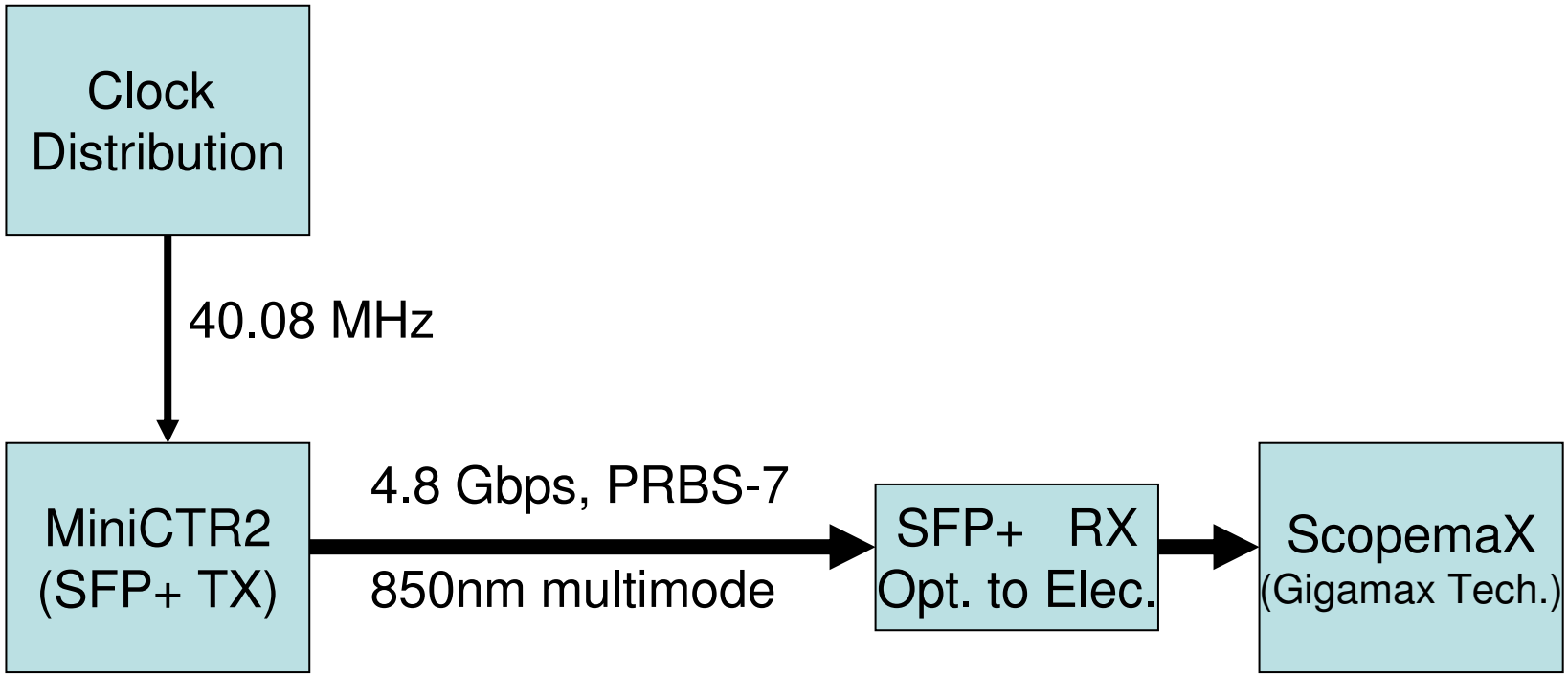


The communication from board to board over the short MicroTCA backplane was also error free even at speeds above 6 Gbps. (Note that FPGA is not rated above 4.25 Gbps.)

The signal path includes two Molex RA MicroTCA connectors and about 7 inches of FR4 on the backplane.

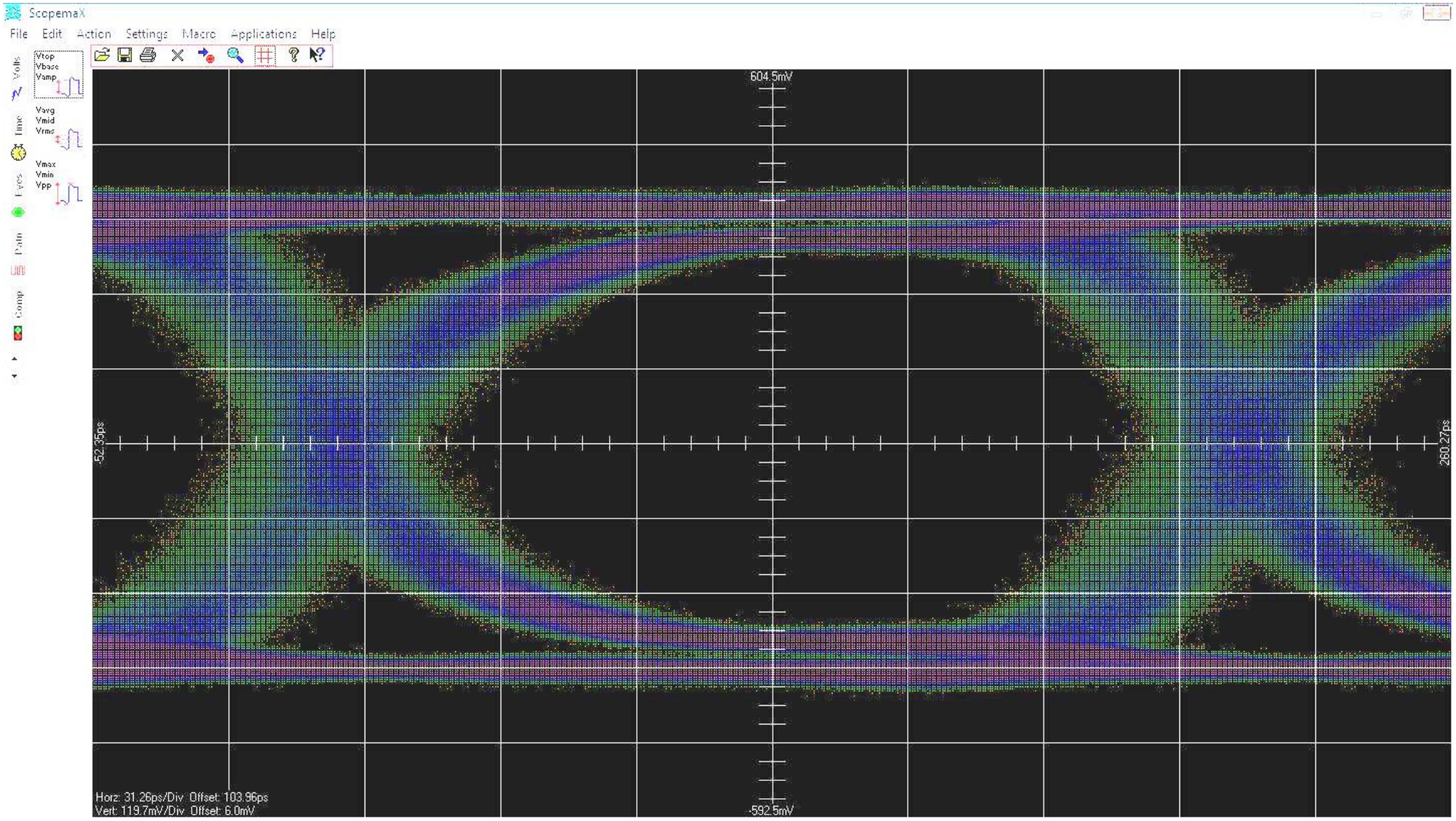
4.8 Gbps Serial Data Integrity Analysis

Data Integrity Analysis



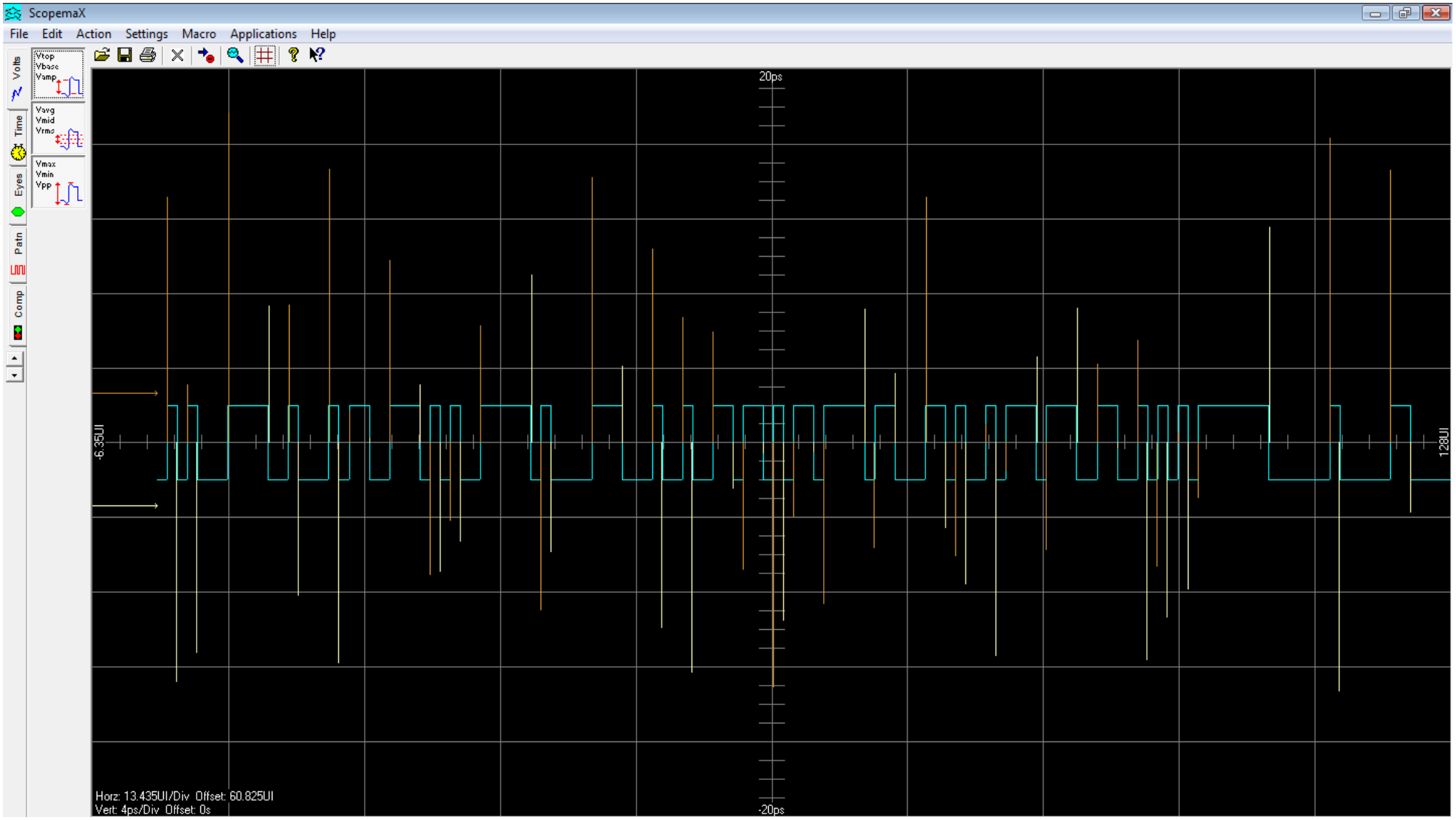
4.8 Gbps Serial Data Integrity Analysis
Measured using a ScopemaX from Gigamax Technology
(Thanks to Brad Hegge, Gigamax Technology, www.gigamaxtech.com)

Data Integrity Analysis



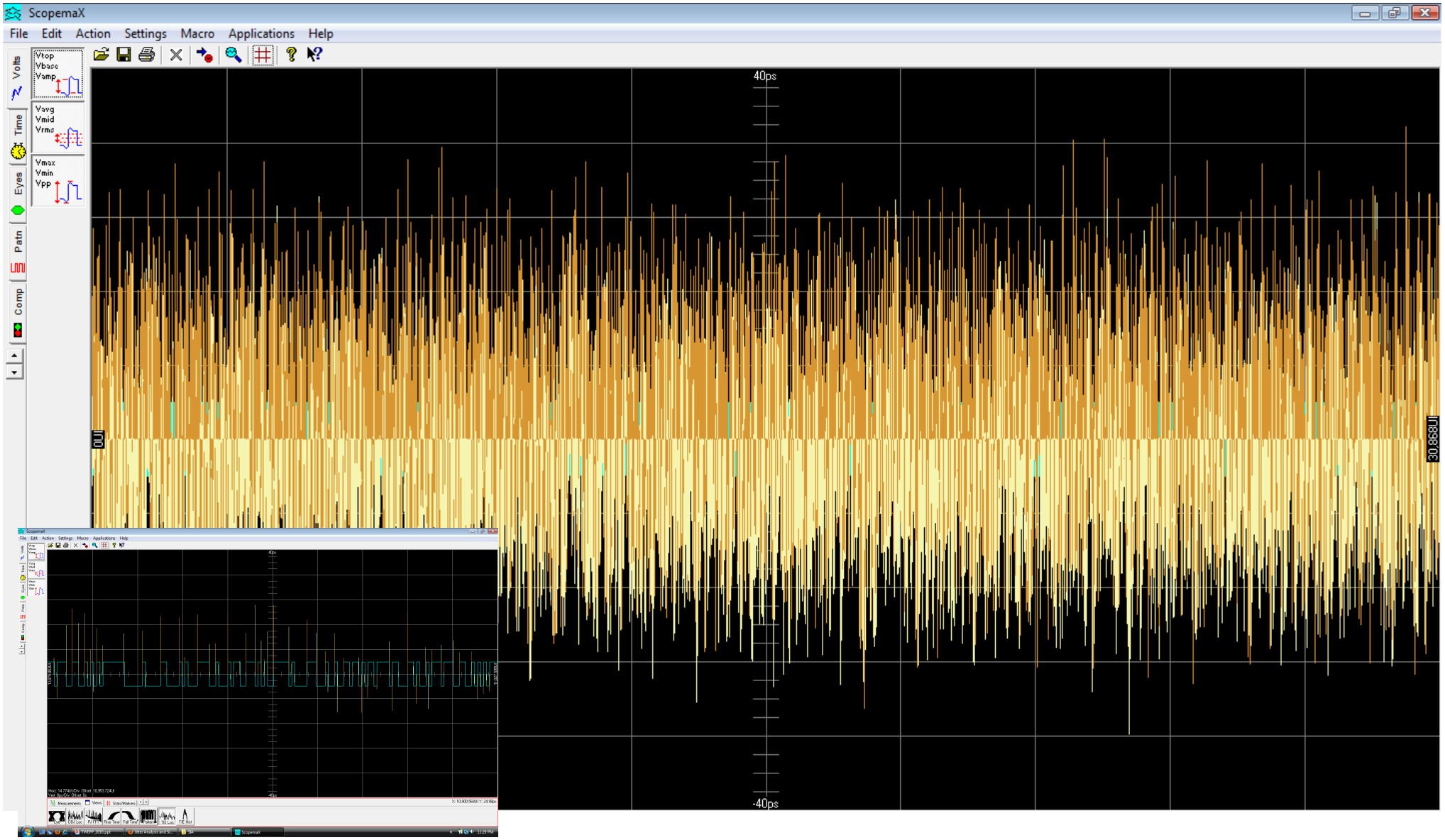
PRBS-7 Eye Diagram at 4.8 Gbps

Data Integrity Analysis



PRBS-7 Data Dependent Jitter Diagram, 4.8 Gbps (208ps bit)
max error: 17.73ps, min error: -13.31ps, 31.04ps pk-pk
Not sensitive to choice of clock distribution branch.

Data Integrity Analysis



PRBS-7 Time Interval Error Diagram for 3086 bits, 4.8 Gbps (208ps bit)
max error: 36.27ps, min error: -31.88ps, 68.15ps pk-pk
Not sensitive to choice of clock distribution branch.

“IPbus” Control Concept

“IPbus” Control Concept

- “IPbus” is an R&D effort in CMS.
- Use Ethernet to control devices through the MicroTCA MCH Ethernet switch.
- Create a virtual A32/D32 bus in FPGA firmware.
- Perform READ, WRITE, RMW transactions on the bus.
- Package multiple bus transactions into a single Ethernet packet to minimize latency and maximize bandwidth.

“IPbus” Status

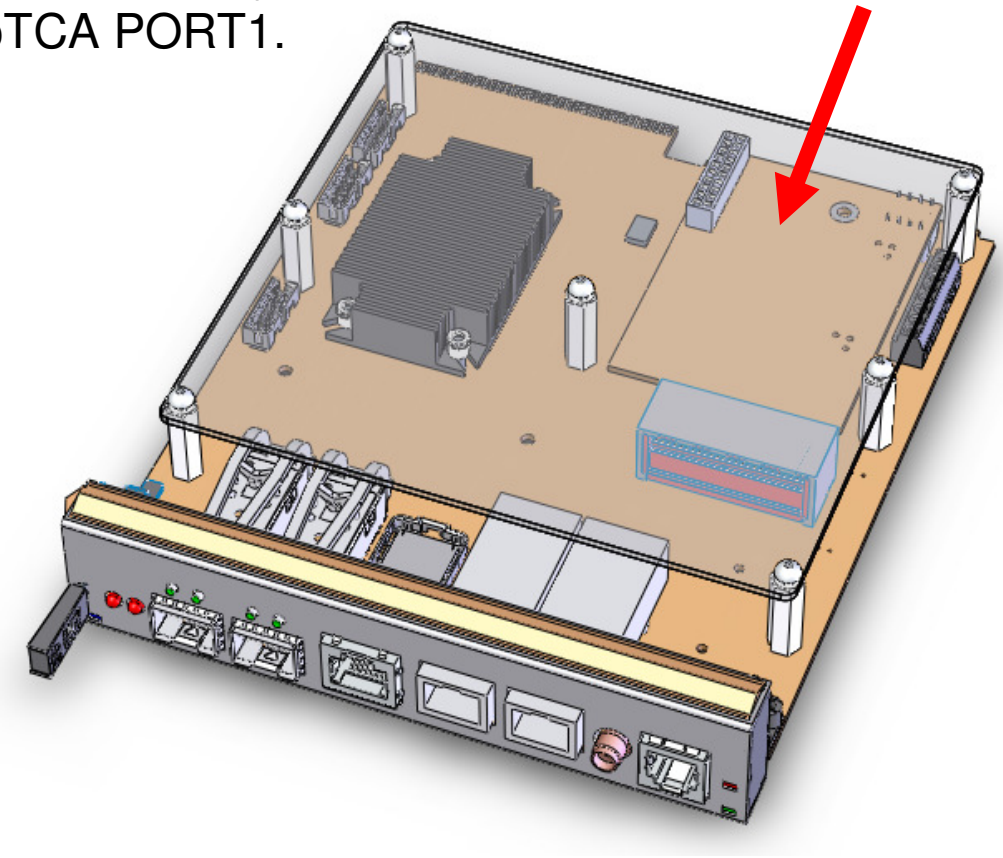
- Initial FPGA demonstration using UDP has been completed.
- Performance: Approximately 20 MBytes/s (block transfers)
- Size: Approximately 3% of XC5VFX70T (MiniCTR2)
- User protocol supports TCP but FPGA firmware does not support it yet.
- Successfully tested with the CMS-MCH (“DTC”) on a backplane.

Other Activities

MiniCTR2b

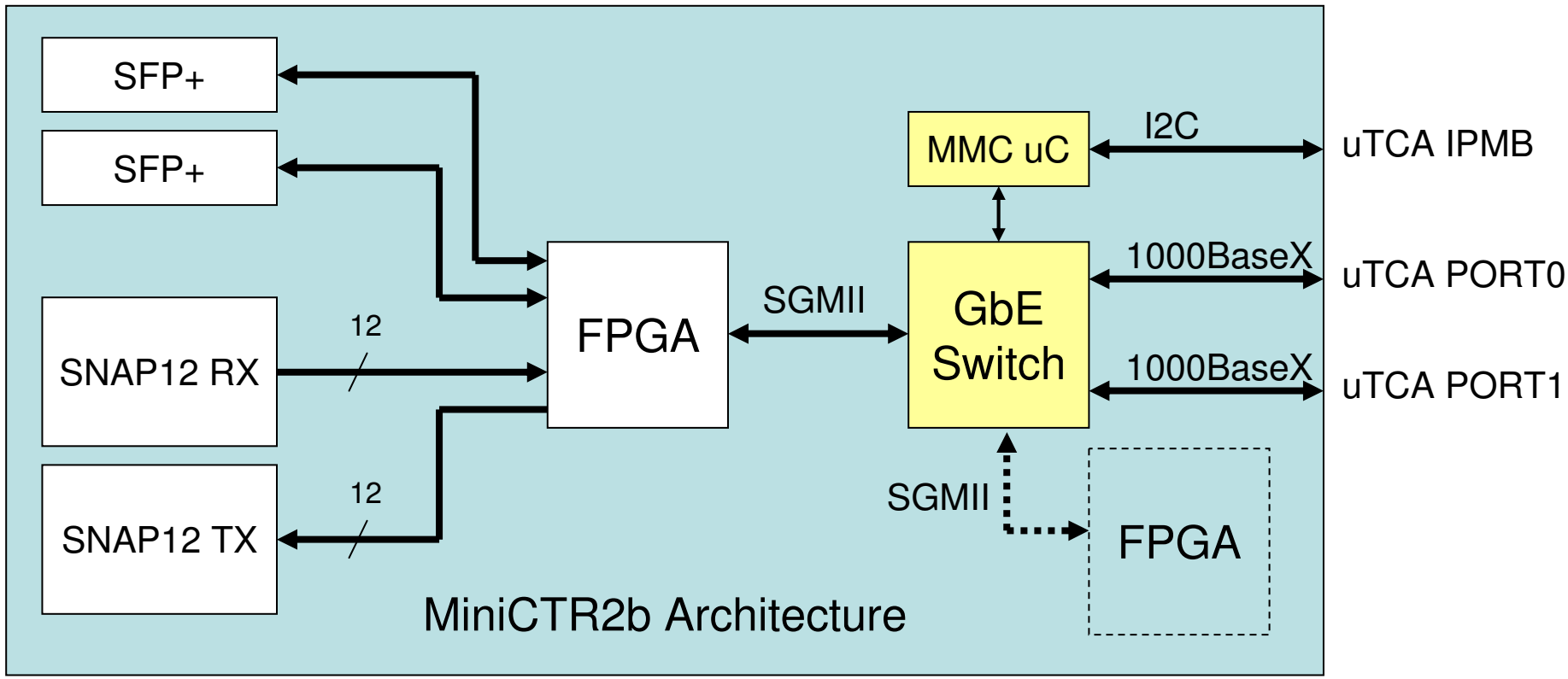
A modified MiniCTR2 board has been designed but not fabricated (yet).

- Better access to Si5319 clock input and output for jitter analysis.
- Microcontroller (MMC) has been moved to a mezzanine card.
- The mezzanine card can also support an Ethernet switch that will connect two SGMII (Gigabit Ethernet) from FPGAs to MicroTCA PORT0 and MicroTCA PORT1. (See next slide.)



- The mezzanine card can also support an Ethernet switch that will connect two SGMII (Gigabit Ethernet) from FPGAs to MicroTCA PORT0 and MicroTCA PORT1.

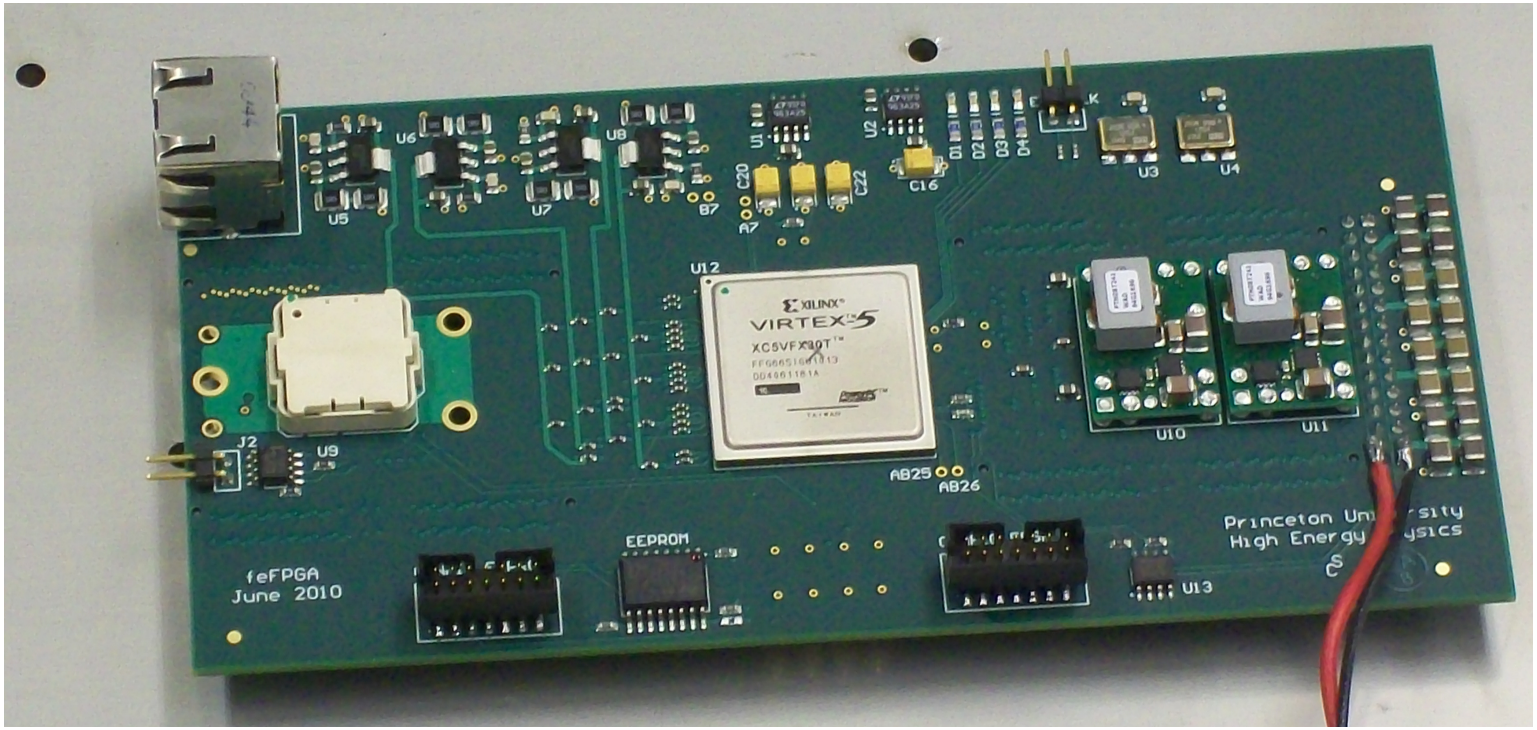
- Collaboration with University of Virginia.



Front End Prototype

Preliminary communication tests with a prototype Front End card are working in our lab at 4.8 Gbps on SNAP12 fiber links.

- Collaboration with Princeton University and Fermilab.



Princeton University / Fermilab Front End Prototype

Future Activities

Measure and Optimize System Latency

- Integration with Front End Prototype
- Integration with Trigger

Demonstration in Test Beam

- Integration with Front End Prototype
- Integration with DAQ