Readout Electronics for Low Dark Count Geiger Mode Avalanche Photodiodes Fabricated in Conventional HV-CMOS Technologies for Future Linear Colliders

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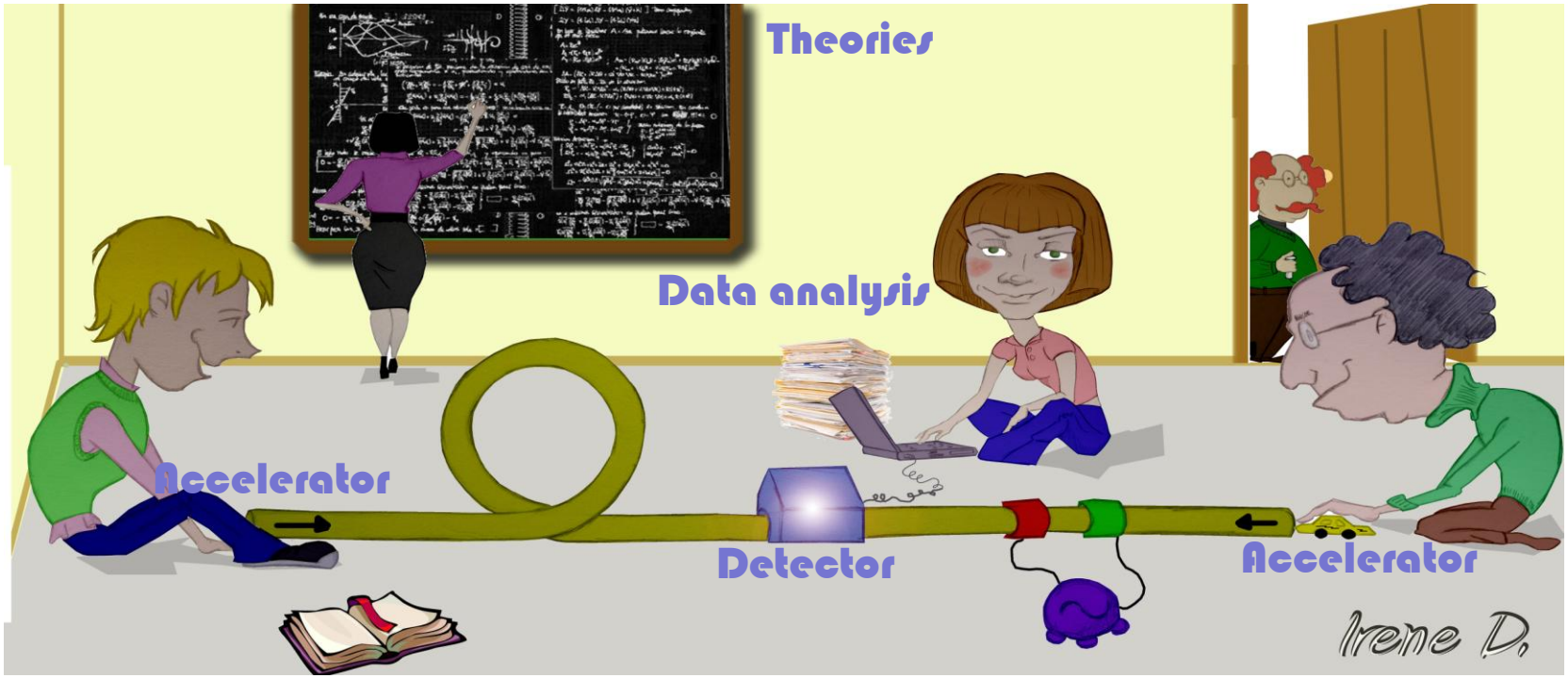
► Outline

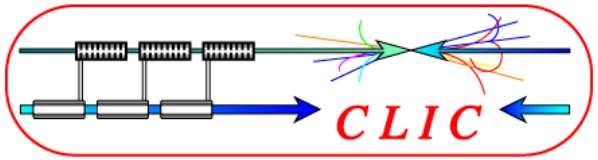
- Introduction
- Avalanche photodiodes in CMOS
- Technologies under comparison
- GAPDs and readout circuits for HEP experiments
  - Beam structure
  - Proposed readout circuits
  - Test and results
  - Comparison
- Conclusions

Motivation: Future colliders



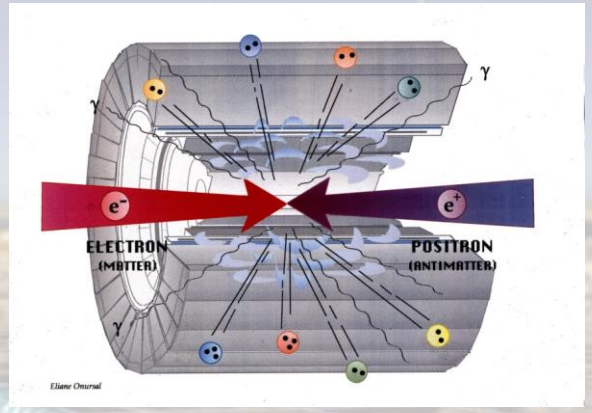
- ✓ Next collider will be a linear collider
- ✓ Still not clear whether a ~ 1TeV (ILC) or multi TeV (~3TeV) CLIC

ilc international linear collider

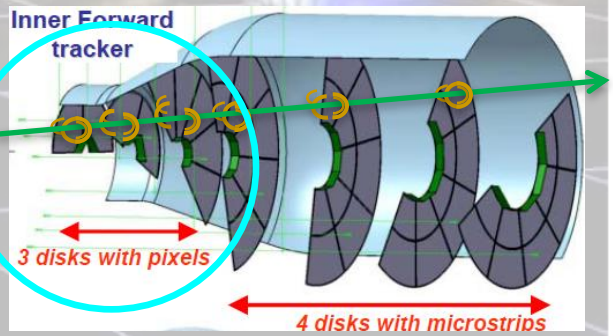


Detector requirements

- **Strict technology requirements posed by the ILD (International Large Detector) Concept Group (last version Feb. 2010)**
  - **Low material budget (0.2-0.5% X_0)**
    - To reduce errors from multiple scattering
  - **High spatial resolution**
    - Best achievable Φ resolution → 5μm
  - **Pixel size → 20μm x 100μm**
  - **Occupancy** (3rd layer of the FTD)
    - Background level → 0.001-0.002 hits/cm²/BX
  - **High readout speed**
    - BX ILC → 337 ns
    - BX CLIC → 0.5 ns
  - **Radiaton tolerance & EMIs tolerance**
  - **Minimum power dissipation** (no cooling)

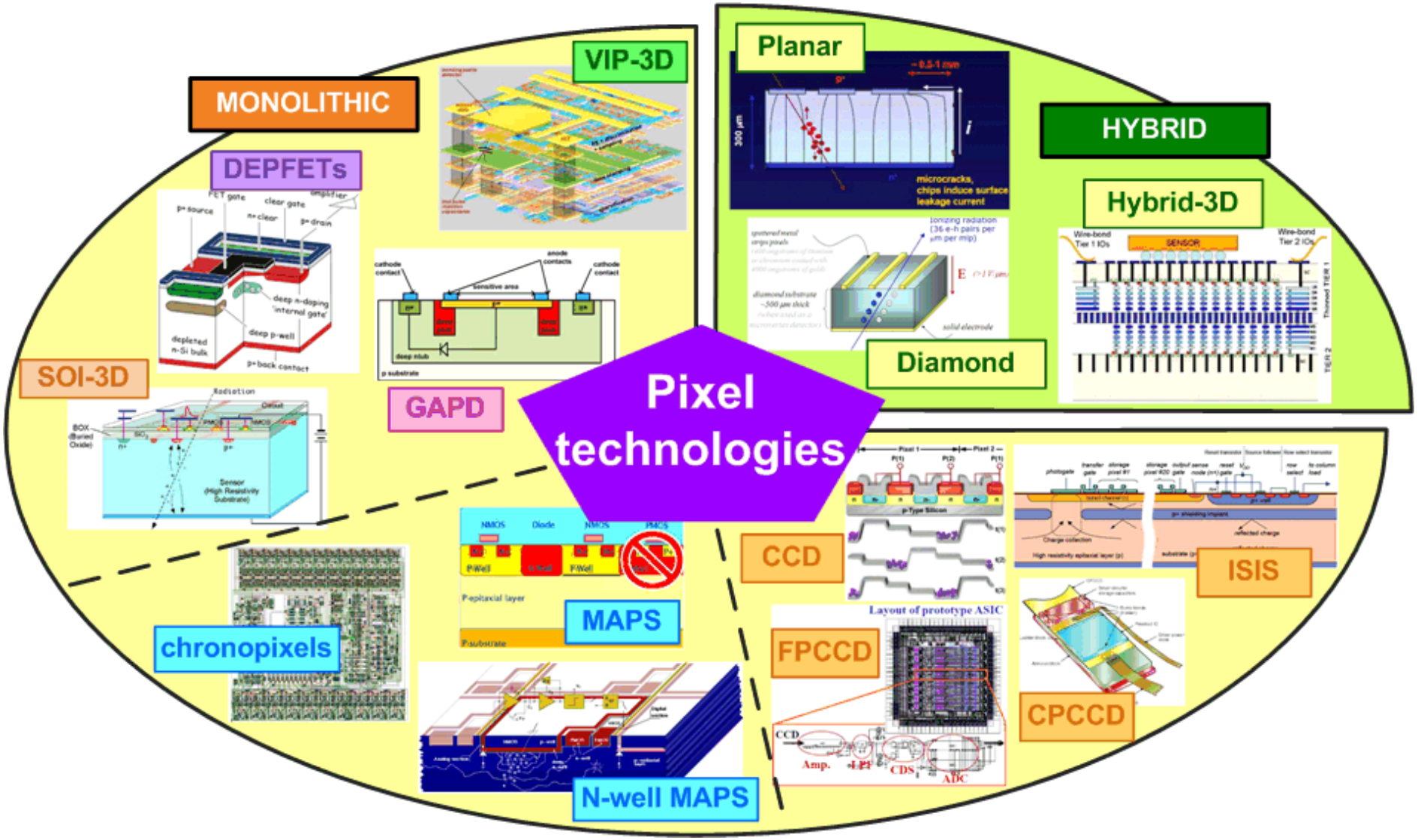


Vertex detector



Tracker detector

Pixel detectors



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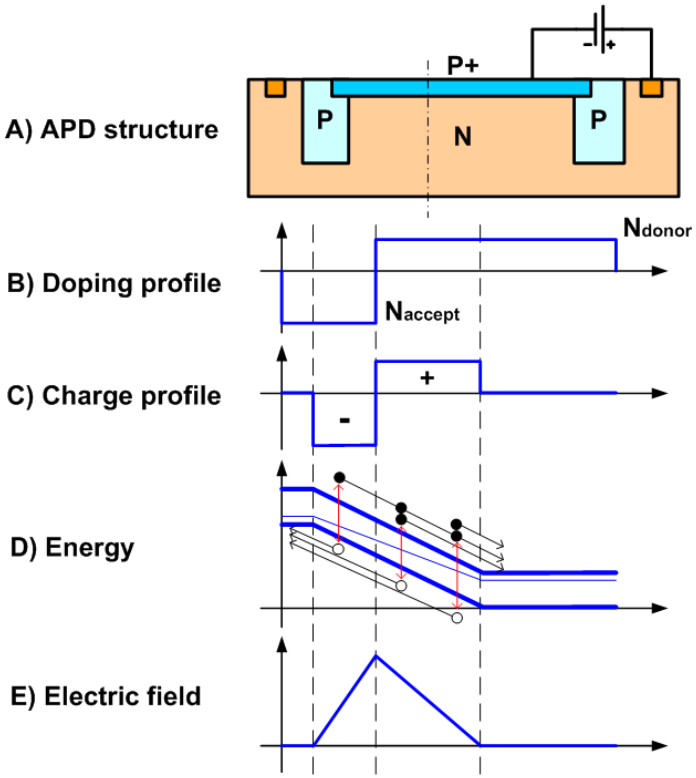
Universitat de Barcelona

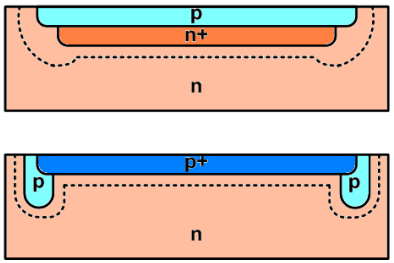
Avalanche photodiodes in CMOS (1)

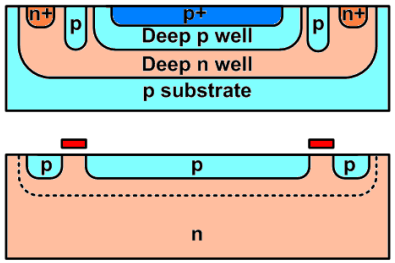
- **APD:** p-n Junction biased above breakdown. Arrival of a photon or a particle generates e-h pair, which initiates an avalanche in the planar multiplication region.
- **Premature edge breakdown** avoidance to assure the planar multiplication region:
  - Low doping profile in the corners
  - Avoid 90º angles → round corners or octogonal shape in the layout

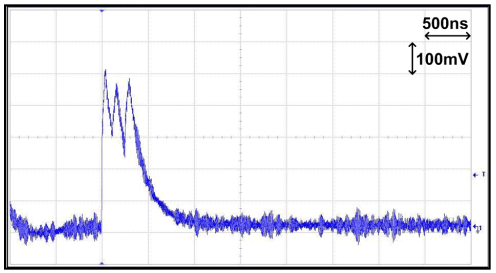
Main drawbacks:

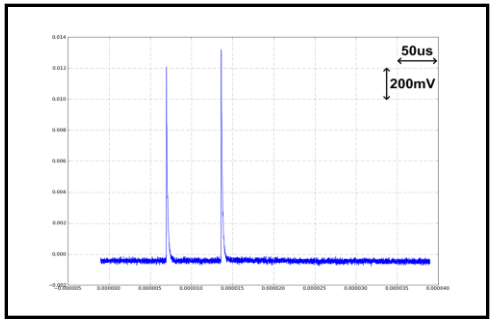
- **Dark count**: Spurious pulses generated in dark, due to thermal generation and carriers tunneling
- **Afterpulsing**: Pulse due to the release of a carrier trapped during a previous pulse. Depends on: Trapping probability, and lifetime of trapped charge







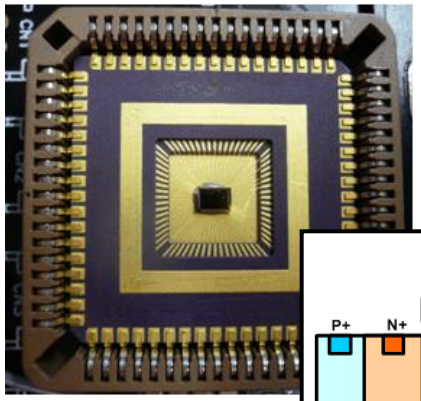




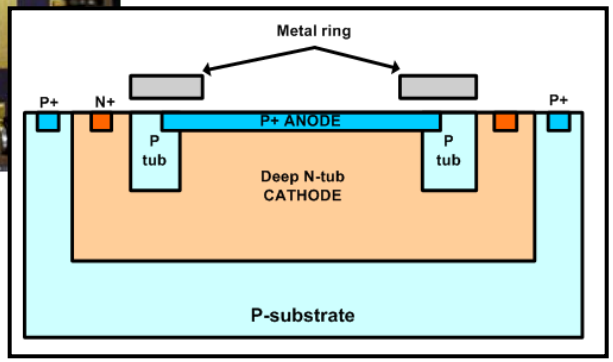
Avalanche photodiodes in CMOS (2)

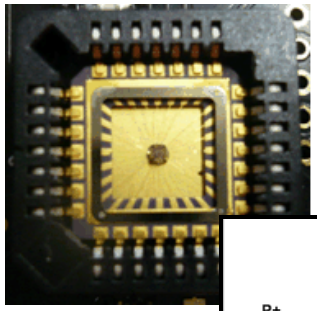
- **Motivation for Geiger-mode APDs**
  - ☑ A detector with high intrinsic gain (>10^8)
  - ☑ Excellent timing accuracy
    - ps rise time
    - short recovery times
    - possible single hit detection
  - ☑ Compatible with standard CMOS technologies
    - on-chip integration of readout circuits
    - low supply voltage requirements
    - reduced power consumption
- **However...**
  - ☒ High intrinsic level of noise (dark counts)
    - false counts
    - severe performance limitation
    - increase of the readout electronics area to store the false hits

Technologies under comparison

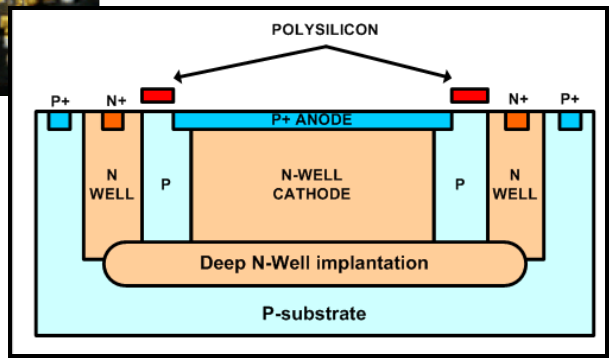


HV-AMS 0.35 µm





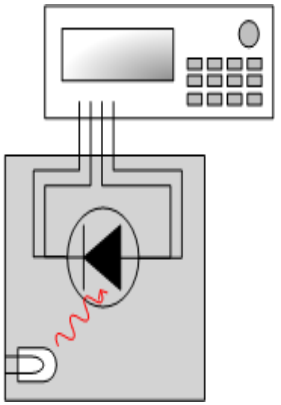
STM 0.13 µm



Technology	V_{bd} (V)	I_a (mA)	DC (KHz)
HV-AMS 0.35 µm	17.32	0.4	2
STM 0.13 µm	10.52	5	17.5

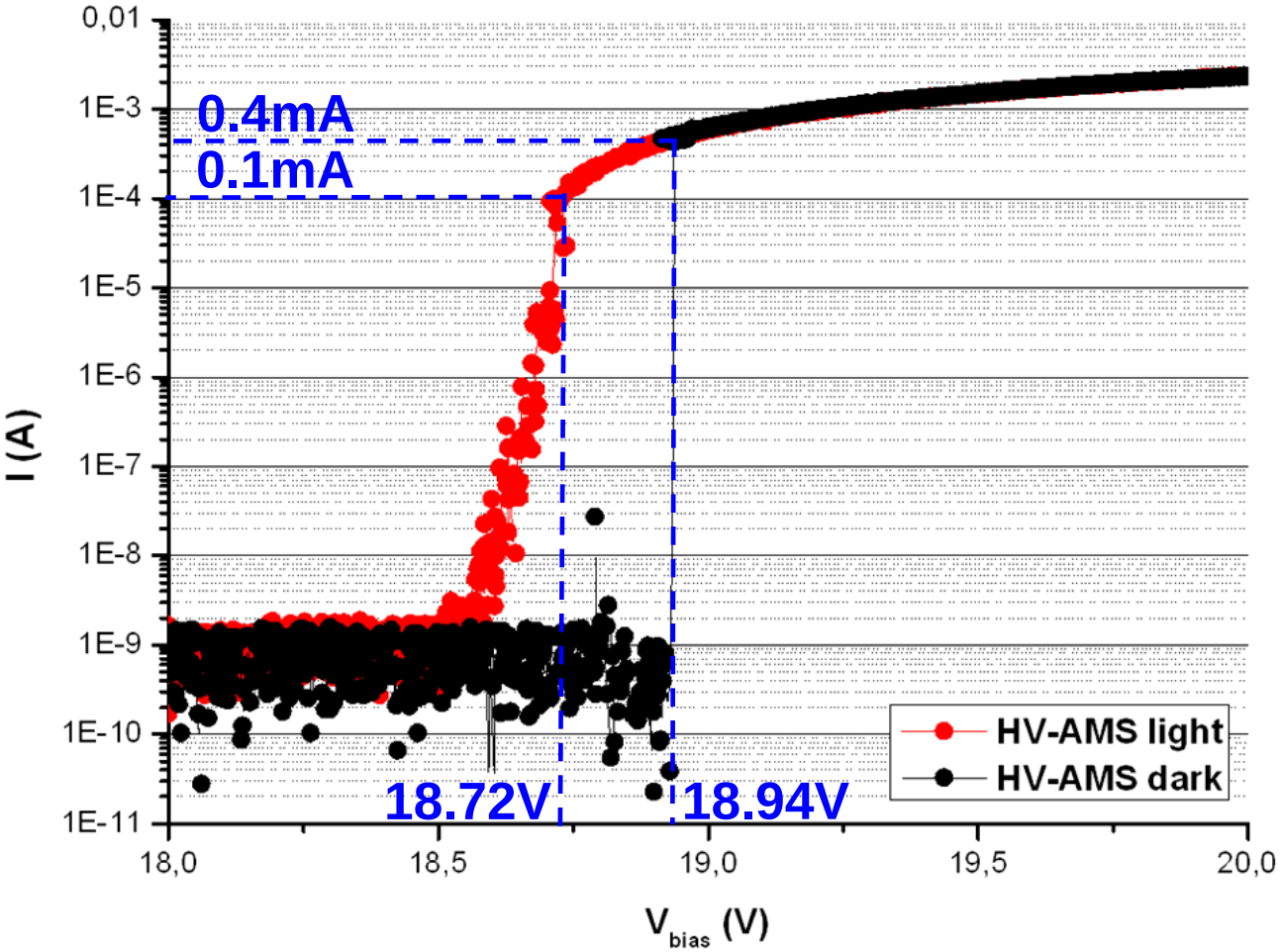
HV-AMS 0.35µm

Characterization: V_{BD} & linear mode

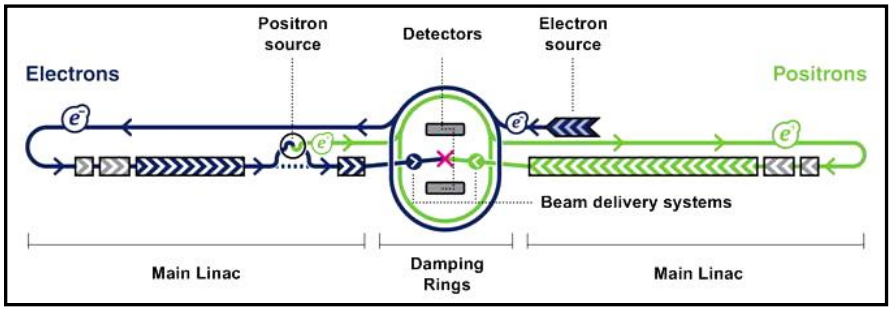


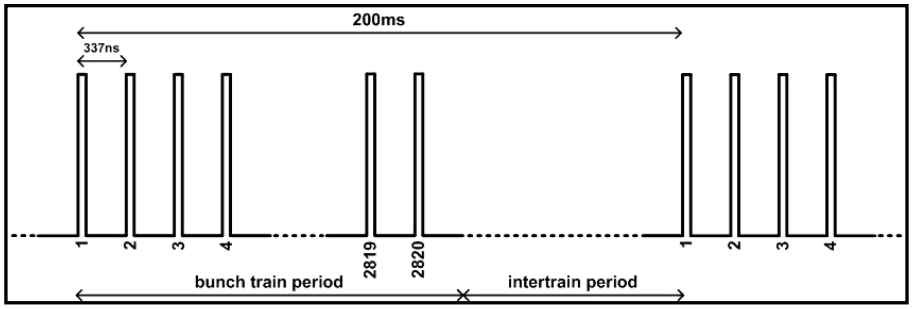
I(V)
measured with
a 4-wire method
with & without light

2010 APDs chip

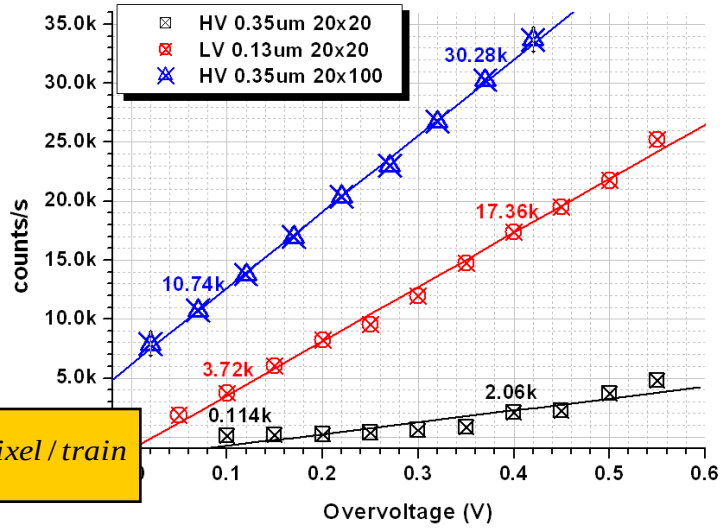


Beam structure





- **ILC timing**
  - 2820 BX in 0.95ms → acquisition phase
  - BX spacing of 337ns
  - 199.05ms quiet time → readout phase



- **ILC background**
  - 0.001-0.003 hits/cm ^{2}/BX for the 3rd layer of the FTD

$$\left(0.003\,hits/cm^2/BX\right)\cdot\frac{1cm^2}{\left(1\cdot10^4\,\mu m\right)^2}\cdot\frac{20\,\mu m x 100\,\mu m}{pixel}\cdot\frac{2820\,BX}{train}=1.69\cdot10^{-16}\,hits/\,pixel/train$$

- **0.35µm HV-AMS CMOS DC noise in ILC**
  - 38kHz/pixel (20µm x 100µm @ 18.28V)

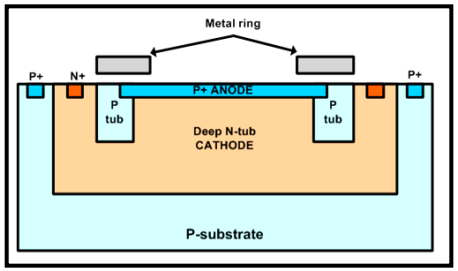
$$D.C._{EFFECTIVE}=\frac{38kHz}{pixel}\cdot10ns\cdot\frac{2820\,BX}{train}=1\ false\ hits/\,pixel/train$$

Gated acquisition

Readout circuits. V_{bias} generation.

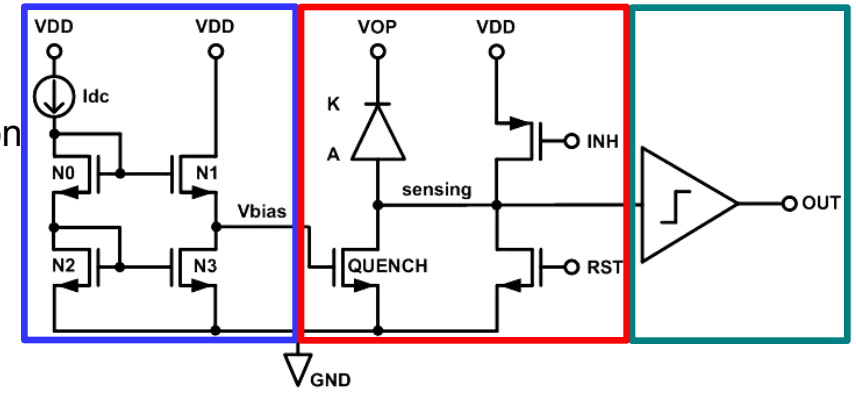
- **V_{bias} generation**
  - Current source → control of $\Delta V_{sensing}$ during the 'off' period thanks to I_{DC} → $\Delta V_{sensing} = (\tau_{OFF}/C)\cdot I_{DC}$
  - Traps emptied before the new 'on' period → afterpulsing probability ↓

- **Passive quenching/recharge**
  - **QUENCH** Active load → pMOS or nMOS topology?
    - nMOS topology allows fully isolation between the deep ntub/p-substrate and the sensing node → reduction of the total capacitance → response time ↓
    - nMOS transistor with $(W/L)_n$ = (0.8µm/5µm)
    - $I_D < I_{GAPD}$ latching current → correct quenching
  - **INH** Gate command through pMOS transistor.
    - INH = '1' → 'on' period → free running
    - INH = '0' → 'off' period → no particle detection
  - **RST** GAPD recharge through nMOS transistor.
    - RST = '1' → V_{OP} is restored (1ns)



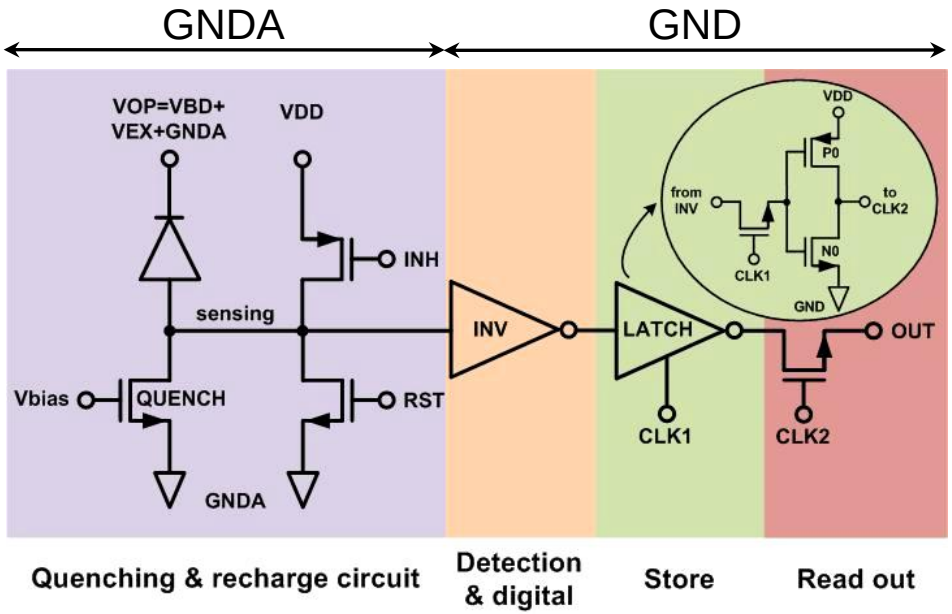
V_{bias} generation | Passive Q/R | L.O. readout

$V_{OP} = V_{BD} + V_{EX}$



- **L.O. readout...**
  - but V_{Th} of MOS transistors **(V_{Thp}=0.65V, V_{Thn}=0.5V)** makes avalanche detection difficult...

Readout circuits. 2 grounds scheme.

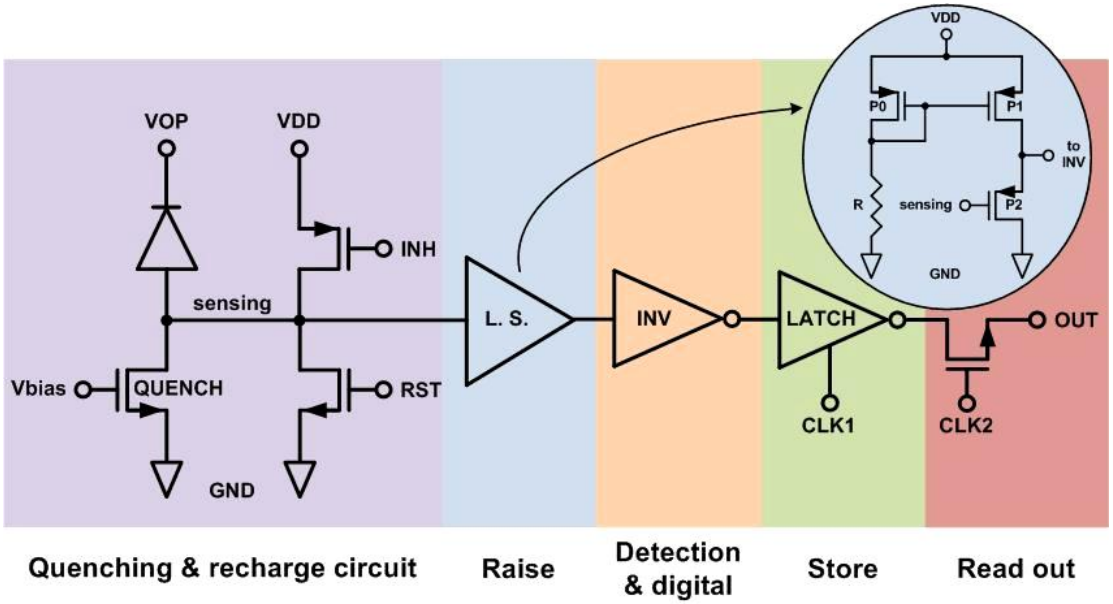


- **Main features:**
  - 2nd ground (GNDA > GND) to enable low V_{EX} operation
  - Minimum area latch to store the resulting value of the 'on' period
  - Readout with external control (CLK2 pass gate)

Gated acquisition	CLK1	INH
'on' period	'1'	'1'
'off' period	'0'	'0'
Reset → RST = '1'		
Readout → CLK2 = '1'		

- **Upon particle hit (or D.C):**
  - An avalanche fires
  - $V_{sensing}$ increases from GNDA → GNDA+V_{EX}
  - If GNDA+V_{EX} > V_{th} inverter → **the avalanche is detected**

Readout circuits. Level shifter.

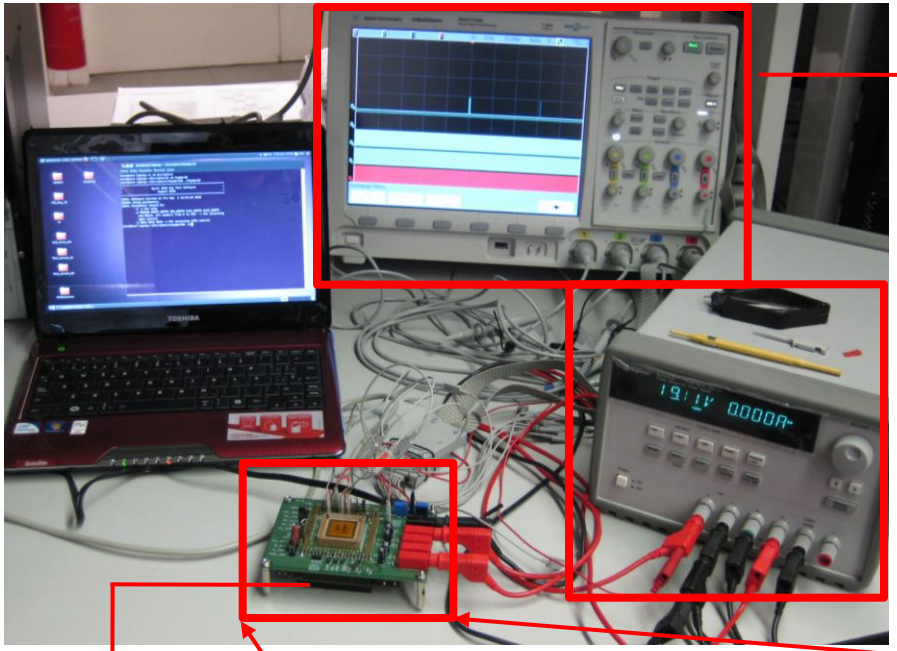


- **Main features:**
- L.S. with external resistor
- Minimum area latch to store the resulting value of the 'on' period
- Readout with external control (CLK2 pass gate)

Gated acquisition	CLK1	INH
'on' period	'1'	'1'
'off' period	'0'	'0'
Reset → RST = '1'		
Readout → CLK2 = '1'		

- **Upon particle hit (or D.C):**
- An avalanche fires
- $V_{sensing}$ increases from GND → V_{EX}
- L.S. raises V_{EX} to $V_{EX} > V_{th}$ inverter (1.65V) → **the avalanche is detected**

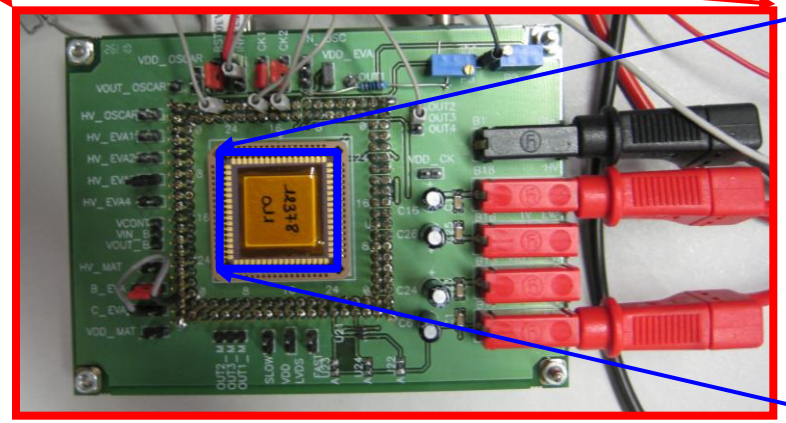
Test. Set-up.



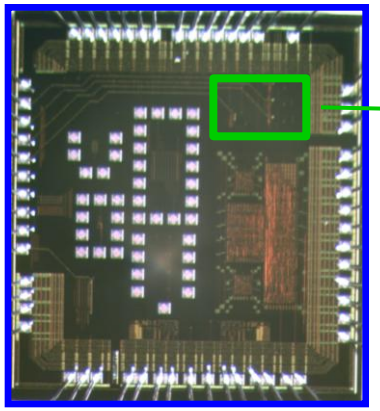
Scope
(Agilent MS07104A)

Voltage source
(Agilent E3631A)

FPGA
(control signals)

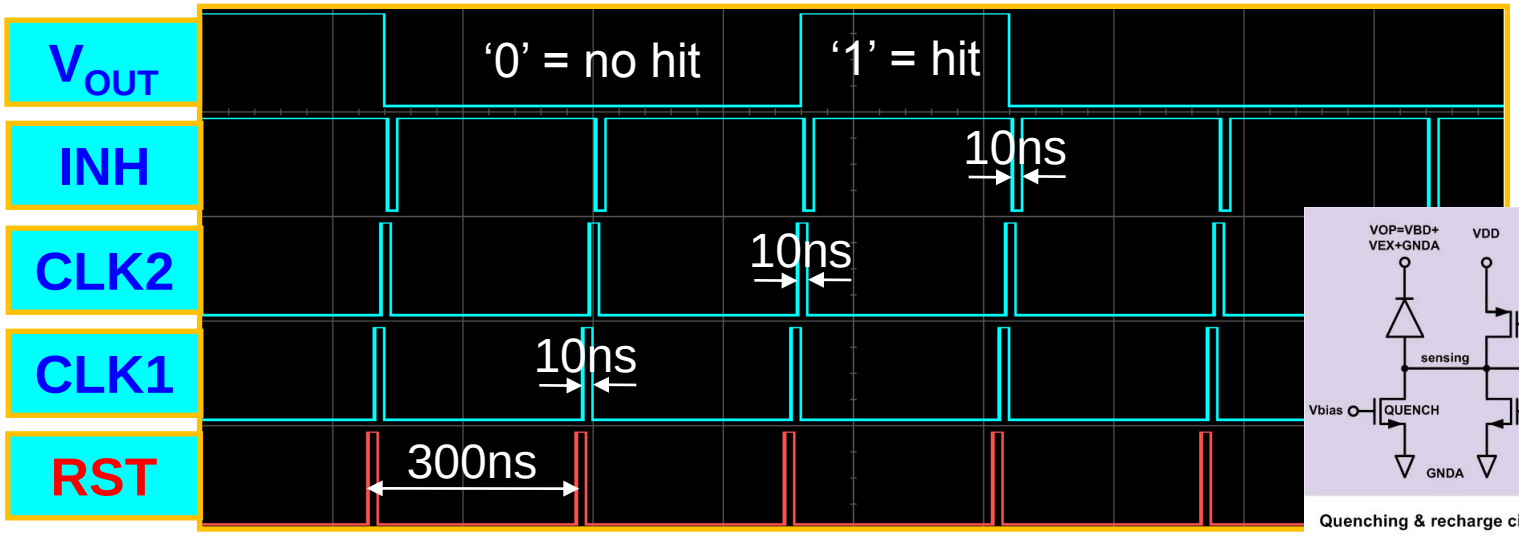


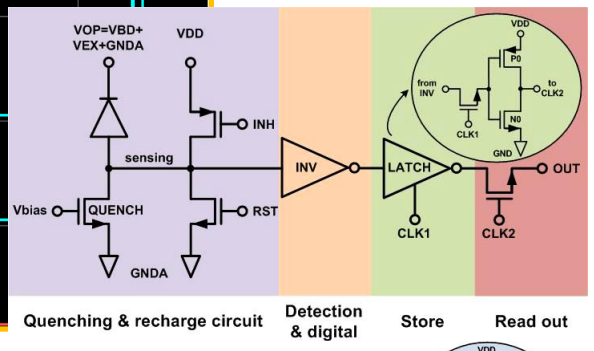
HV-AMS 0.35 µm

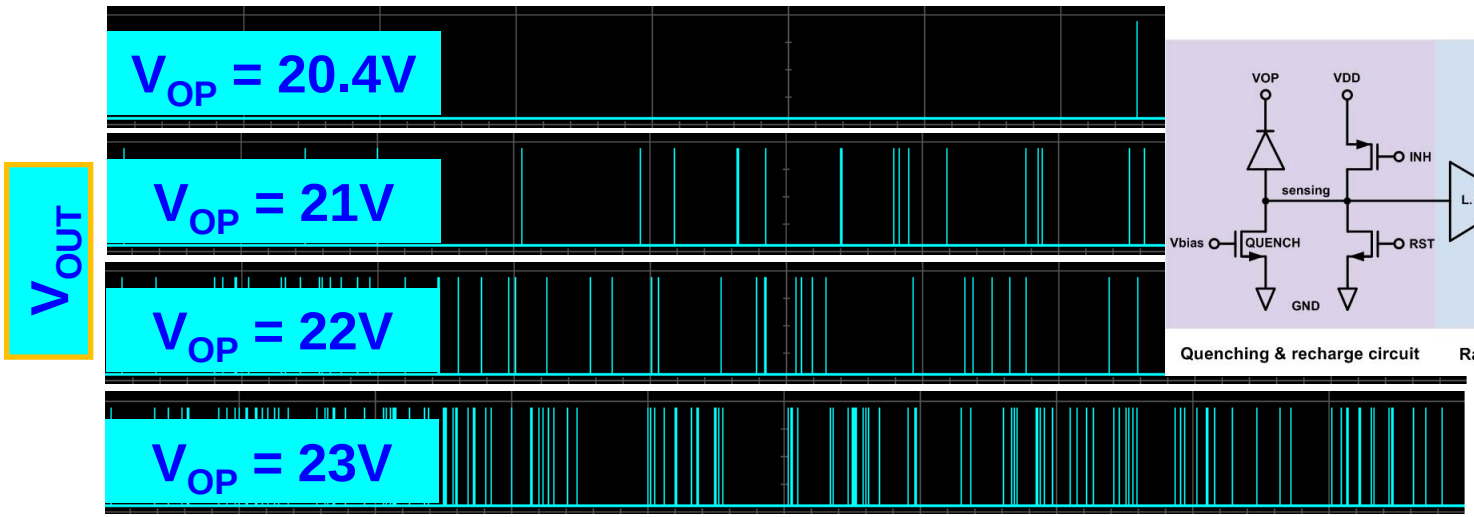


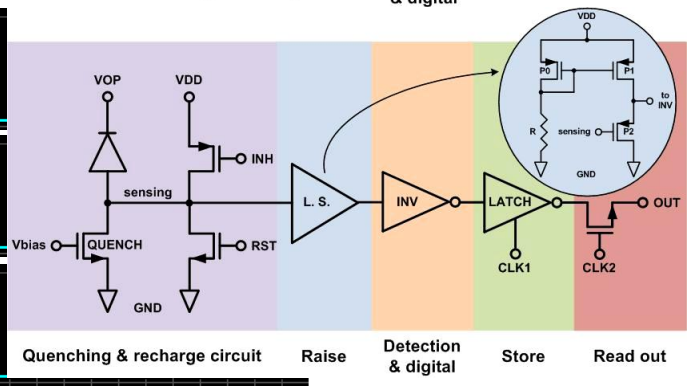
Pixels

Test. Results.



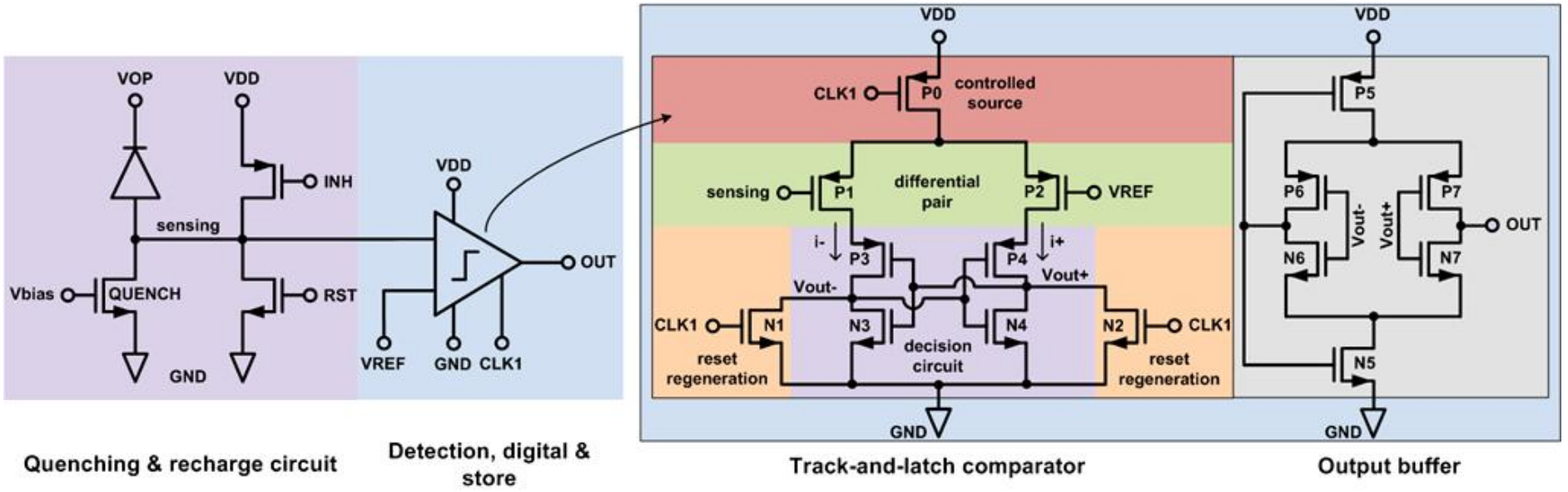




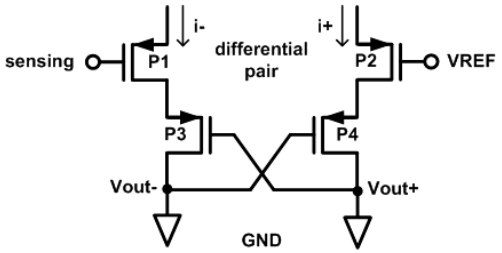


Δt = 1ms

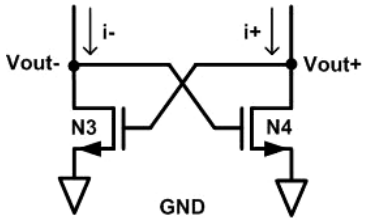
Readout circuits. Track-and-latch comparator.



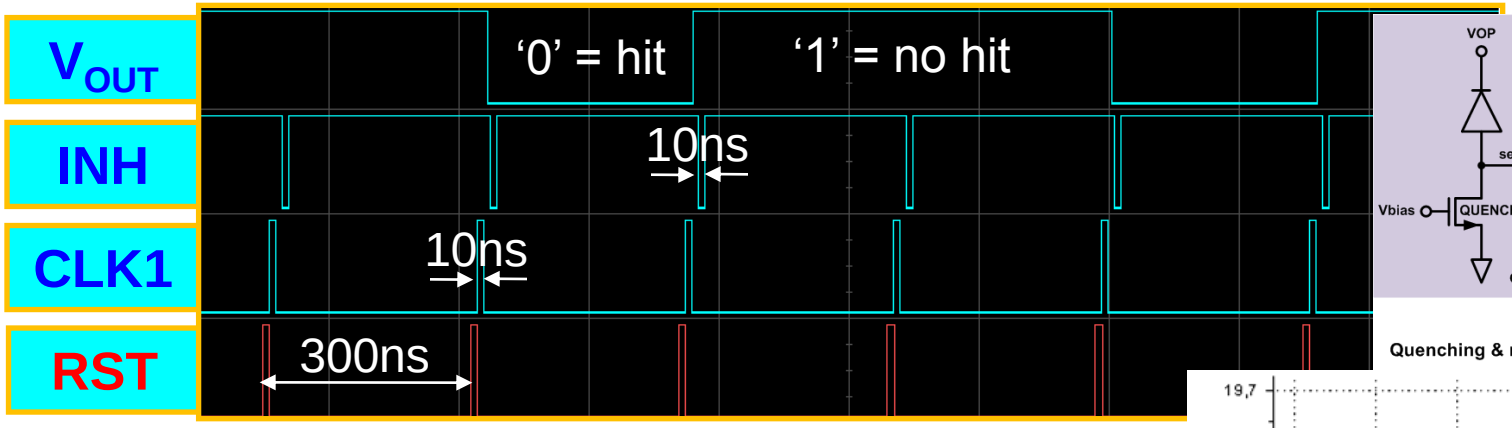
- **CLK1 = '1'** → **Track phase**
- Differential pair is sampling
- V_{out+}, V_{out-} = '0' → **OUT = '1'**

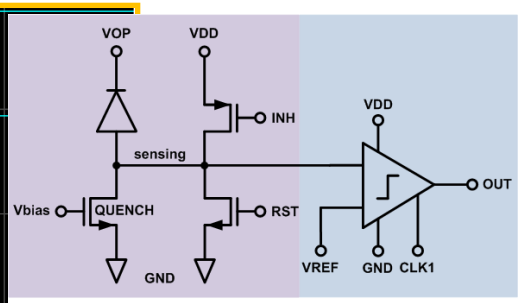


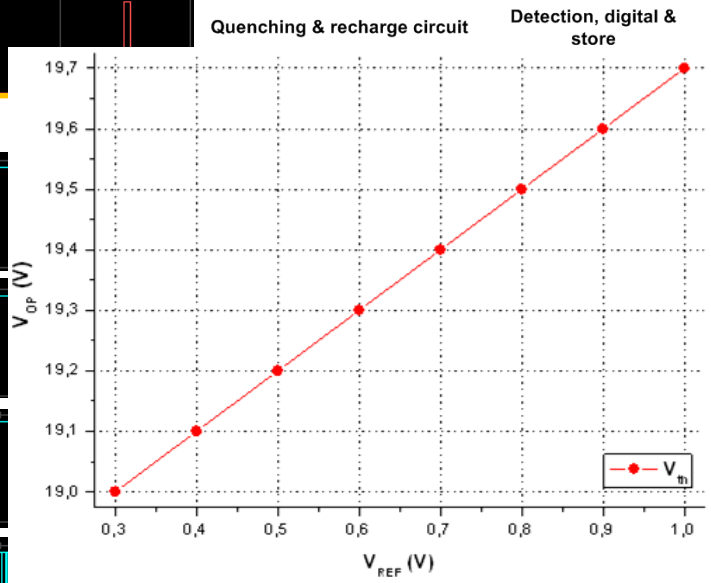
- **CLK1 = '0'** → **Latch mode. 2 possibilities:**
- **No hit or $V_{EX} < V_{REF}$**
  - $V_{sensing} < V_{REF}$ → V_{out+} = '0', V_{out-} = '1'
  - **OUT = '1'**
- **Particle hit & $V_{EX} > V_{REF}$**
  - $V_{sensing} > V_{REF}$ → V_{out-} = '1', V_{out-} = '0'
  - **OUT = '0'**

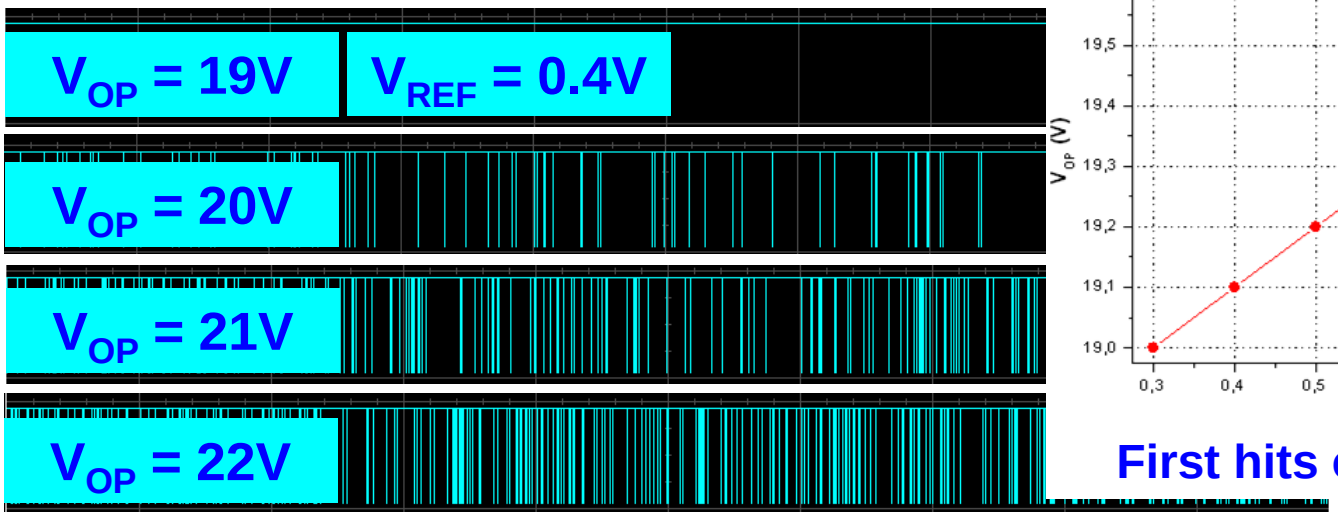


Test. Results.







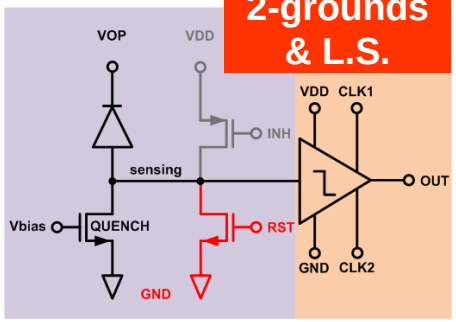


First hits observed (dark)

Δt = 1ms

Readout circuits. Comparison.

2-grounds & L.S.



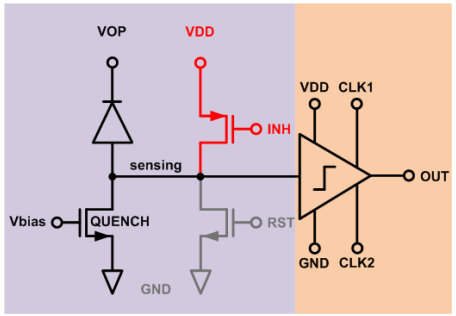
Quenching & recharge circuit

Detection, digital, store & read out

Signal	Value
RST	‘1’
CLK1, CLK2	‘1’
INH	‘1’

→

Propagation delay	
Readout circuit	‘0’
2 grounds scheme	1.8ns
Level shifter	1.7ns

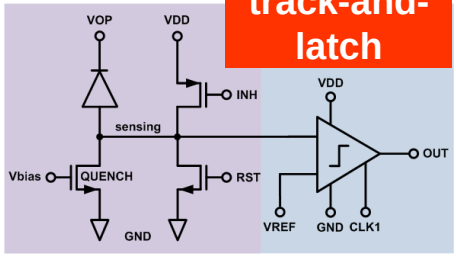


Signal	Value
RST	‘0’
CLK1, CLK2	‘1’
INH	‘0’

→

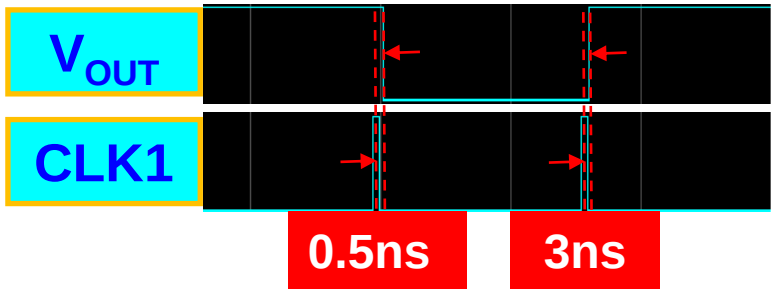
Propagation delay	
Readout circuit	‘1’
2 grounds scheme	0.5ns
Level shifter	1ns

track-and-latch



Quenching & recharge circuit

Detection, digital & store



Wait until the falling edge of CLK1 to observe the result of the ‘on’ period

- **Conclusions**
  - ✓ GAPD-pixels are possible candidates for tracking systems in future linear colliders in order to have single BX resolution
  - ✓ We have designed GAPD-pixels with low dark count rate
    - Standard 0.35μm HV-AMS CMOS technology
    - Sensitive area of 20μm x 100μm
    - Gated acquisition with an ‘on’ period of 10ns
    - Readout electronics for low reverse bias overvoltage operation
    - Quick response time and low power consumption
  - ✓ We work to fit ILC requirements
  - ? Coming soon...
    - Fabricated chips have already been received
    - Test is under development
  - ? In the future...
    - Study of different parameters of the sensor for the forward region tracker
    - Arrays, 3D….

Thank you very much for being such an attentive audience

Questions and comments are welcome

Back-up slides

Technology discussion

	Technology	
	HV-AMS 0.35 µm	**STM 0.13 µm**
PROS	✓ Low trap concentration ✓ Reduced dark count ✓ Lower storage data	✓ High density of integration ✓ High speed ✓ No afterpulsing ✓ Lower T dependance
CONS	X Reduced speed → active recharge X Afterpulsing → active quenching X Higher T dependence	X High dark count → gated mode X High storage data

HV-AMS 0.35µm