

Characterisation Of The NA62 GigaTracker End Of Column Readout ASIC

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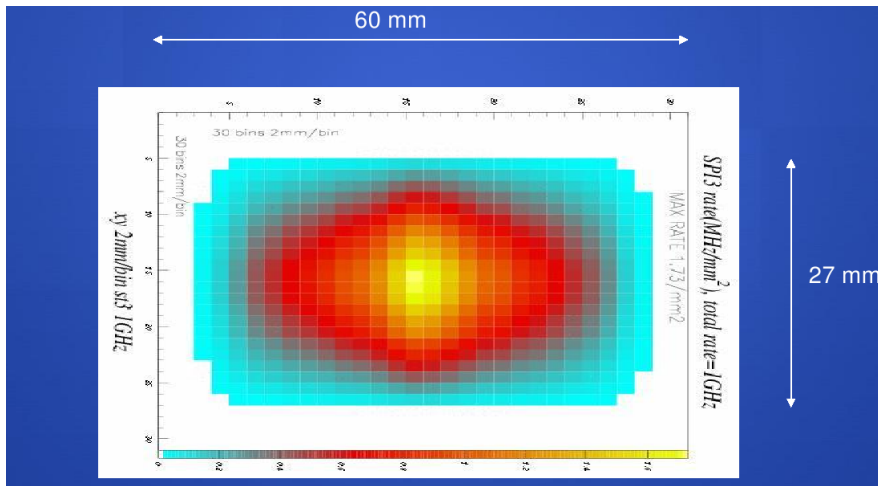
TWEPP-10.
20th-24th September 2010
Aachen.

¹matthew.noy@cern.ch

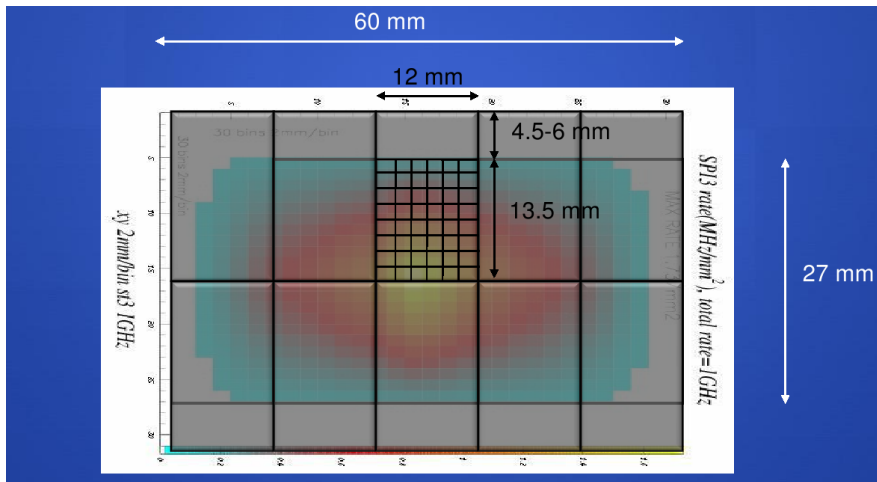
- 1 GTK Architecture and Requirements
- 2 Demonstrator ASIC
- 3 Testing Ethos and Methodology
- 4 Results
 - TDC Performance
 - Test Pixel Performance
 - Electrical Charge Injection: ASIC Full Chain
- 5 Synopsis

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Beam Profile



Beam and Detector Profile

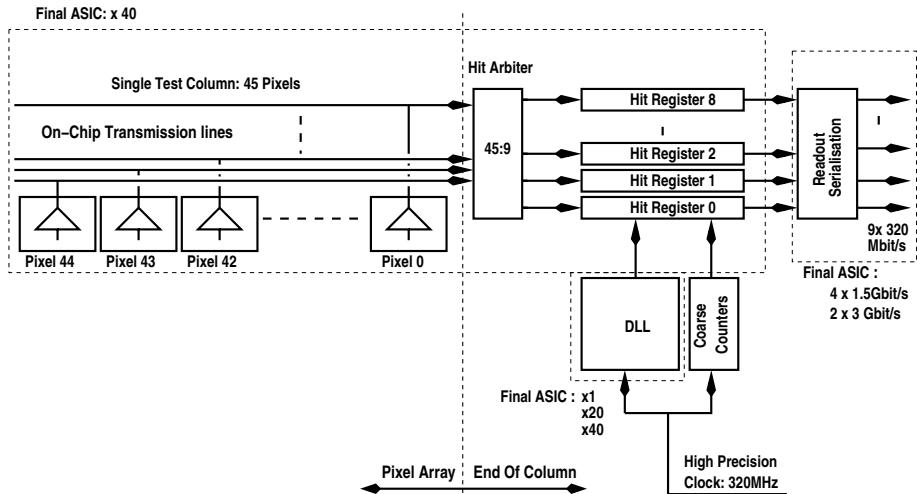


GigaTracker Requirements

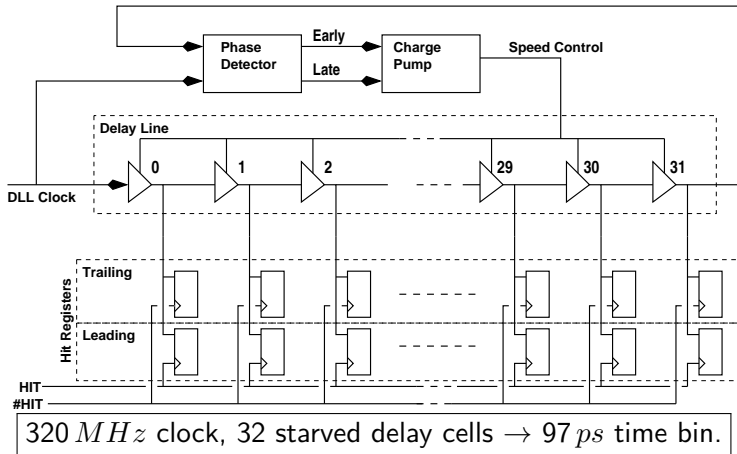
Radiation Environment	$10^{14} n cm^{-2} yr^{-1}$
Columns/Readout Chip	40
Pixels/Column	45
Pixel Size	$300 \mu m \times 300 \mu m$
Beam Rate	$800 MHz \rightarrow 1 GHz$
Dynamic Range	$\sim 1 fC \rightarrow 10 fC$
Q_{MP}	$2.4 fC$
Front End Peaking Time	$\sim 4 ns$
Time Binning	$\sim 97 ps$
Momentum Resolution	0.4%
Efficiency	$\geq 99\%$

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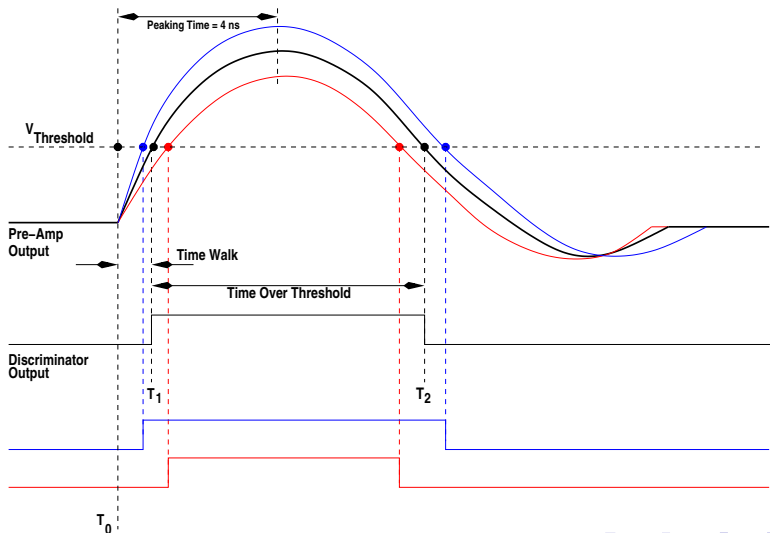
EoC Design Overview



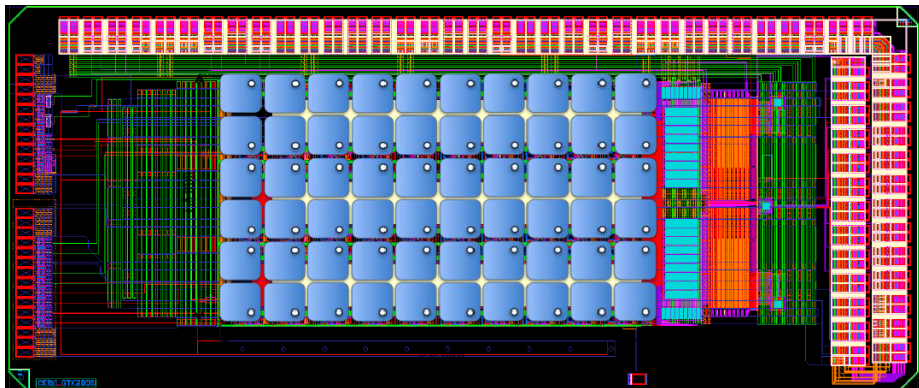
EoC DLL-Based TDC



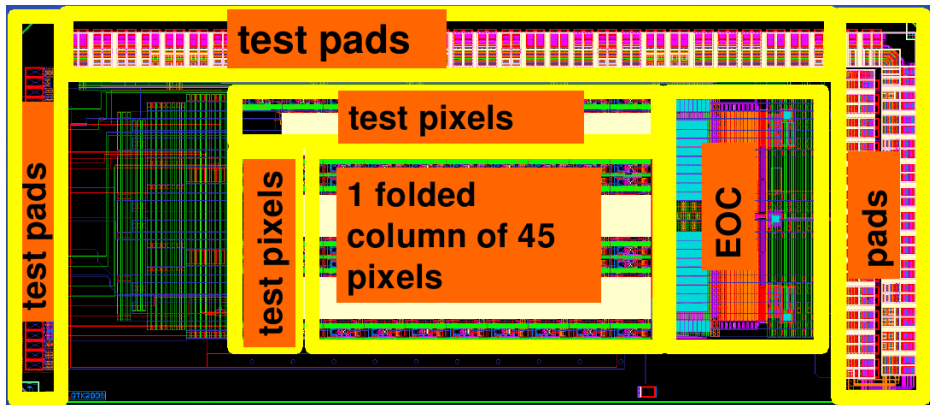
Time Over Threshold Time Walk Correction



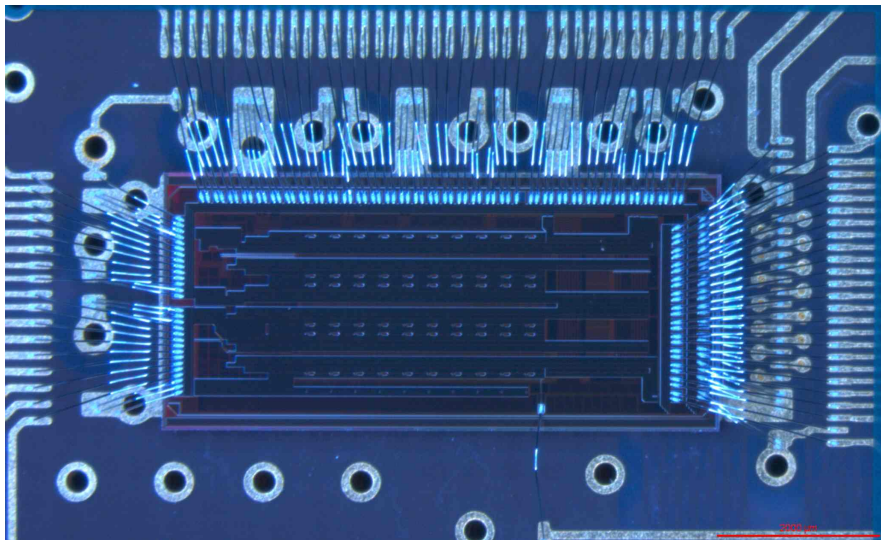
EoC: Chip Top Level Layout



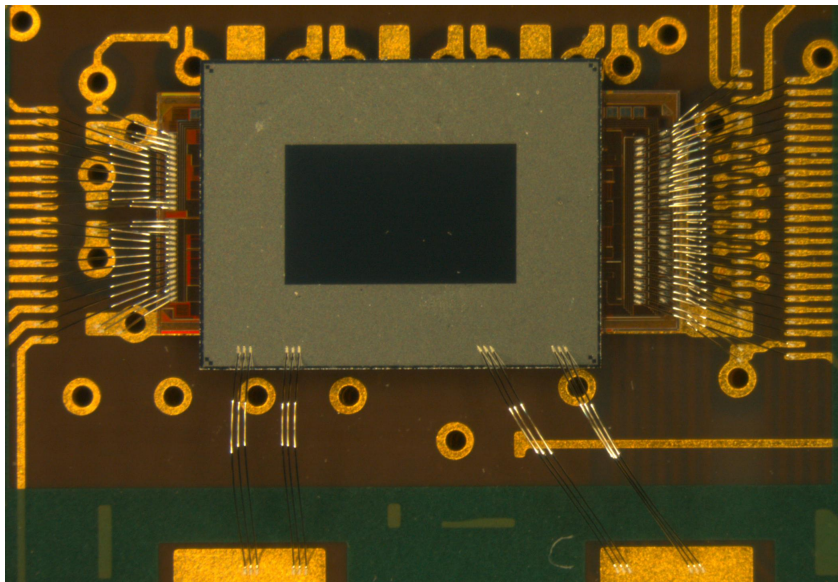
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EoC Chip



EoC Assembly



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 - ^{109}Cd and ^{241}Am γ emissions used

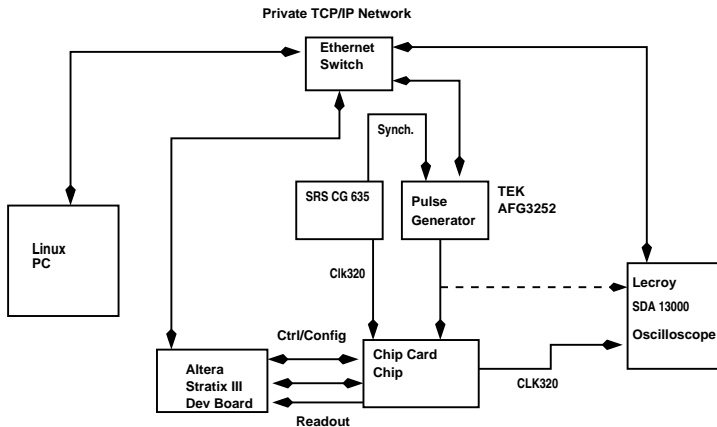
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- Laser Charge Injection
 - 60 *ps* FWHM, 1060 *nm* Laser
 - Light pulse timing is good to ~ 5 *ps* RMS
 - spot size ~ 10 μm at focal distance
 - X-Y stage to scan laser spot across pixel matrix

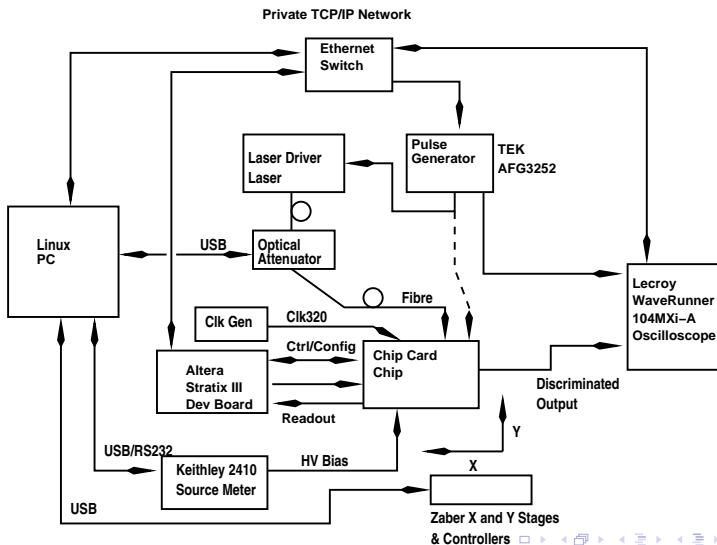
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 - X-Y stage to scan laser spot across pixel matrix
- Beam test
 - 10 *GeV* π^+/p^+ beam at PS (T9)
 - 4 cards placed in beam with GasTOF
 - underway now (16th \rightarrow 29th September 2010)

Testing Setup



Testing Setup

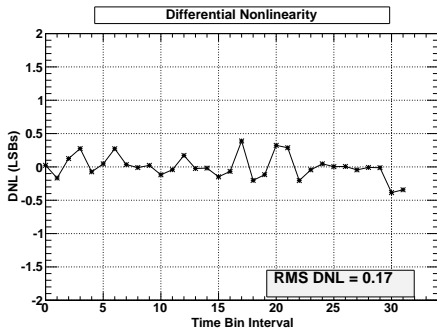


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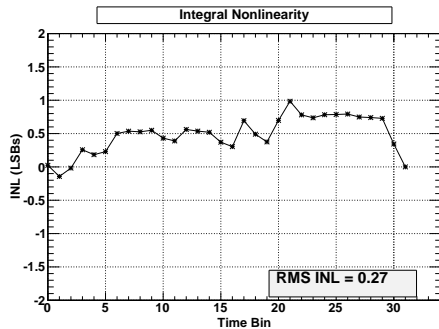
TDC Performance

EoC TDC Non-Linearity

Differential:



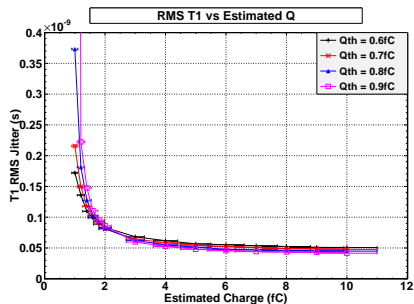
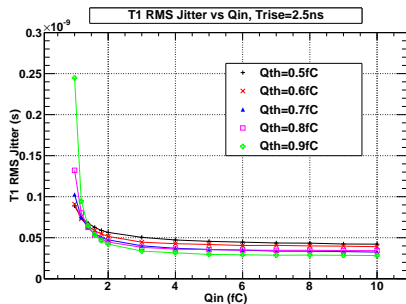
Integral:



DLL TDC Jitter = 7 ps

Test Pixel Performance

T1 RMS Jitter: Qin and Qth



Electrical charge injection.

No detector

~ 40 ps RMS at 2.4 fC

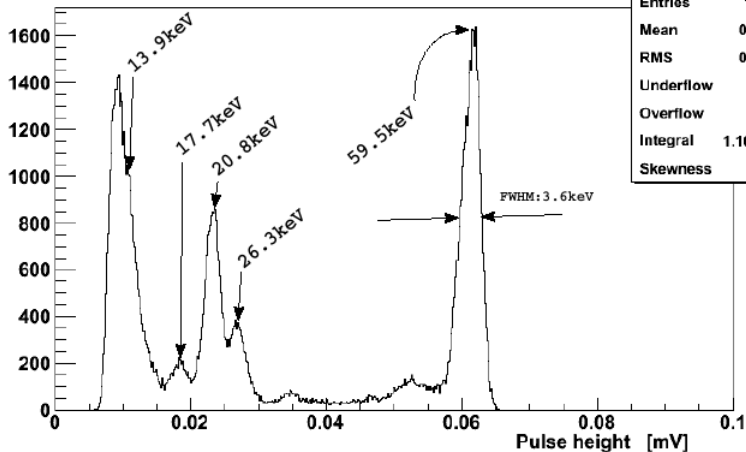
ENC $\sim 130 e^-$

Laser Charge Injection.

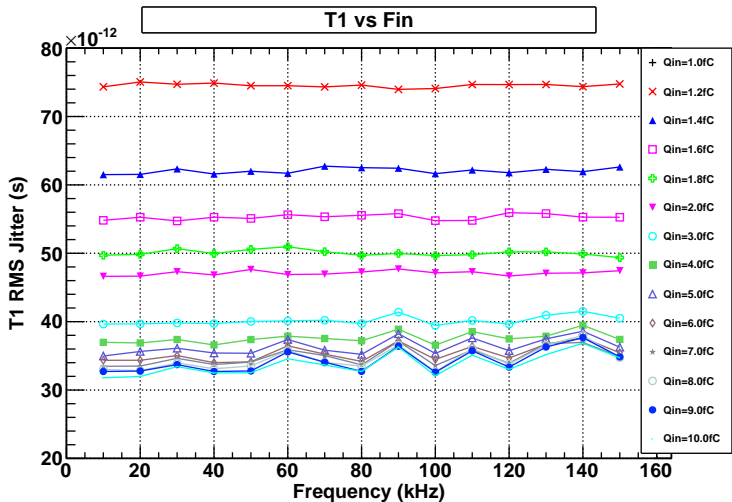
Detector biased at 300V.

~ 70 ps RMS at 2.4 fC

ENC $\sim 180 e^-$

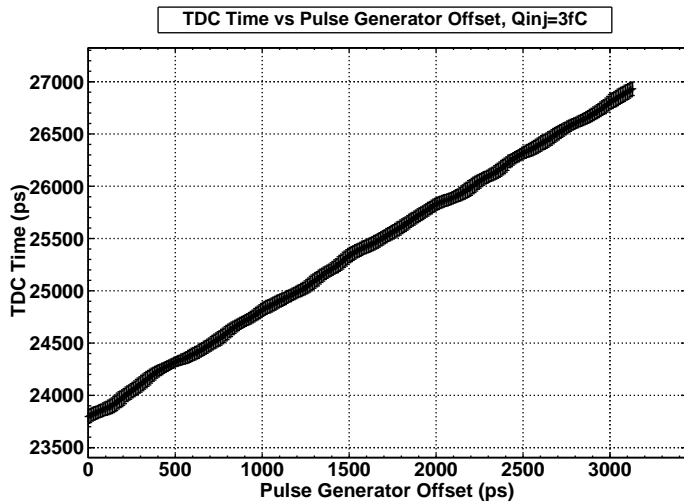
Analogue Pixel Pulse Height Spectrum with ^{241}Am Pulse height spectrum (^{241}Am source)

T1 RMS Jitter: Operation Frequency

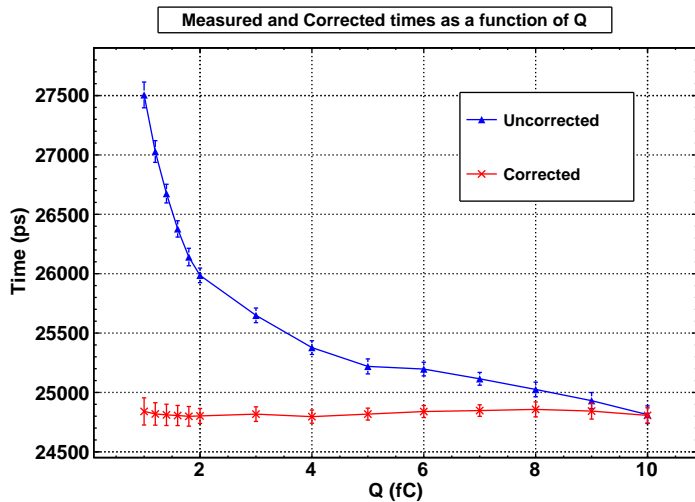


Electrical Charge Injection: ASIC Full Chain

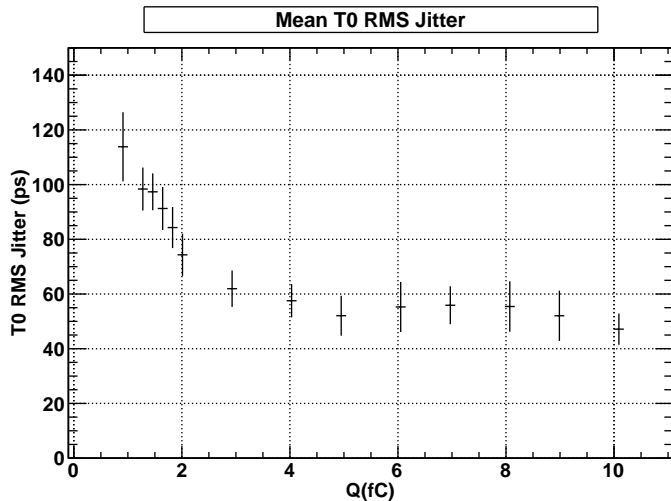
T0 Transfer Function



T0 and T1 as a function of Injected Charge

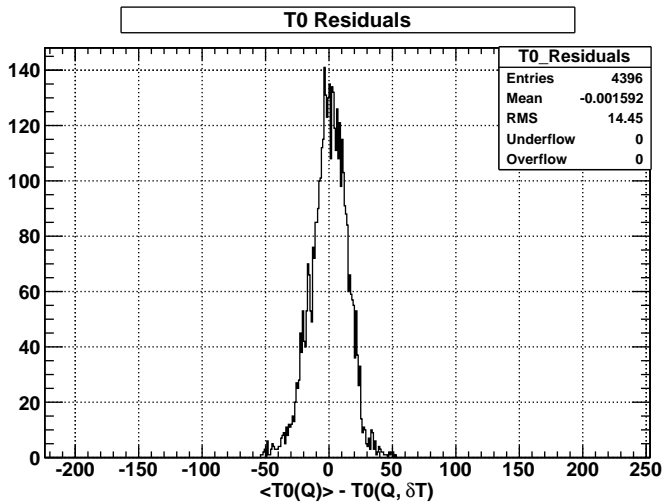


RMS T0 Jitter Vs Q: Average Case



Time walk compensated, full chain readout, all pixels firing.

Systematic (uncorrectable) Residual TimeWalk



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 - monotonic behaviour
 - RMS DNL ~ 0.17 LSBs
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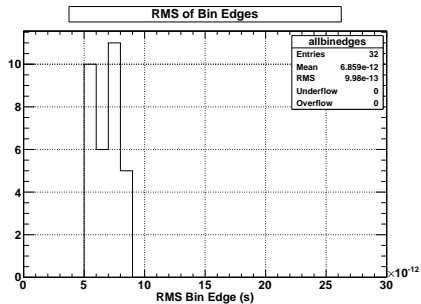
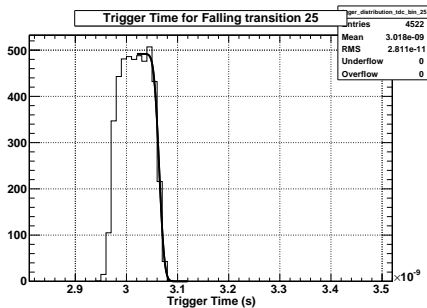
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 - Leading Edge Jitter ~ 40 ps bare ASIC at 2.4 fC
 - Leading Edge Jitter ~ 70 ps Full depleted sensor with light injection at 2.4 fC

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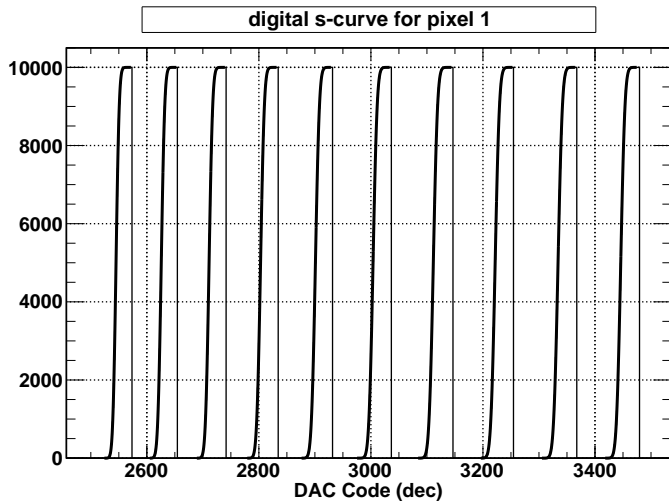
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 - Leading Edge Jitter $\sim 40 ps$ bare ASIC at $2.4 fC$
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- Full chain and time walk correction
 - timewalk correction mechanism shown to work well
 - Residual systematic remainder $< 15 ps$ RMS
 - RMS T0 Jitter $\sim 70 ps$ at $2.4 fC$ (bare ASIC)

Backup Slides

DLL Jitter

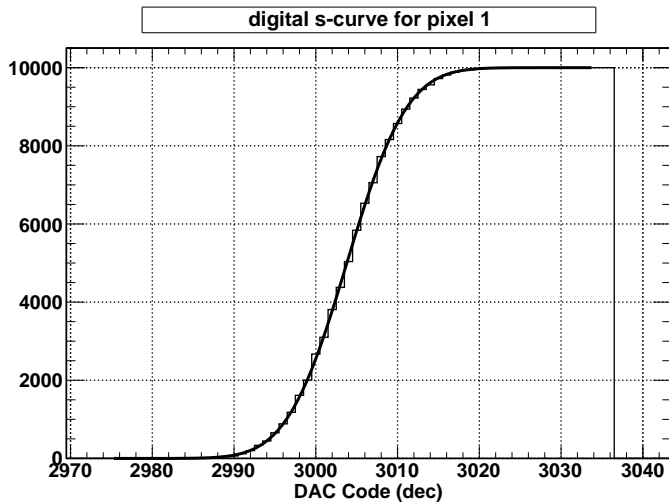


Chip 6 Full Column S-Curve @ 50V

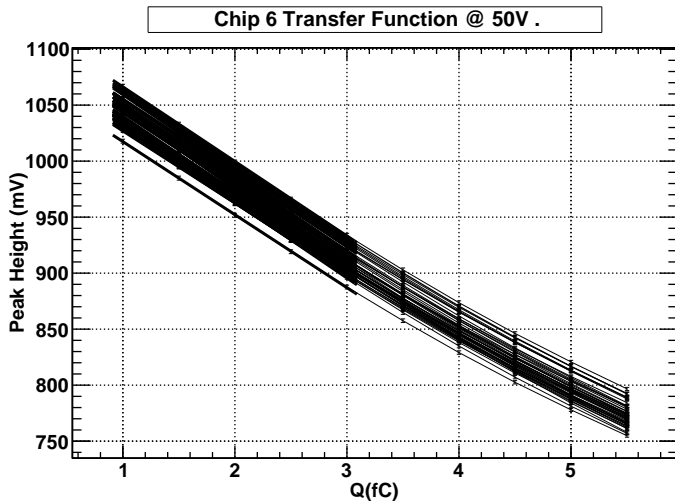


Charges $1.0 fC \rightarrow 5.5 fC$

Chip 6 Full Column S-Curve @ 50V: Zoom

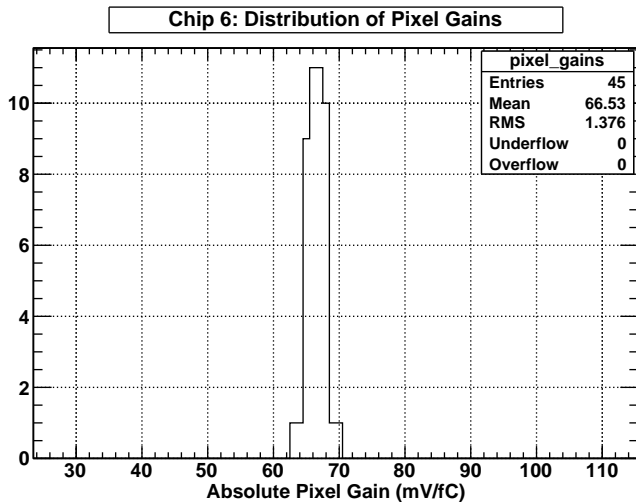


Chip 6 Full Column Transfer Functions @ 50V

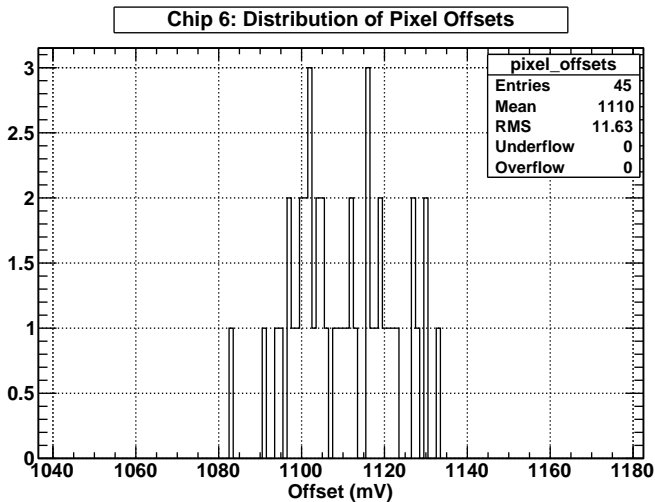


All 45 pixels from the full column are shown here

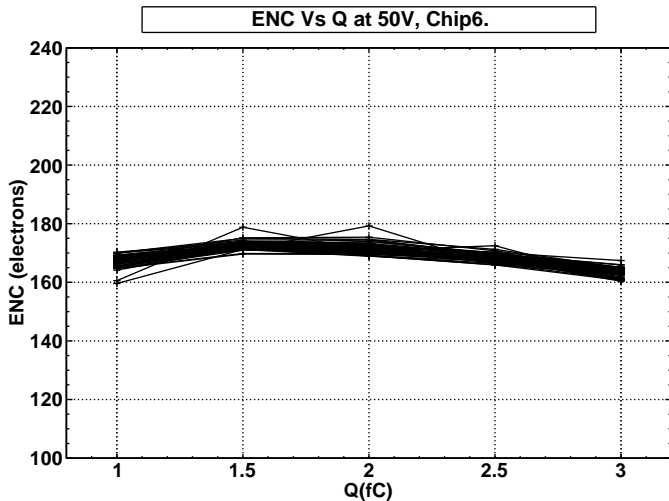
Chip 6 Full Column Gains @ 50V



Chip 6 Full Column Offsets @ 50V

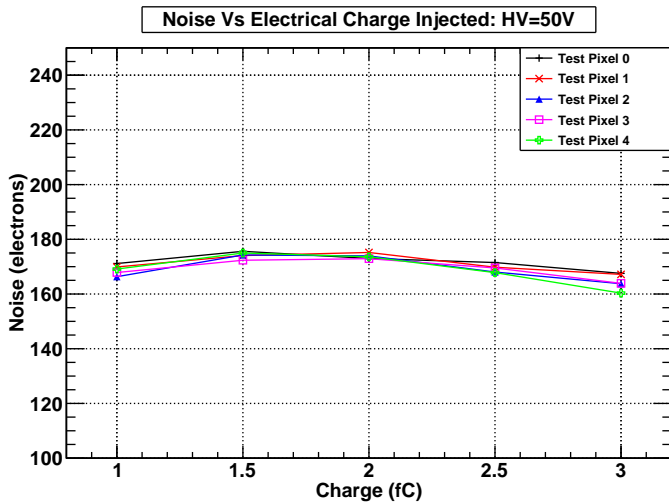


Chip 6 Full Column ENC @ 50V



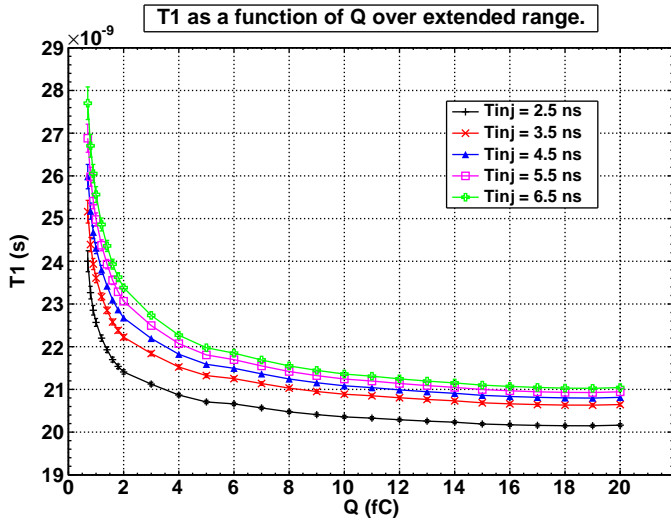
ENC is under $180 e^-$

Chip 6 Test Pixel ENC @ 50V

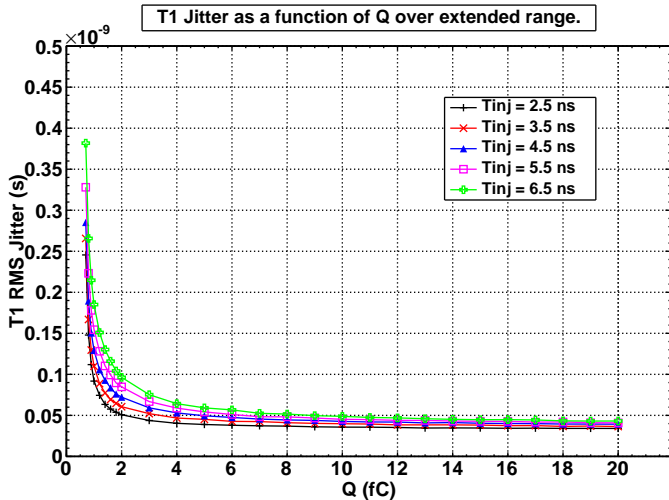


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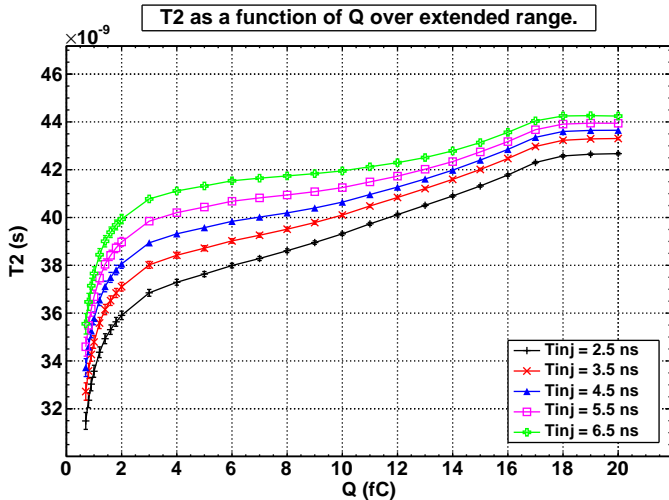
Extended Range T1



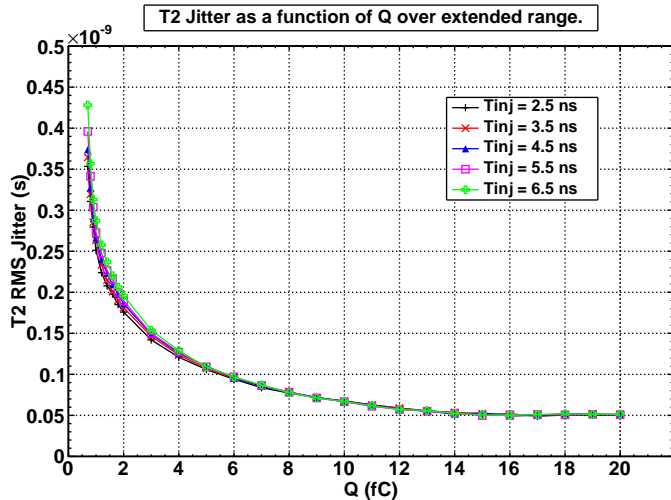
Extended Range T1 Jitter



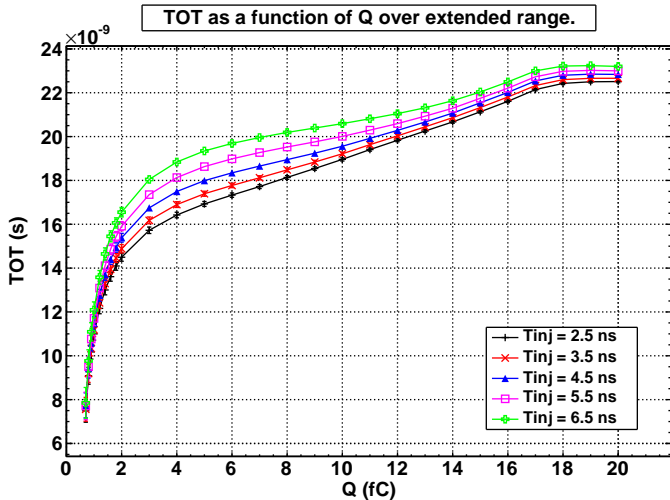
Extended Range T2



Extended Range T2 Jitter



Extended Range TOT



Extended Range TOT Jitter

