An FPGA-based backup version of the TileCal Digitizer

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Radiation Tolerance

The study of radiation tolerance in commercial FPGAs has a broad interest since, while their use is becoming widespread in high energy physics and space applications, there are still unknowns regarding the radiation effects in modern semiconductor technologies as feature sizes and geometries decrease.

The main focus of this work was to ensure sufficient radiation tolerance. Spartan 6 is not specifically designed for radiation tolerance but there are several techniques available to counteract this, such as post CRC check, triple mode redundancy (TMR), scrubbing and ECC. Our primary choice was a combination of ECC memories and TMR in the FPGA. We opted out of scrubbing of the Block RAM in the initial versions, because the memory content is changed too fast for this to be a concern. Should radiation tests show the memory to be a hot spot, scrubbing is easily implemented.

If an error occurs in the configuration memory one can order a reset via the TTCrx JTAG interface. There is also a built in automatic post CRC checker that is a standard feature in all Spartan 6 devices. It can not count errors however, which makes it too coarse to use for automatic reset, since we use TMR to be able to function with multiple errors. This error flag might still be useful and could be sent during idle times to flag that at least one error has occurred.

The ECC memories were implemented with Xilinx Coregen software. It can correct single bit errors in a 32 bit word and flag for 2-bit errors. Unfortunately we found that ECC implementation increased our FPGA utilisation by 25%. This is too high a price to pay for single bit correction of memories that are rewritten every 2.5us. If we did not have enough space to triple the memories, or if the memories were substantially larger, this would be an option to consider.

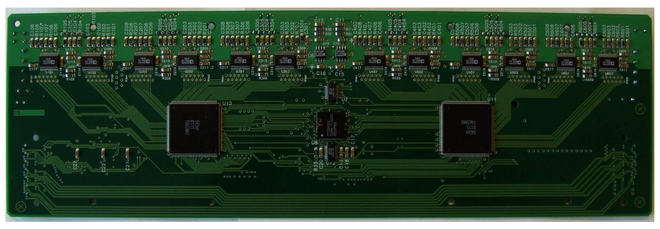
The new board will be subjected to radiation tests at the levels of the current ATLAS requirements and beyond, comparing different levels of TMR. The radiation requirements are not as high as for the most exposed components (eg. the inner detector) due to the protected positions of the TileCal drawers.

These tests will also give us useful experience and data for our work with the ATLAS upgrade.

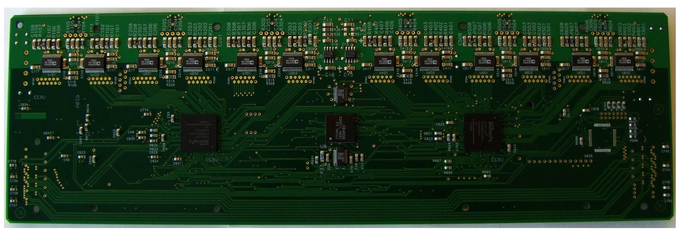
Introduction

The ATLAS TileCalorimeter contains some 2000 digitizer boards with 2 TileDMU ASICs on each board. The TileDMUs are responsible for all digital operations on the board except for those taken care of by the TTCrx (Cern made Timing, Trigger and Control receiver chip). We have more than the agreed number of board and component spares. However, in the unlikely event that we run out of spares anyway or if a catastrophic failure occurs it would help to have a backup solution.

The original version contains both outdated and custom made circuits which are difficult or impossible to find in sufficient numbers. This version uses a cheap off the shelf FPGA (Spartan 6) instead of an ASIC. The FPGA has all the functionality of the TileDMU but will be readily available for a considerable time. It is functionally compatible with the current version and to a large extent uses the same code. The general idea is to leave the digitizer design as intact as possible since it is well tested and well performing. We have added in system programmability via TTCrx for both the FPGA and the configuration memory using one way JTAG. This provides a way to recover from radiation damage in the PROM as well as tweaking the system without having to replace boards.

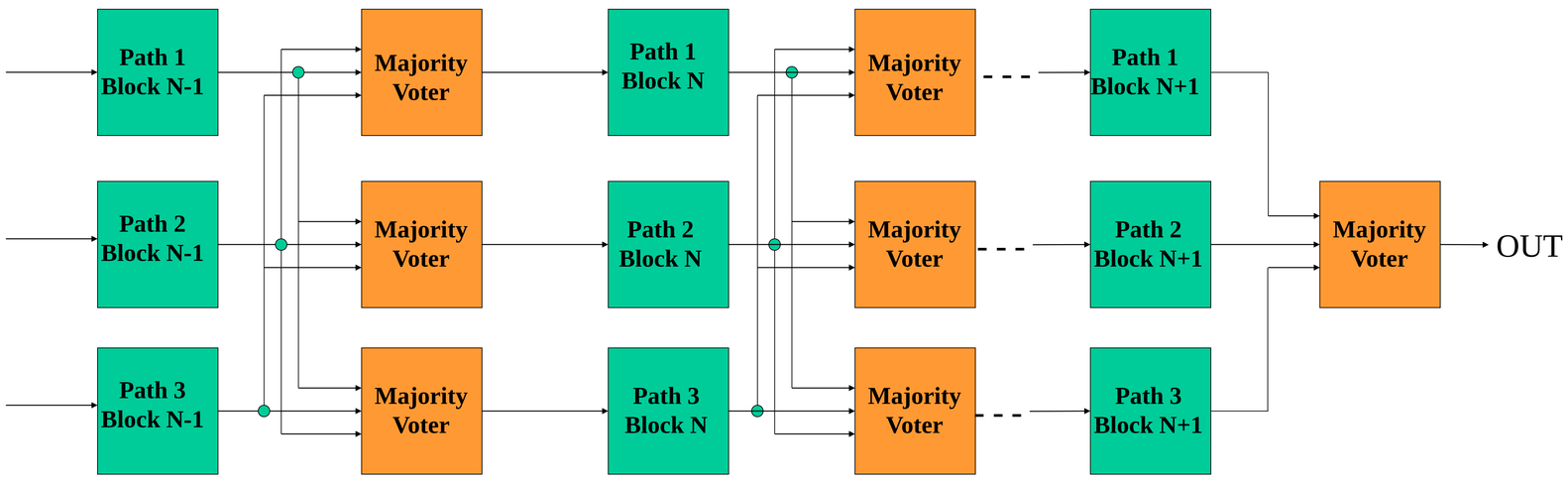


Current Digitizer with TileDMUs



New Digitizer with Spartan-6

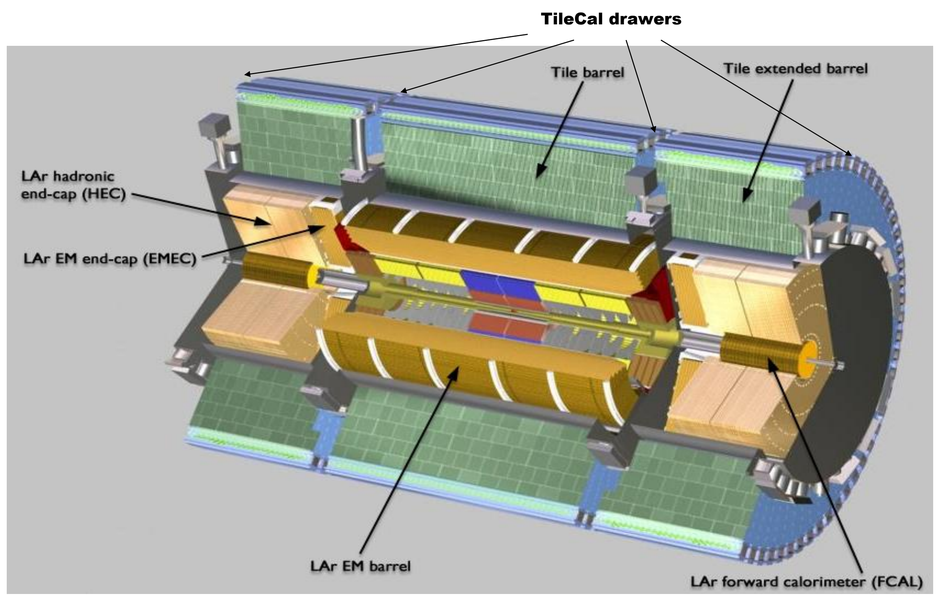
Triple Mode Redundancy (TMR)



The TMR consists of majority voters in several stages. The voters connect the 3 paths so that it can maintain functionality even with multiple errors as long as the errors occur in separate sections. Further redundancy can include triplicating the component pins which we chose not to do due to routing constraints.

The TMR we have implemented can easily be increased to higher orders of redundancy and increased complexity

A number of tools for implementing TMR and other mitigation techniques have recently reached the market, like Xilinx's XTMR and Mentor's Precision rad-tolerant, but these are still quite expensive. This work shows that robust TMR can be implemented without too much effort with ordinary tools. For more advanced features, such as soft cores or very large designs these tools are necessary.



Final design

The new board has been tested, has all the functionality of the current version used in ATLAS and can be plugged into the existing system. If the results from the radiation tests are positive, the final version of these boards can gradually start to be used during refurbishments if needed. The prototype has a CPLD in order to try out the JTAG via TTCrx functionality. In the final version this will be done in a more efficient and robust way. We may also add features like PTC resettable fuses and voltage monitoring. Upgrading components no longer in production is also a concern.