CMS Pixel Detector with new Digital Readout Architecture

Beat Meier *Chip Design Core Team*
Paul Scherrer Institut, 5232 Villigen, Switzerland
beat.meier@psi.ch

New Readout Chip Design for Phase I Upgrade

Abstract

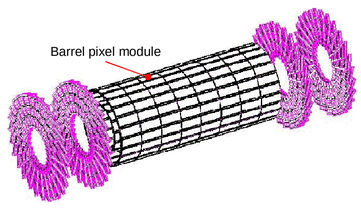
The CMS pixel detector is planned to be upgraded in 2016 to a new one with a significantly reduced material budget. The new pixel system with more layers (4 for the barrel pixel) has to operate through the existing services at double the luminosity. Therefore a new readout scheme is implemented with a new pixel read out chip (ROC).
A description of the ASIC modifications of the digital readout interface of the ROC is presented as well as the results and the performance of the physics based electronic simulations of a complete pixel module consisting of 16 pixel ROCs and a token bit manager chip.

Requirements for Phase I Upgrade

R1 4 layers for the pixel barrel detector instead of 3
3 layers for the forward detector instead of 2

R2 Reduction of material budget (Mechanical structure, cooling, Cabling)

R3 Design for double the luminosity ($2 \cdot 10^{34}$ cm^{-2} s^{-1})

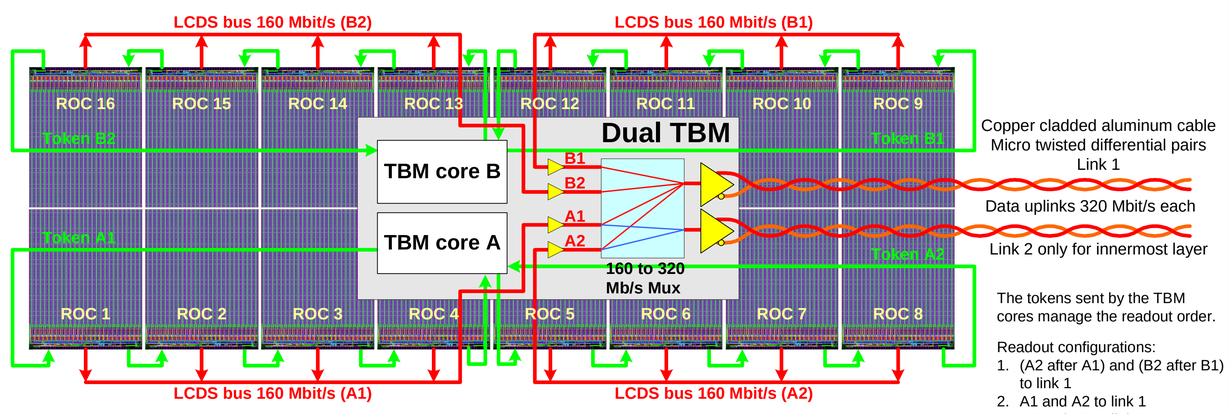


Schematic view of the present CMS Pixel detector consisting of 3 barrel layers and 2 forward disks on each side. For the phase I detector upgrade, 4 barrel layers and 3 forward disks on each side are intended.

Limitations & Modifications

1. R3 → L1 trigger latency buffer overflows cause resets in double columns (dominating data loss)
   → **Increase number of data buffers in double columns**
2. R3 → Readout related dead-time at higher data volumes (blocked buffers in double columns)
   → **Additional readout buffer stage**
3. R1 → Higher module count with more layers and the same number of fibers
   → **Digital readout** and data link with 320 MBit/s
4. R2 → **Micro twisted pair cables** for signals

Module with new Readout Scheme

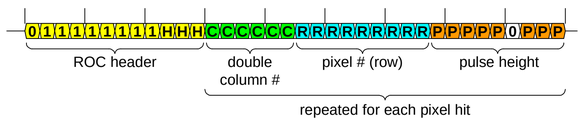


The tokens sent by the TBM cores manage the readout order.

Readout configurations:
1. (A2 after A1) and (B2 after B1) to link 1
2. A1 and A2 to link 1
   B1 and B2 to link 2

Digital Readout

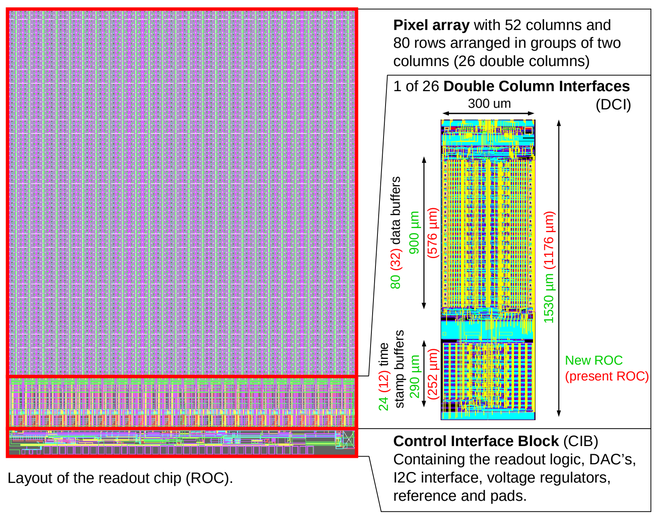
The new digital ROC readout is running at 160 Mb/s. Two serial data streams are recombined in the dual TBM chip to a single serial data stream at 320 Mb/s. Optimized drivers and receivers for LCDS (low current differential signal) are designed for very low power consumption.



Proposed data format for the digital output of the ROC

The following new blocks for the ROC are needed:
- LCDS drivers and receivers (design tested at 320 Mb/s)
- PLL clock multiplier to provide higher clock frequencies for the serial data transfer (designed and tested)
- New control logic and readout buffer FIFO (dig. simulation)
- 8 bit ADC to digitize the analog pulse height information

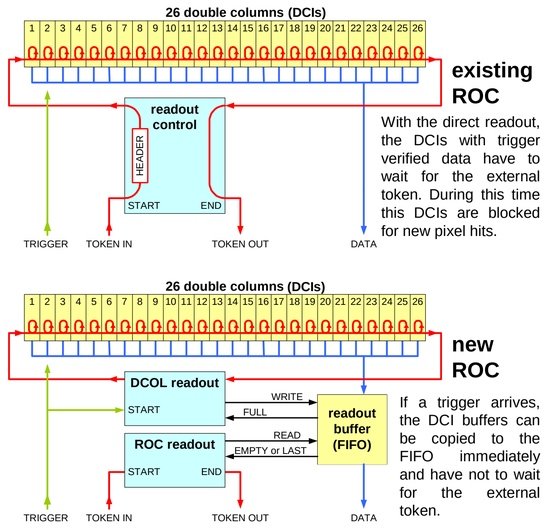
Data Buffers in Readout Chip (ROC)



Layout of the readout chip (ROC).

In the double column interface (DCI) more buffer cells have to be added. The bigger size can partially be compensated by smaller memory cells. The readout logic in the CIB will be replaced by a buffered, fully digital readout at 160 Mb/s. A PLL to provide the 160 MHz clock and a 8 bit ADC has to be added. The new readout buffer will be added between the DCI and the CIB. There are no modifications needed in the pixel array.

Insertion of a ROC global readout buffer (FIFO)



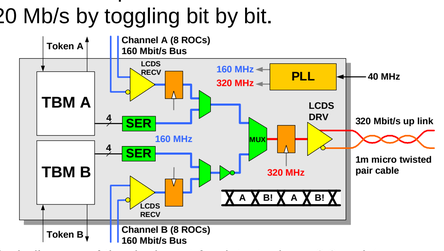
With the direct readout, the DCIs with trigger verified data have to wait for the external token. During this time this DCIs are blocked for new pixel hits.

If a trigger arrives, the DCI buffers can be copied to the FIFO immediately and have not to wait for the external token.

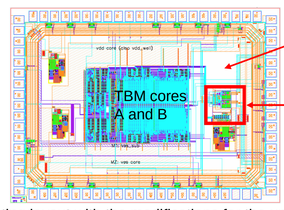
At double the luminosity an additional readout buffer (FIFO) is needed to separate the double column readout from the ROC readout. In this way, the waiting time of the data in the double columns buffers can be reduced significantly.

Dual Token Bit Manager (TBM)

For the upgrade the existing TBM has to be changed. The two TBM cores that manage the ROC readout have to be redesigned slightly (see "Critical Trigger and Readout Timing"). The new data multiplexer refreshes the signals from the ROCs, adds the TBM header and trailer to the data stream and multiplexes two 160 Mb/s data streams together to 320 Mb/s by toggling bit by bit.



Block diagram of the dual TBM for detector layer 2,3 and 4 configuration with one data link



PLL to generate the 320 and 160 MHz clock

Existing analog switch replaced by digital multiplexer

Designed by Ed Bartz Rutgers University

Existing layout with the modifications for the upgrade

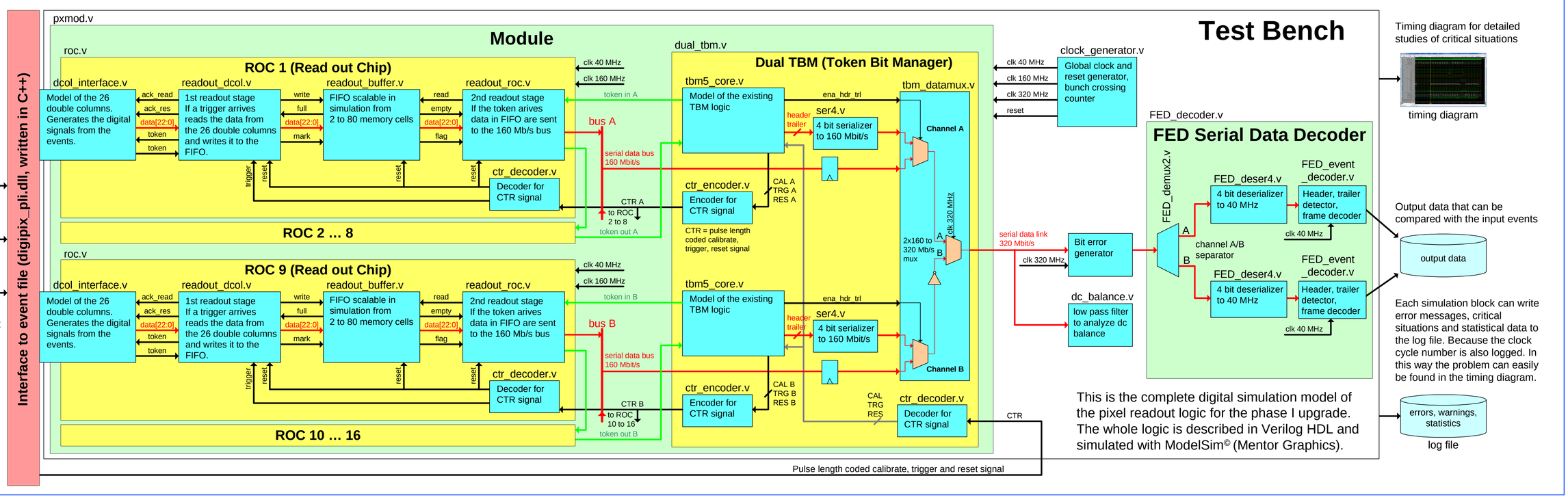
Digital Simulation with Physics Data

Simulation Model

Physics and detector simulation results from the CMS software (PYTHIA, GEANT) with different luminosity and trigger rates as input for a digital logic simulation with Modelsim® under realistic condition.

physics simulation PYTHIA, GEANT
or
random data
or
handwritten events

Handwritten stimulus to test the module under different critical situations.



Timing diagram for detailed studies of critical situations

timing diagram

Output data that can be compared with the input events

output data

Each simulation block can write error messages, critical situations and statistical data to the log file. Because the clock cycle number is also logged. In this way the problem can easily be found in the timing diagram.

errors, warnings, statistics

log file

This is the complete digital simulation model of the pixel readout logic for the phase I upgrade. The whole logic is described in Verilog HDL and simulated with ModelSim© (Mentor Graphics).

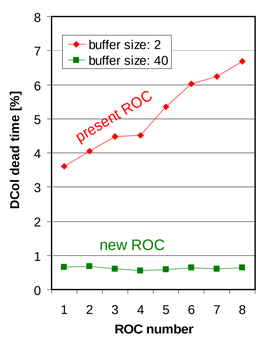
Introduction

The goal of the overall simulation is to test the new ROC and TBM logic before doing the layout. This should be done under realistic conditions to cover all possible critical situations. In particle physics experiments a digital circuit should be able to cope with widely fluctuating data. To setup such a simulation, an interface program library for the digital simulator is written to access the physics data. In this way, it is possible to simulate over millions of clock cycles.

Simulation Performance

- Overall simulation of a whole module with 16 read out chips (ROC) and a TBM
- Clock cycle by cycle exact simulation (40 MHz, 160 MHz and 320 MHz) including serial data stream
- Each block can send messages to a log file
- Simulation speed: 70µs (2800 bunch crossings) per 1s

Double Column Dead Time

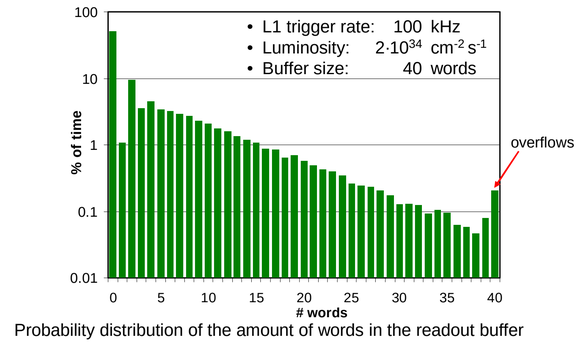


This plots shows the simulation results of the double column waiting time in percent of the 8 ROCs in a token chain. Chip 1 receives the readout token first.

Simulation conditions:
- Simulation over 500,000 clock cycles (bunch crossings)
- L1 trigger rate: 100 kHz
- Luminosity: $2 \cdot 10^{34}$ cm^{-2} s^{-1}

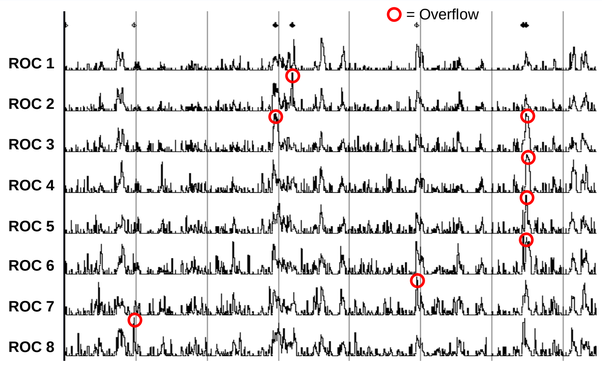
The red curve (read out buffer size 2) comes nearest to the existing pixel chip without a readout buffer. The green curve shows the improvement with a readout buffer of size 40.

Readout Buffer Fill State



Probability distribution of the amount of words in the readout buffer

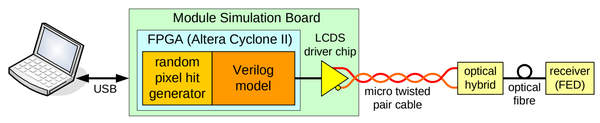
Numbers of Data Words in the Readout Buffer



- Simulation over 4 ms or 160,000 clock cycles
- Simulation time: 60 s
- L1 trigger rate: 100 kHz
- Luminosity: $2 \cdot 10^{34}$ cm^{-2} s^{-1}
- Buffer size: 40 words (events)

FPGA Implementation of Simulation Model

It is planned to implement the Verilog model of the module in an FPGA. The physics data file interface is replaced by a random pixel hit generator.



The Verilog model with a random pixel hit generator implemented in an FPGA. At the output a LCDS driver chip with the micro twisted pair cable, the optical link and the FED.

Application of the FPGA pixel module:
- Test of cables, optical link with realistic data
- Test of FED decoding
- Development of new test board firmware

This tests do not need to wait for the complete chip and module prototype.

Module simulation board with FPGA, containing the module emulator and a CPU (NIOS II) with an USB interface to communicate with a PC. On the right side are the LCDS driver chips and micro twisted pair cables to the optical link.

Critical Trigger to Readout Timing

Between the trigger and the token from the TBM, the first ROC in the token chain has only 8 clock cycles to process the first pixel hit what is too short. In this time the analog pulse height has to be converted in the ADC and the result has to be copied to the readout buffer. Therefore, the TBM core has to be modified slightly to have an additional clock cycle.

This timing diagram shows a short sequence of a simulation with the critical situation.