Microelectronics User Group Meeting

TWEPP 2010, Aachen, Germany

22/9/2010

Agenda

- *16:45 – 17:00*

  "ASIC design tools and foundry services at CERN"
  by Kostas Kloukinas (CERN)

- *17:00 – 17:15*

  "Update on the Design Implementation Methodology for a 130nm process"
  by Sandro Bonacini (CERN)

- *17:15 – 17:30*

  "Discussion"

ASIC technology support and foundry services at CERN

Kostas Kloukinas
CERN, PH-ESE dept.
CH1211, Geneve 23
Switzerland

Overview of Technologies

- Foundry services & Technology technical support provided by CERN.

CMOS 8RF-LM

Low cost technology for Large Digital designs

CMOS 8RF-DM

Low cost technology for Analog & RF designs

BiCMOS 8WL

Cost effective technology for Low Power RF designs

BiCMOS 8HP

High Performance technology for demanding RF designs

CMOS 9SF LP/RF

High performance technology for dense designs

130nm CMOS

90nm CMOS

CMOS 10LPRF

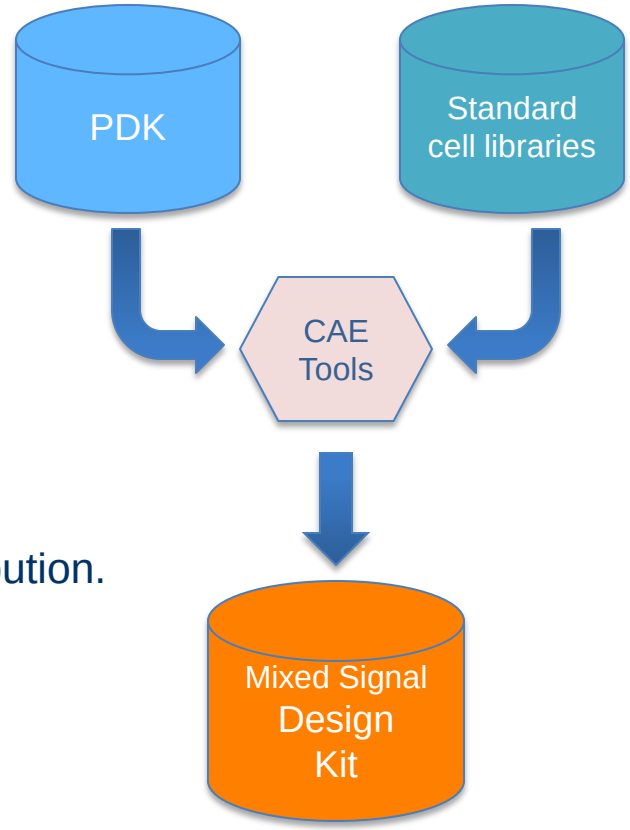
High performance technology for dense designs

65nm CMOS

- Mainstream technology CMOS8RF-DM (130nm)
  - Full support: CERN compiled Mixed-Signal design kit
- Advance technology CMOS9LP/RF (90nm)
  - Limited support: Project specific.
  - Development of a “lightweight” standard cell library is in progress.
- Future technology CMOS10 (65nm)
  - Plans to evaluate 65 nm processes for SLHC applications.
  - Access to Physical Design Kit.
  - No user support yet.

CMOS8RF Mixed Signal design kit

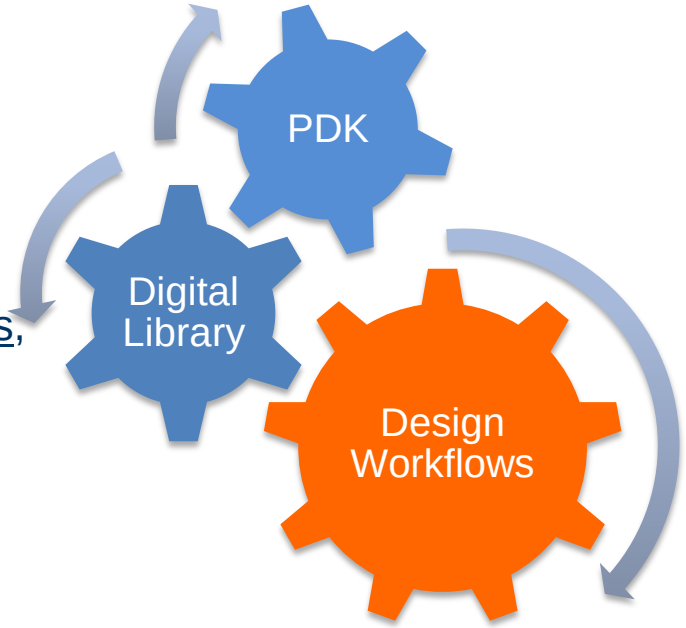
- Mixed Signal Kit V1.7
  - Based on foundry PDK V1.7.0.2
  - Ready for release (Sept. 2010)
  - Foundry Standard cell and IO pad libraries
    - Physical Layout views available.
    - Access to standard cell libraries is legally covered by standing CDAs with the foundry.
  - New versions of CAE Tools
    - Compatible with the *"Europractice" 2010* distribution.
    - Open Access database.
  - Bug fixes and Important updates.
    - *Presentation by Sandro Bonacini*
  - Support for LINUX Platform
    - Qualified on RHEL4 & RHEL5



- Two design kits available:
  - CMOS8RF-DM (3-2-3 BEOL)
  - CMOS8RF-LM (6-2 BEOL)

CMOS8RF Mixed Signal Workflows

- Analog & Mixed Signal (AMS) Workflows.
  - Formalize the design work by employing standardized and validated Design Workflows.
  - Formalize the design work across design teams in common projects.
  - Provide a repository with reference design examples, presented in AMS Workshop training sessions.



- Development work subcontracted to Cadence, VCAD design services.
  - Close collaboration of CERN - VCAD - IBM
    - VCAD brought in their invaluable expertise on the CAE tools
    - IBM provided the physical IP blocks and important technical assistance
    - CERN assisted the development and validated the design kit functionality.

- Key Technology
  - Design kit that supports CAE tools based on Open Access database.

Design Kit Distribution

- The Mixed Signal Design kit is available to collaborating institutes.
  - Distributed to 25 Institutes and Universities
  - No access fees required.
  - Pay-per-use scheme.
    - A 7% fee is applied on the fabrication cost (prototyping, production).
    - This fee covers part of the design kit maintenance costs.

- For New Users
  - To acquire the CMOS8RF Mixed Signal Design Kit
  - Contact Bert.Van.Koningsveld@cern.ch
    or Kostas.Kloukinas@cern.ch
  - Establish a CDA with foundry (if not already in place).
  - Granted access to the CERN ASIC support web site.

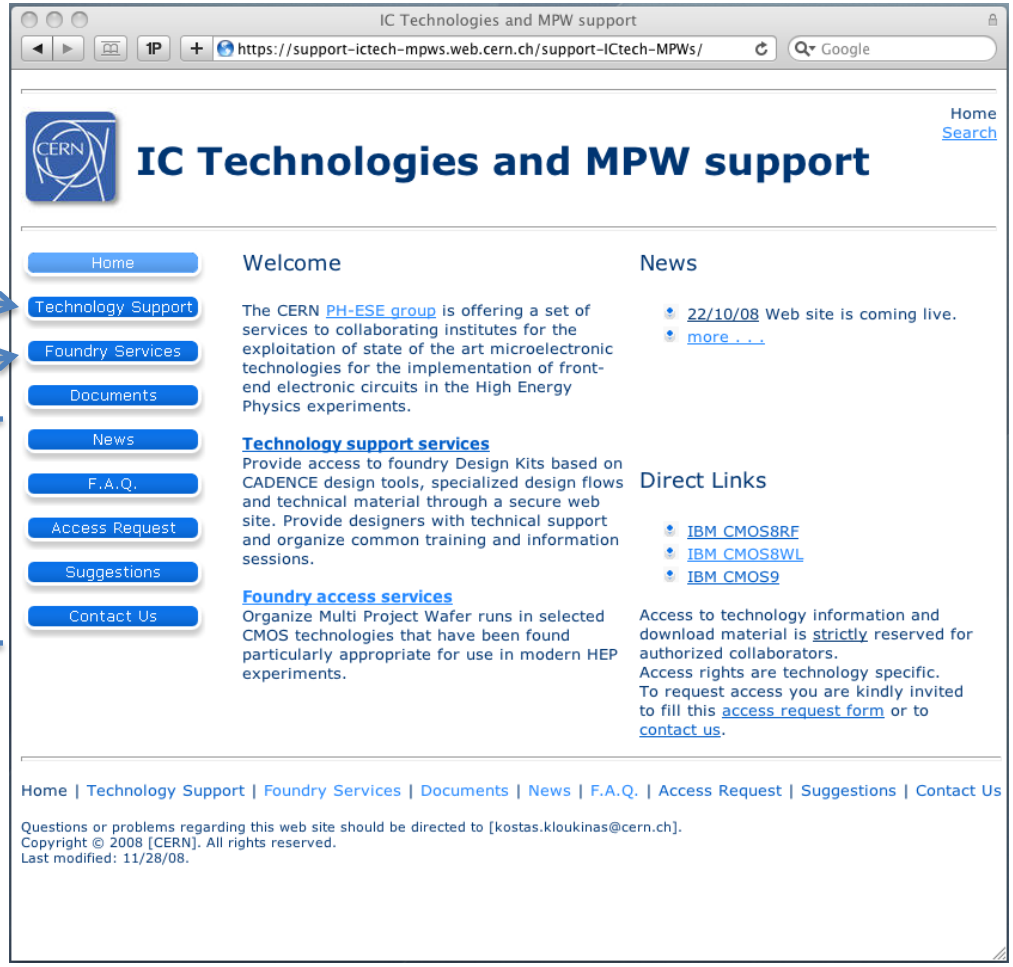
The CERN ASIC support website

http://cern.ch/asic-support

Download Design Kits and access technical documents (**restricted access**)

Information about MPW runs and foundry access services.

Communicate news and User support feedback forms and access request forms.



User Support and Training

- Maintenance
  - Distribution of PDK updates.
  - Design Workflow updates and enhancements.
  - Updates for new versions of CAE tools.
- User Support
  - Technical Support for Design Workflows.
  - Limited to the distributed Design Kit versions, running under the supported versions of the CAE design tools.
- User Training
  - Training sessions organized by CERN.

Training: AMS Workshops

- The scope of the Workshop :
  - Present the CMOS8RF (130nm) Mixed Signal Kit.
  - Present Analog, Digital and Mixed Signal design Workflows.
  - Introduce the new Platform of CAE Tools.
- This is NOT:
  - A course on analog and digital circuit design.
  - A detail course on specific CAE Tools.
- Details
  - 5 days training with short lectures and exercises (hands-on experience)
  - 2 engineers per workstation, 10 engineers per session
  - Instructors from Cadence (VCAD) design services team.
  - Training material (scripts, design examples) is made available to participants.
  - Practical example on Triple Module Redundancy for SEU tolerant designs.
  - Cost: 900 euros per participant

AMS Workshop Contents

- **Day 1** (Instructor: Maxime Barbe)
  - Introduction to AMS kit Workshop
  - Functional Verification : Digital Simulation Flow
  - Functional Verification : AMS Simulation from command-line
  - Functional Verification : AMS Simulation from DFII
- **Day 2** (Instructor: Maxime Barbe)
  - Analog IP Characterization : ADEXL
  - Overview of IC6.13 (ADEXL and VSE)
  - Analog Block Creation: Constraints

Analog
&
Mixed Signal

- **Day 3** (Instructor: Vincent Cao Van Phu)
  - Hierarchical Floorplaning (Virtuoso based)
  - CDB IP Import to OA database for IC61 Methodology
- **Day 4** (Instructor: Vincent Cao Van Phu)
  - Digital Block Implementation
  - Block IP Characterization Back End
  - Digital IP Characterization Front-End

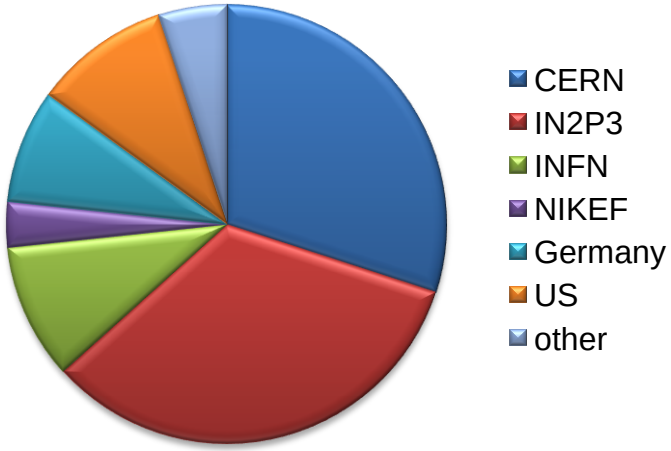
Digital

- **Day 5** (Instructor: Vincent Cao Van Phu)
  - Constraint Driven Analog Block Creation Back-End
  - DRC (Calibre + Assura workflows)
  - LVS (Callibre + Assura workflows)
  - Extraction
  - *Round table discussion and workshop evaluation (30min).*

Physical Verification

AMS Workshops

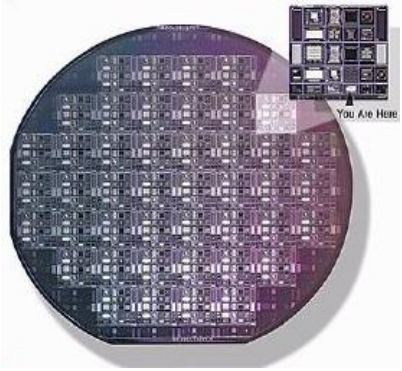
- Workshop sessions
  - 1st session: 26/10 – 30/10, 2009 (CERN internal engineers, “pilot” run)
  - 2nd session: 16/11 – 20/11, 2009 (CERN, open to external engineers)
  - 3rd session: 30/11 – 4/12, 2009 (IPHC, Strasbourg, France)
  - 4th session: 1/2 – 5/2, 2010 (CERN, with fees)
  - 5th session: 15/2 – 19/2, 2010 (CERN, with fees)
  - 6th session: 1/3 – 5/3, 2010 (CERN, with fees)
  - 7th session: 12/4 – 16/4, 2010 (CERN, with fees)
- Statistics
  - 10 engineers/session.
  - 70 engineers in total.



- New Sessions
  - 8th session: planned for October 18-22, 2010
    (new design kit, enhanced workflows)
  - 9th session: planned for the end of 2010.
  - **If you wish to attend please contact: kostas.kloukinas@cern.ch**
    or our secretary **evelyne.dho@cern.ch**

Access to Foundry Services

- Supported Technologies:
  - IBM CMOS6SF (0.25μm), legacy designs
  - IBM CMOS8RF (130nm), mainstream process
  - IBM CMOS8WL & 8HP (SiGe 130nm)
  - IBM CMOS9LP/RF (90nm)

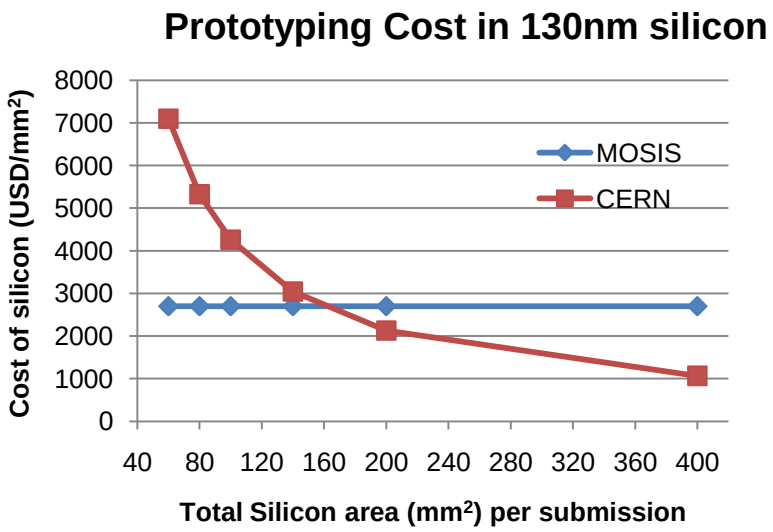


- Engineering runs
  - CERN organizes submissions for design prototyping and small volume production directly with the foundry.

- MPW services:
  - CERN organized MPW runs to help in keeping low the cost of fabricating prototypes and of small-volume production by enabling multiple participants to share production overhead costs.
  - CERN has developed a very good working relationships with the MPW service provider MOSIS as an alternate means to access silicon for prototyping.

MPW runs with MOSIS

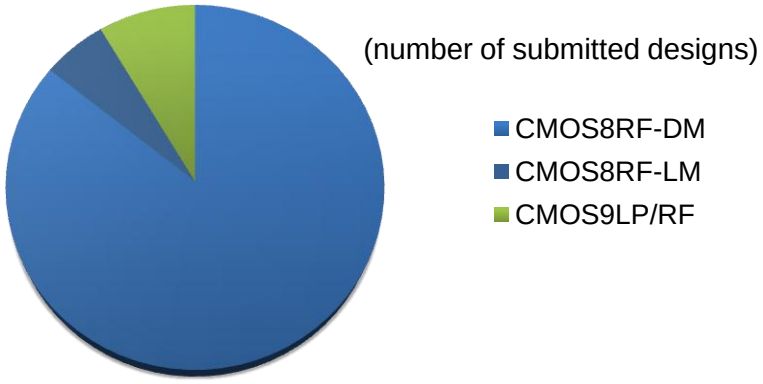
- CERN is making extensive use of the MOSIS CMOS8RF MPW runs
  - The break-even point for the cost of a CERN MPW and a MOSIS MPW is ~150mm^2.
  - Special pricing conditions for the CMOS8RF MPW services
    - MOSIS recognizes the central role of CERN in research and educational activities.
    - 40% cost reduction compared to 2008 prices
    - Waived the 10mm2 minimum order limit per submission
    - CERN appreciates the technical competence and excellent collaborating spirit with MOSIS
  - Convenience of regularly scheduled MPW runs
    - 4 runs per year scheduled every 3 months.
  - Convenience for accommodating different BEOL metallization options:
    - DM (3 thin - 2 thick – 3 RF) metal stack.
    - LM (6thin – 2 thick) metal stack.
    - C4 pad option for bump bonding.



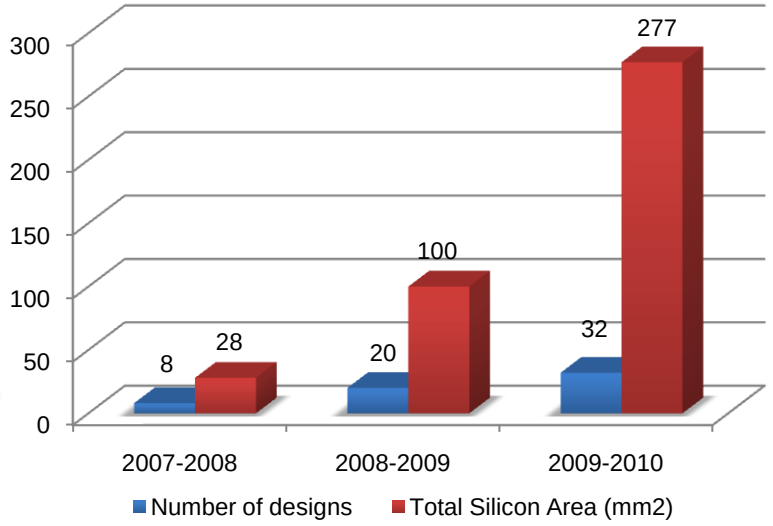
MPW activity 2009-2010

- CMOS8RF (130nm)
  - 32 designs on 6 MPW runs
    - 5 MOSIS MPW runs
    - 1 CERN organized MPW run
    - 30 designs on 8RF-DM
    - 2 designs on 8RF-LM
  - 277 mm^2 total silicon area
  - *CMOS8RF-DM (3-2-3) is the dominant metal stack option*
- CMOS9LP/RF (90nm)
  - 9 designs of 40mm^2 on 1 MPW
- CMOS8RF MPW activity for the last 3 years:

MPW activity per technology node

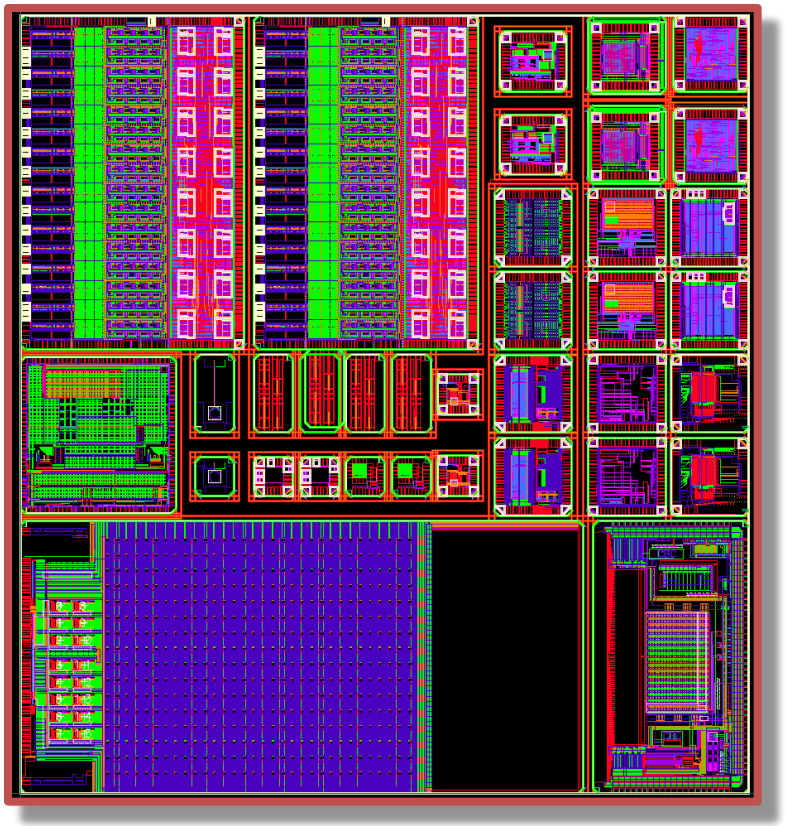


CMO8RF (130nm) Prototyping activity



CMOS8_MPW1

- CERN organized MPW
- Driven by 3 large area projects.
- 20 projects in total
- Total area: 240 mm^2
  - Small designs instantiated twice
- Cost: 2,000 USD/mm^2
- Yield: ~200 dies/project
  - More dies on request.
- Timeline:
  - Submission deadline: May 31st
  - Last Design received: July 6th
  - Tape Out to foundry: July 21st
  - Release to Manufacturing: Aug. 9th
  - Shipping of wafers: Dec. 1st
  - Effort to distribute dies before the end of the year.

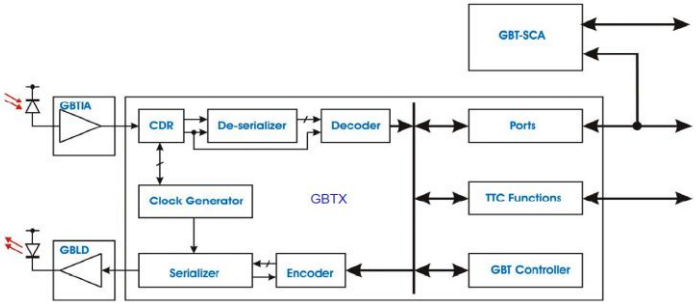


Lessons Learned

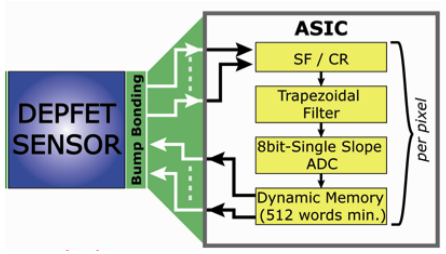
- Short IO library issues on CMOS8RF design kit V1.6
  - Inconsistencies in Verilog descriptions causing LVS problems.
  - Design Rule violations on power breaker cells.
  - Fixed on V1.7
- DRC Violations and user request for waivers.
  - Time consuming procedures with the foundry.
  - Waivers need to be well documented by designers.
  - Pattern density rules cannot be waived. Restricted use of EXCLUDE layers.
- Digital core filler cell causing PC/RX pattern density violations.
  - The “abuse” of filler cells in some designs (>50% of core area) could cause density problems.
  - A new type of filler cell that compensates pattern density is introduced in V1.7.
- Designs not conforming to declared design size.
  - Stricter policy!

Major Projects

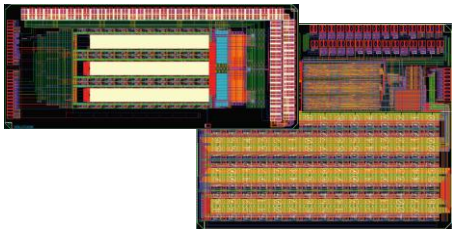
- Gigabit Transceiver Project (GBT)
  - "GBLD" Gigabit Laser Driver chip
  - "GBT-TIA"Tranimpedance Amplifier chip
  - "e-link" test chip
  - "GBTX", first prototype transceiver chip (2009Q4 MPW)



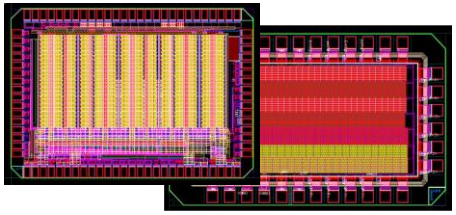
- DSSC Project for the XFEL Synchrotron Radiation Source
  - First proto with all elements in the pixel, bump test chip (2010 MPW)



- CBC: CMS Tracker Front-End ASIC
  - First prototype submitted in 2010 MPW.
- S-Altro: ALICE TPC Readout ASIC
  - First prototype submitted in 2010 MPW.

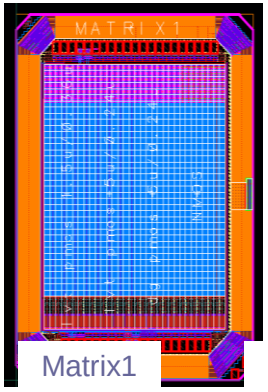


- NA62 Pixel Gigatracker detector
  - Readout test chip with ON pixel TDC cell
  - Readout test chip with End-Of-Column TDC cell
- FE-I4: ATLAS PIXEL 'b-layer upgrade'
  - Full scale prototype chip, 19x20mm2 (2010Q2 engineering run)

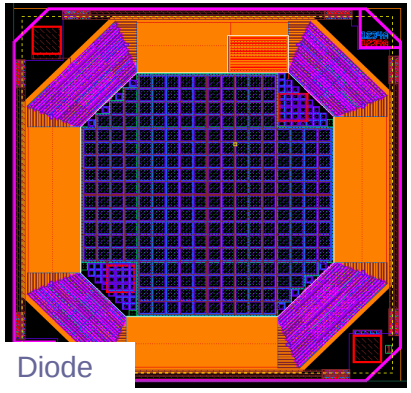


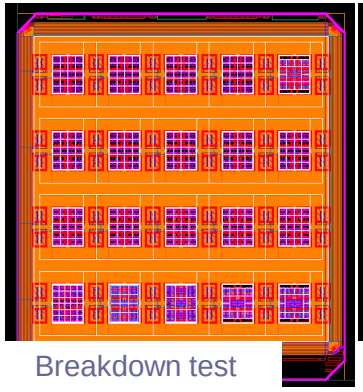
LePIX: monolithic detectors in advanced CMOS

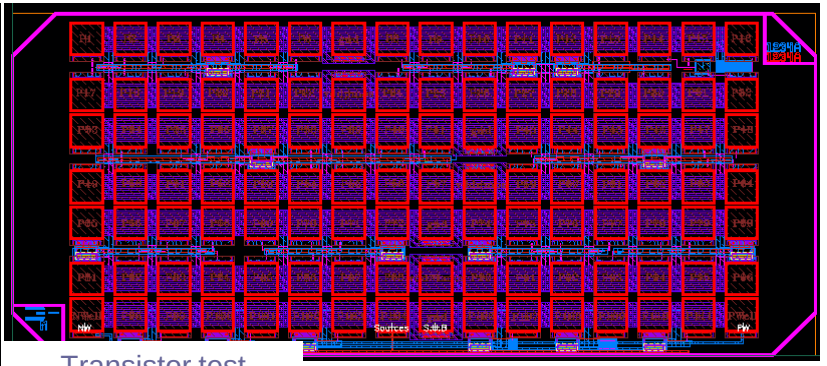
- Collaboration between CERN, MIND financed by the Haute Savoie, Alice and CMS groups (INFN Torino, Bari, Padova and IReS Strasbourg), UC Santa Cruz
- Scope:
  - Develop monolithic pixel detectors integrating readout and detecting elements on moderate resistivity substrates.
  - Reverse bias of up to 100 V to collect signal charge by drift
- 7 chips submitted in first submission :
  - 4 test matrices, 1 diode for radiation tolerance,1 breakdown test structure,1 transistor test: already submitted once in test submission
- First project in CMOS9LP/RF (90nm) on special substrates.
- Requires direct communication links with a number of technology specialist in the foundry.



Matrix1


Diode


Breakdown test


Transistor test

Courtesy of Walter.Snoeys@cern.ch

Call for Interest

- Please contact us for participation in:
  - Forthcoming MPW runs:
    - **CMOS6 (250nm)**
      - Tape Out beginning of next year.
      - Support for 3 and/or 6 metal stacks.
    - **CMOS8RF (130nm)**
      - MOSIS Nov. 8, 2010
    - **CMOS9LP/RF (90nm)**
      - MOSIS Dec. 8, 2010
  - Forthcoming AMS Workshops
    - Week of Oct. 18-22
    - End of 2010
- Contact: kostas.kloukinas@cern.ch, evelyne.dho@cern.ch

THANK YOU

Reminder for MUX-2010

Microelectronics Users eXchange MUX-2010

To be held at CERN, October 21-22, 2010

http://indico.cern.ch/event/MUX2010

The MUX2010 is the first of a new generation of meetings popular in the HEP community in the late 90's under the name of MUG. It is organized as a series of educational and information exchange seminars given by experts in industry and from our community on a variety of topics related to microelectronics design for HEP applications.

Preliminary programme:

Thursday, October 21

9:00 Welcome and Introduction – A. Marchioro, CERN
9:15 3D Silicon integration – J. Knickerbocker, IBM
11:30 Applications of 3D techniques for HEP – S. Vaehaenen, CERN/VTT

14:00 Integrated Power Conversion – S. Saggini, U. of Udine
16:00 Tool challenges at 65nm and below - W. Stronski, Cadence
17:15 Discussion Session: "What do we need next in HEP?"

Friday, October 22

9:00 Designing MEMS Sensors – G. Henriet, ST
11:00 Comparing 130 and 90nm for FE designs - J. Kaplon, CERN

14:00 Analog Design at 90nm and below - A. Baschirotto, U. of Milano
17:15 Feedback and Wrap-Up

Participation registration is mandatory but free of charge. For the registration, please go to the web site above.
Enquiries concerning the workshop programme and participation can be directed to the Workshop Secretariat, by emailing Evelyne.Dho@cern.ch.

Organised by: CERN, the European Organization for Nuclear Research and ACEOLE, a Marie Curie Action at CERN
funded by the European Commission under the 7th Framework Programme.

SPARES

Wrap-Up

- Technology support & foundry services.
  - Provide standardized common design kits and design flows.
  - Provide access to advanced technologies by sharing expenses.
  - Organize common Training and Information sessions.
  - Collective activities help to minimize costs and effort.

- Availability of foundry and technology services is modulated by user's demand.
  - Your feedback is Welcomed.

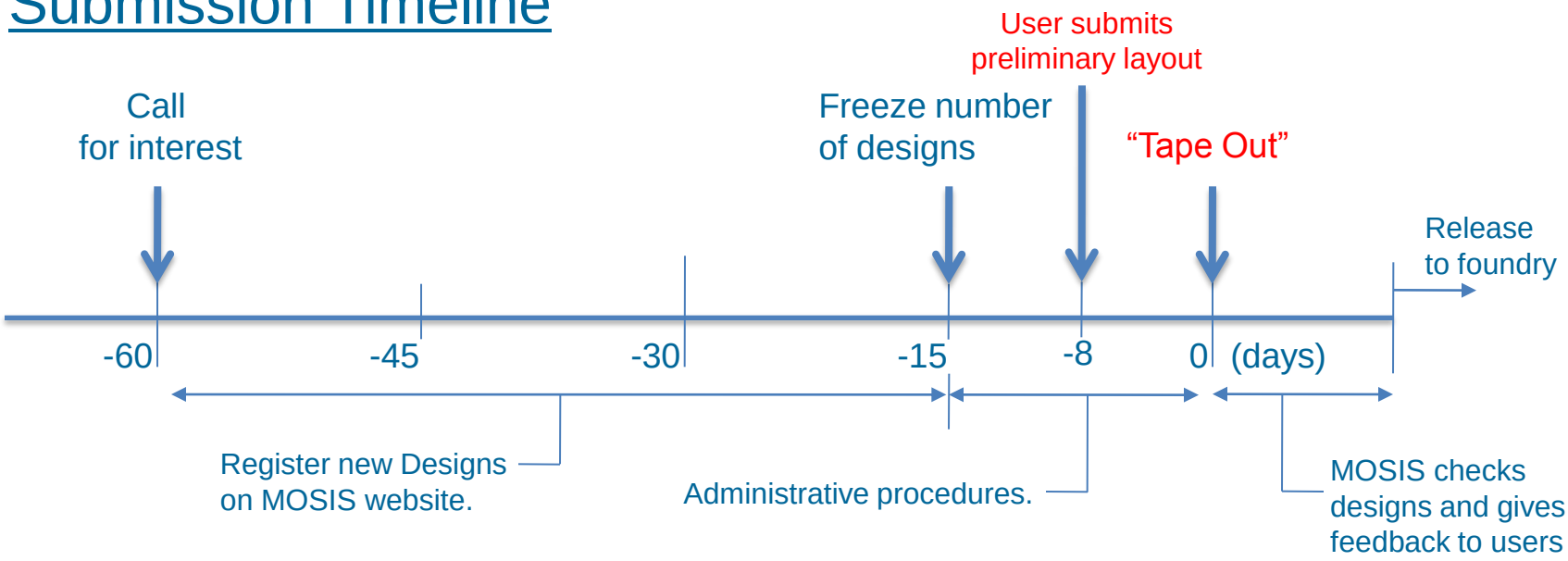
- Contact Details:
  - Foundry services & Technology support:
    - Kostas.Kloukinas@cern.ch
  - Access to design kits and installation support:
    - Bert.van.Koningsved@cern.ch
  - Technical support (Front End & Back End workflows):
    - Wojciech.Bialas@cern.ch , Sandro.Bonacini@cern.ch

Future Plans

- Maintenance of the CMOS8RF (130nm) kit.
- Development of a Design Kit for the CMOS9LP/RF (90nm)
  - Standard cell library (limited number of cells).
  - Design Workflows similar to those in the CMOS8RF Design Kit.
- Investigate access to 65nm technologies
  - Evaluation for SLHC environment
  - Access to libraries and IP blocks.

Fabricating through MOSIS

Submission Timeline

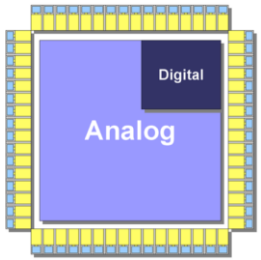


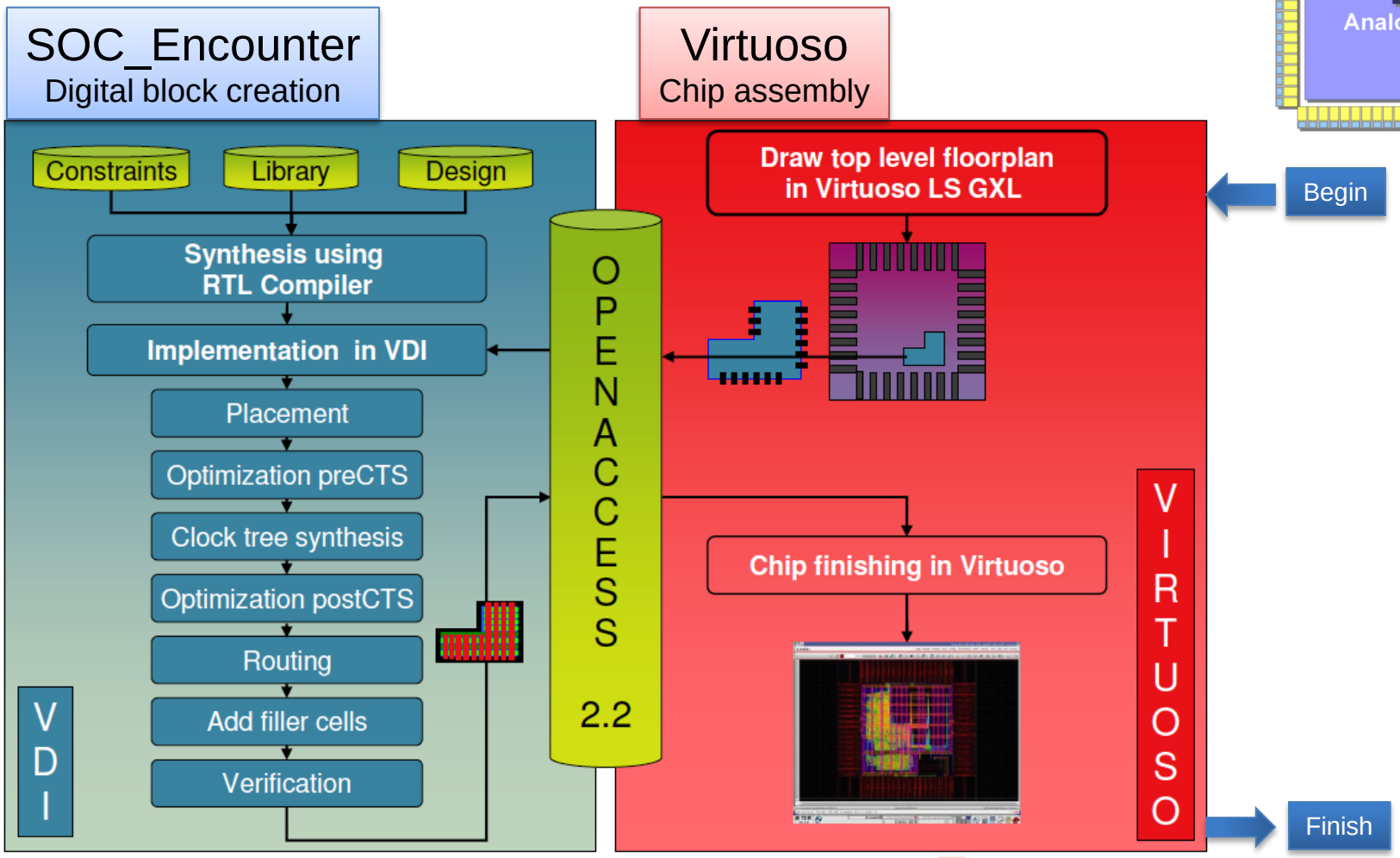
- Turn Around Time: ~70 calendar days from release to foundry
- Number of prototypes: 40 pieces

"Analog on Top" Design Flow

Chip Finishing in Virtuoso

For big 'A' small 'D' designs.

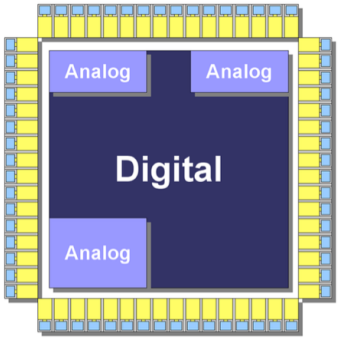




"Digital on Top" Design Flow

Chip Finishing in SOC_Encounter

For big 'D' small 'A' designs.



Virtuoso
Analog Block Creation

SOC_Encounter
Chip Design

Automated task
User task

RTL synthesis
Logical Equivalence Checking
Floorplanning & power routing
Placement
Congestion analysis
Timing optimization
Clock tree synthesis
Timing optimization
Routing
Timing optimization
DFM
Signoff RC extraction
Timing analysis
Logical Equivalence Checking
DRC
LVS
Tape-out

Open Access

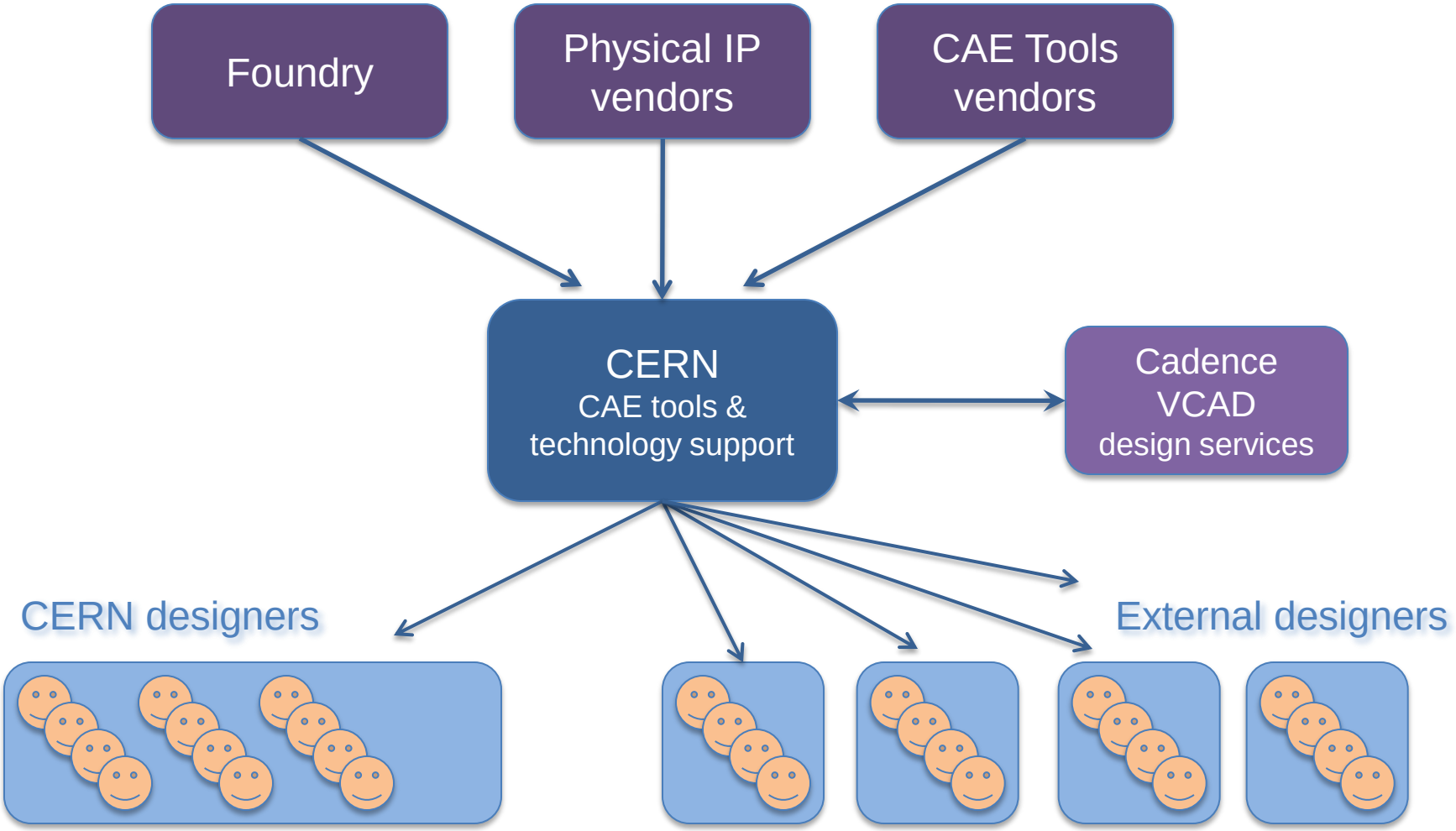
Access to Technology Data

- Distributed by CERN

Technology	Process	Distributable
CMOS8RF-LM	130nm	IBM PDK, Design Kit
CMOS8RF-DM	130nm	IBM PDK, Design Kit
BiCMOS8WL	130nm (SiGe)	IBM PDK
BiCMOS8HP	130nm (SiGe)	IBM PDK, IBM PDK
CMOS9SF	90nm	

- IBM PDK : Physical Design Kit for Analog full custom design.
- Design Kit : Design Kit that supports Analog & Mixed Signal design.

Technology Support Services



Foundry Access Services