Radiation-Hard ASICS for Optical Data Transmission in the First Phase of the LHC Upgrade

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Outline

- Introduction
- Result on VCSEL Driver Chip
- Result on PIN Receiver/Decoder Chip
- Summary

IBL

- ATLAS proposed to add one more layer to the current pixel detector:
  - "Insertable B-Layer" or IBL
  - installation ~ 2015-6
  - optical links will use VCSEL/PIN array as in current pixel detector
  - an updated version of current driver (VDC) and receiver (DORIC) with redundancy and individual VCSEL current control would be a logical improvement
    - experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for SLHC
      - ⇨ submission of 1st prototype chip (130 nm) in 2/2010

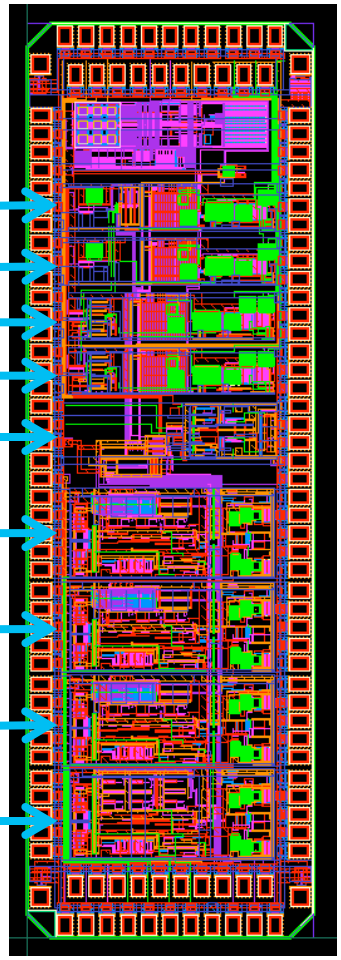
Chip Content

Design

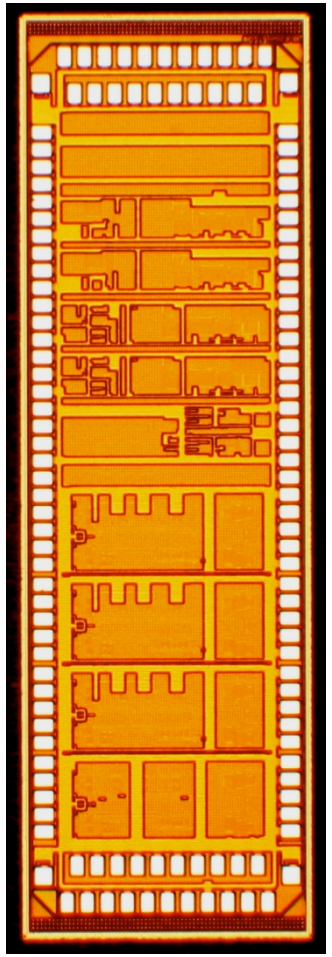
Photo

VCSEL Driver (spare)
VCSEL Driver
VCSEL Driver with pre-emphasis
VCSEL Driver with pre-emphasis
CML Driver with pre-emphasis

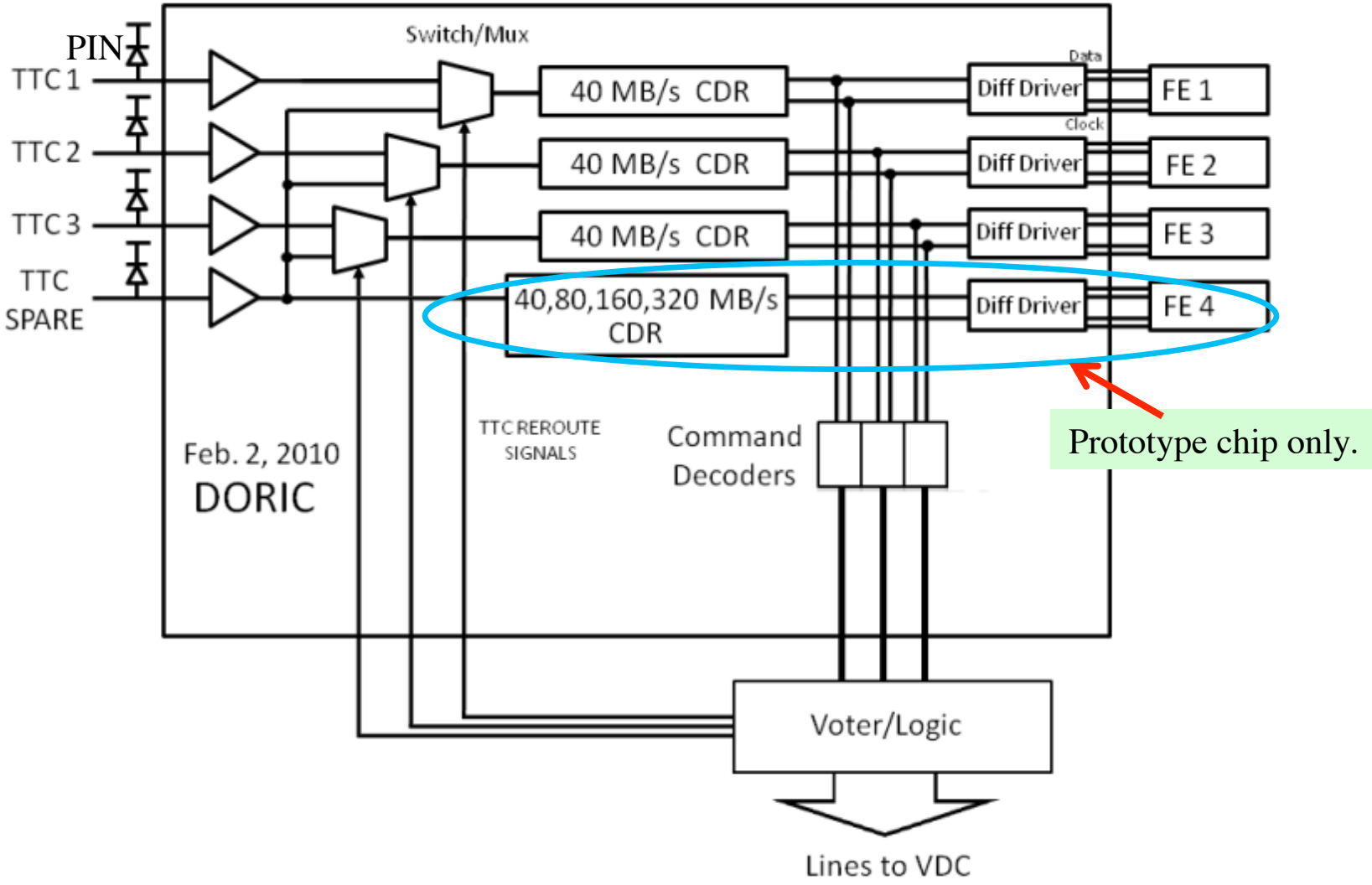
Decoder (40Mb/s)
Decoder (40Mb/s)
Decoder (40Mb/s)
Decoder (40/80/160/320 Mb/s, spare)



1.5 mm



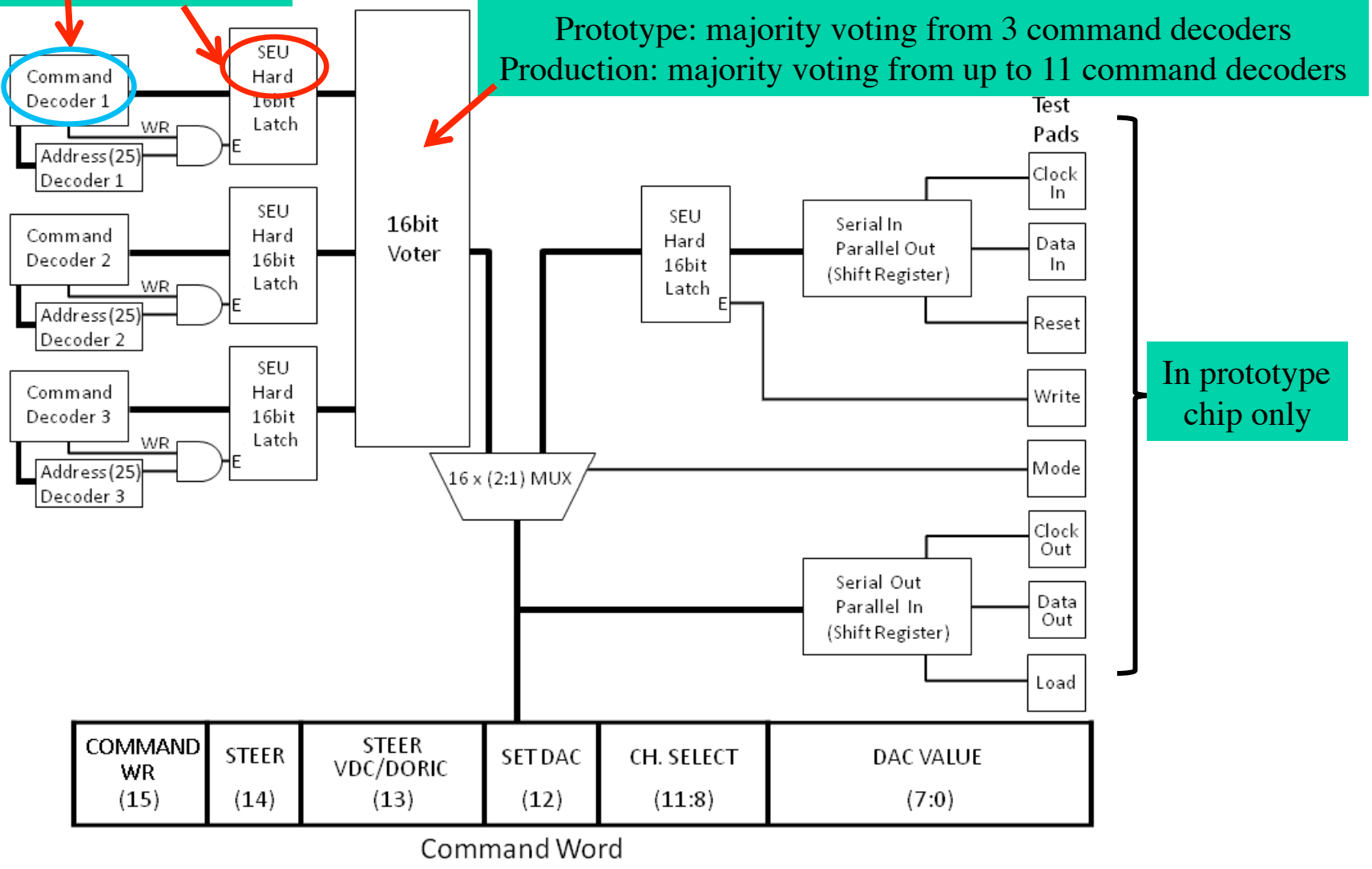
PIN Receiver/Decoder



Command Decoder Interface

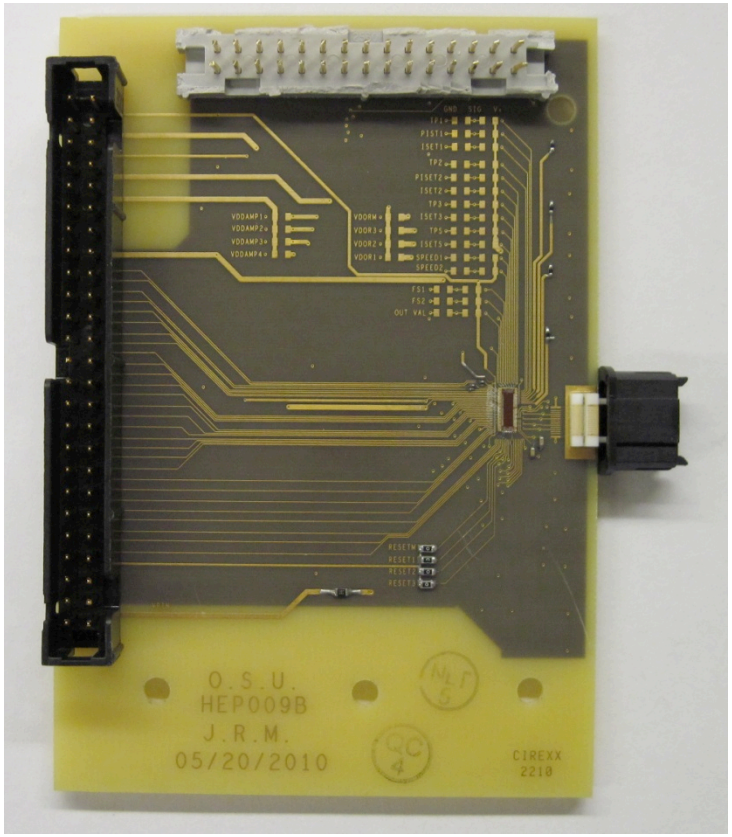
Courtesy of FE-I4 of IBL

Prototype: majority voting from 3 command decoders
Production: majority voting from up to 11 command decoders



Test Card

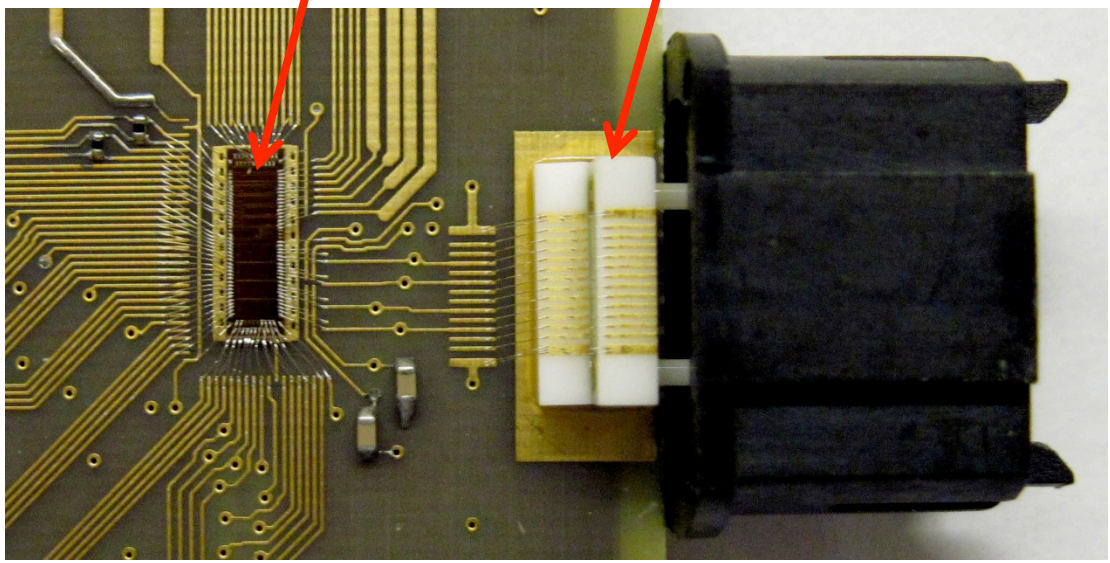
Test card



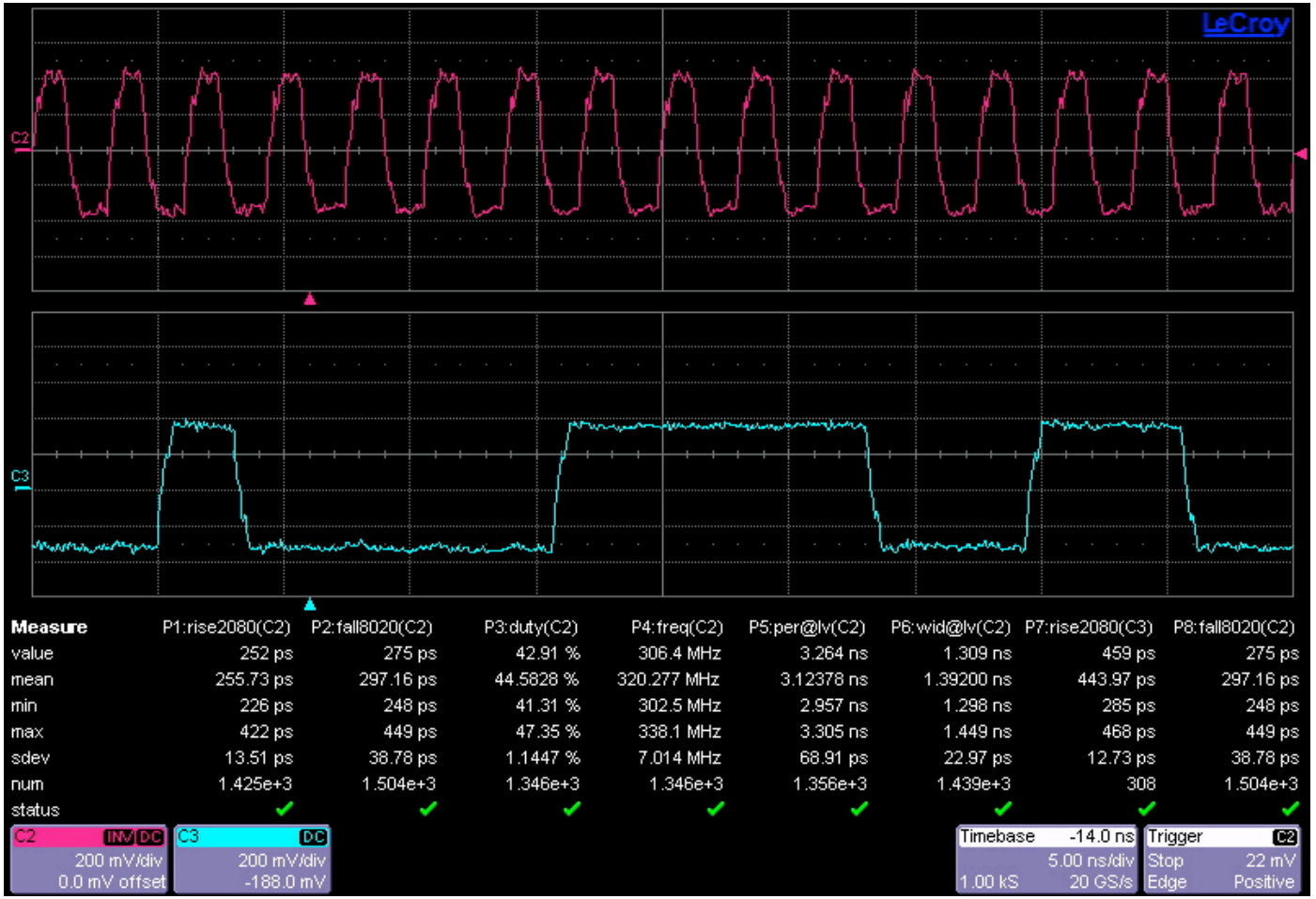
PIN opto-pack

ULM 5 Gb/s

chip



Recovered Clock/Data



320 Mb/s

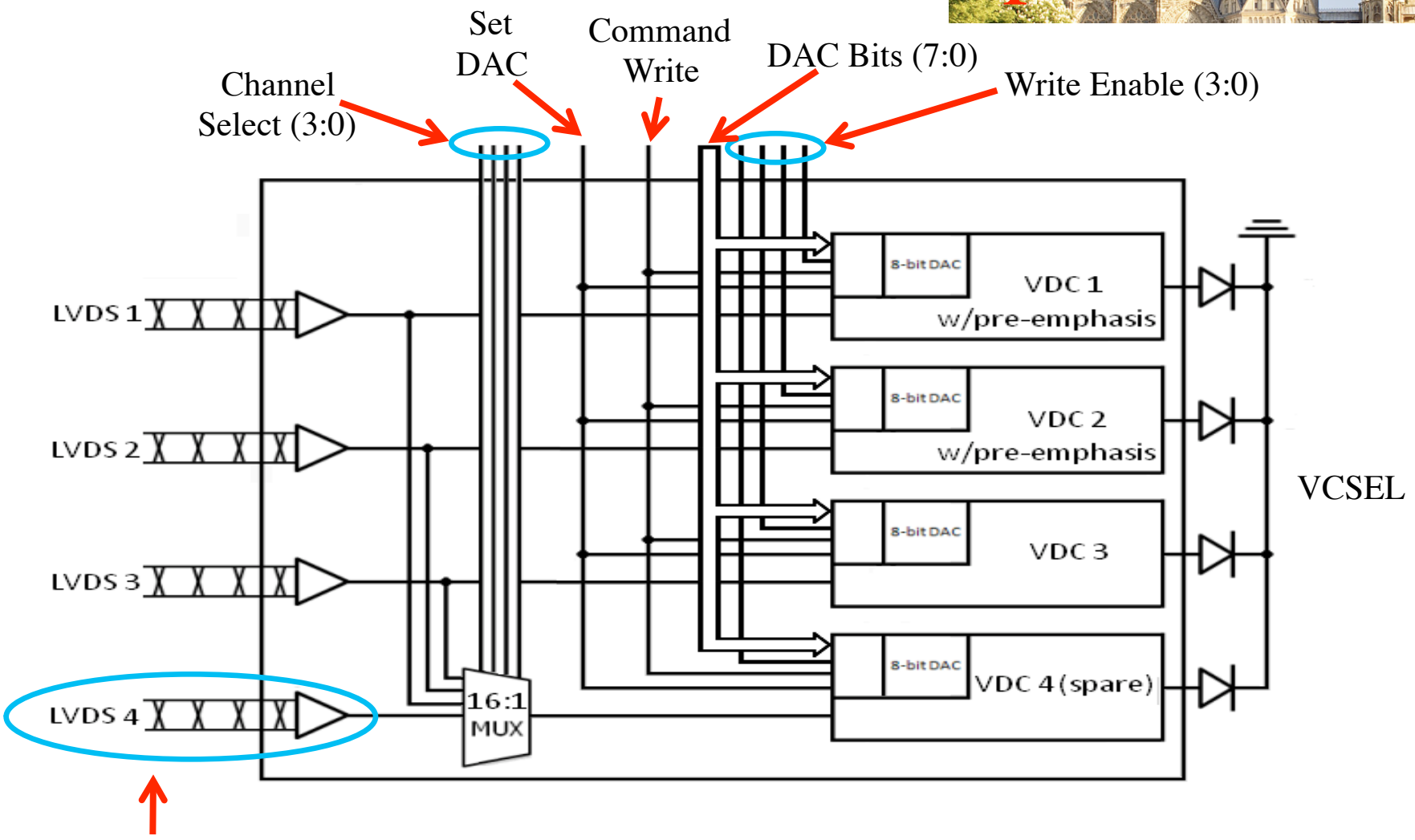
Jitters/Thresholds

- Peak-to-peak clock jitter:
  - 40 Mb/s: 132 ps (normal)
  - 40 Mb/s: 1420 ps (multi speed)
  - 80 Mb/s: 750 ps
  - 160 Mb/s: 193 ps
  - 320 Mb/s: 103 ps
- Threshold for no bit errors:
  - 40 Mb/s:
    - Multi speed: 40 μA
    - Ch 1: 19 μA
    - Ch 2: 22 μA
    - Ch 3: 20 μA
  - 80 Mb/s: 58 μA
  - 160 Mb/s: 74 μA
  - 320 Mb/s: 110 μA

PIN Receiver/Decoder

- ✔ All channels work at 40 Mb/s
- Multi Speed version works at 40, 80, 160, and 320 Mb/s
  - 160 and 320 Mb/s need external bias tuning for proper operation
- ✔ Steering signal to the spare channel works

VCSEL Driver Chip



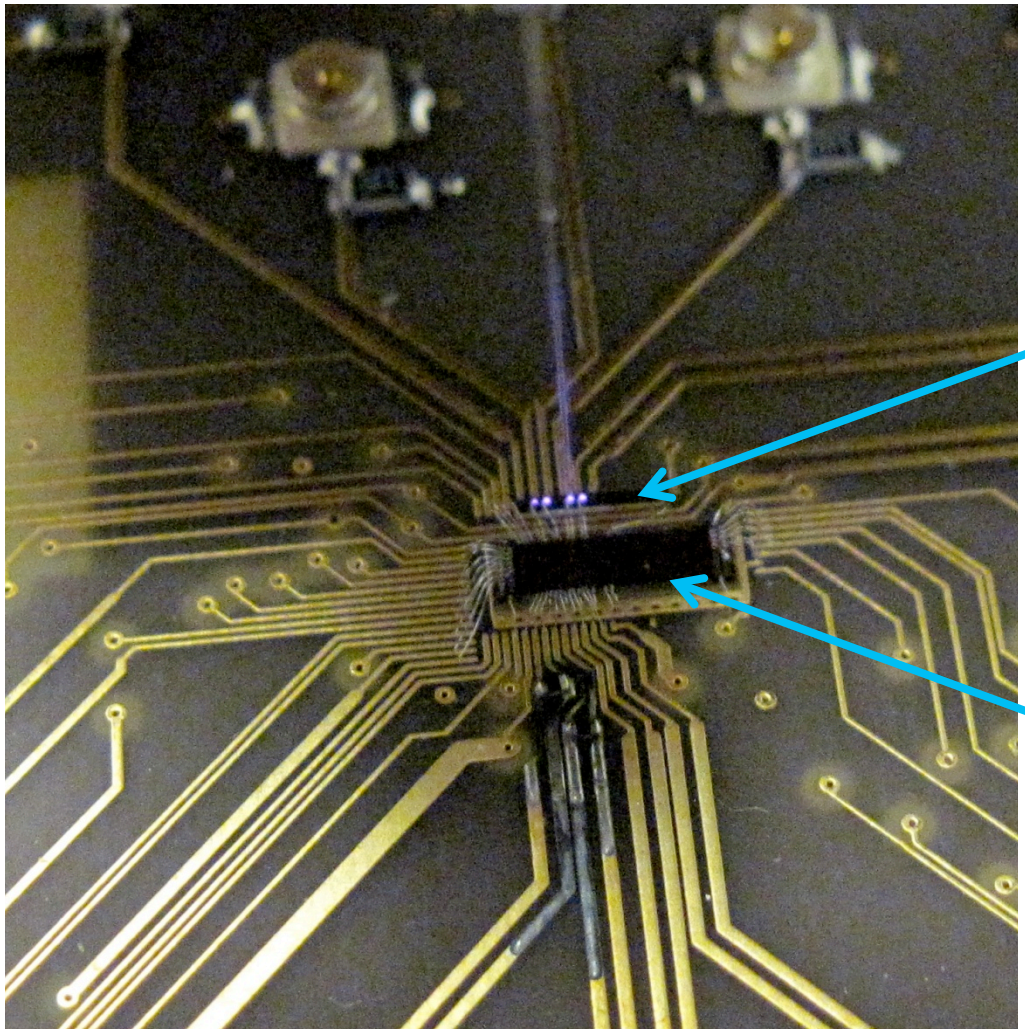
LVDS input added for prototype chip only.

VDC Results

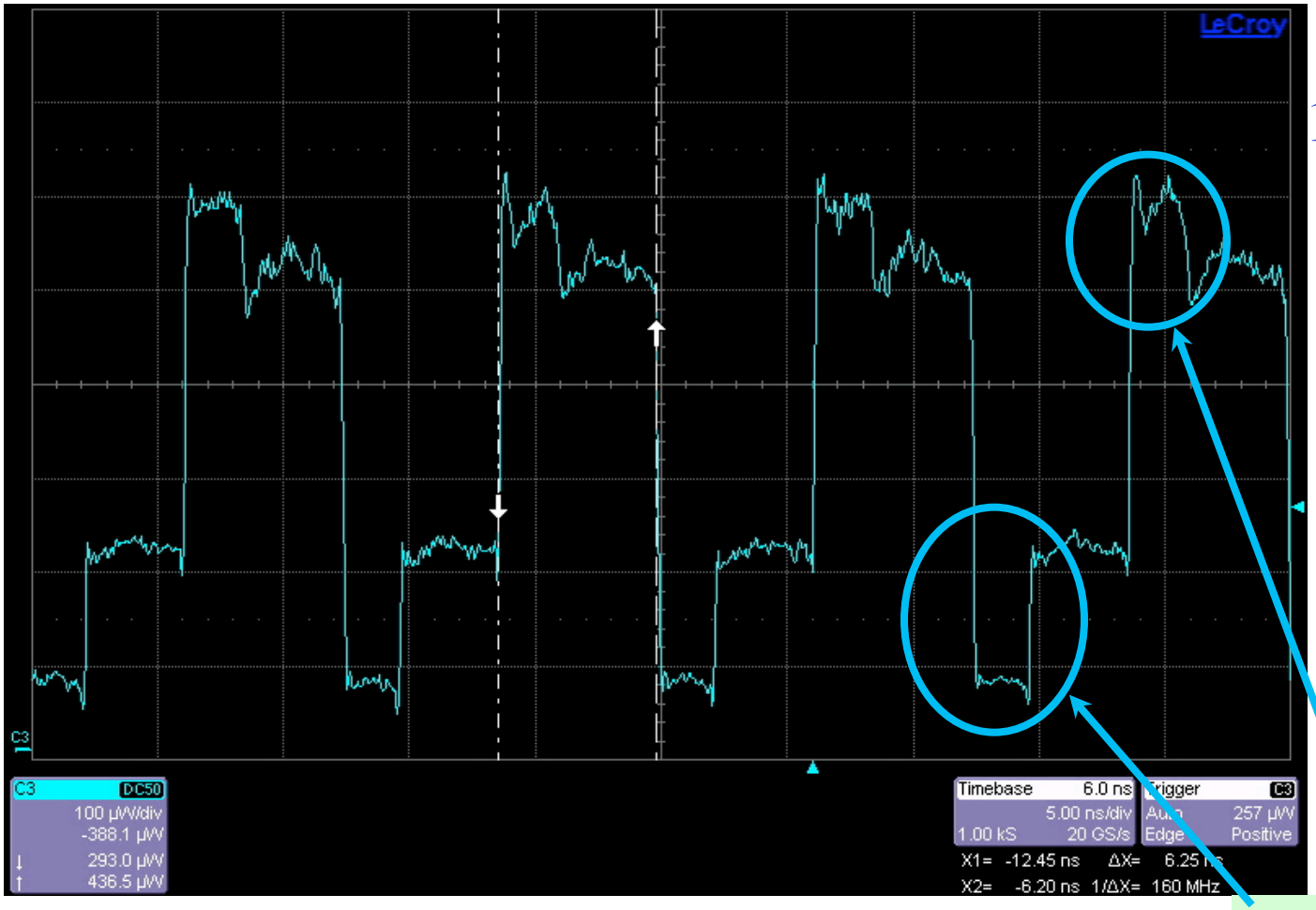
- Power-on reset circuit
  - an open control line disables 6 opto-links in current pixel detector
    - ⇨ implemented power-on reset circuit in prototype chip
    - ✔ chips power up with several mA of VCSEL current
- Test port
  - ✔ can steer signal received to spare VDC/VCSEL
  - ✔ can set DAC to control individual VCSEL currents
- ✔ All 4 channels run error free at 5 Gb/s
  - ✔ includes the spare with signal routed from the other LVDS inputs

VDC Test Setup

- Light from the 4 VCSELs:
  - Fiber aligned over VDC/VCSEL 2

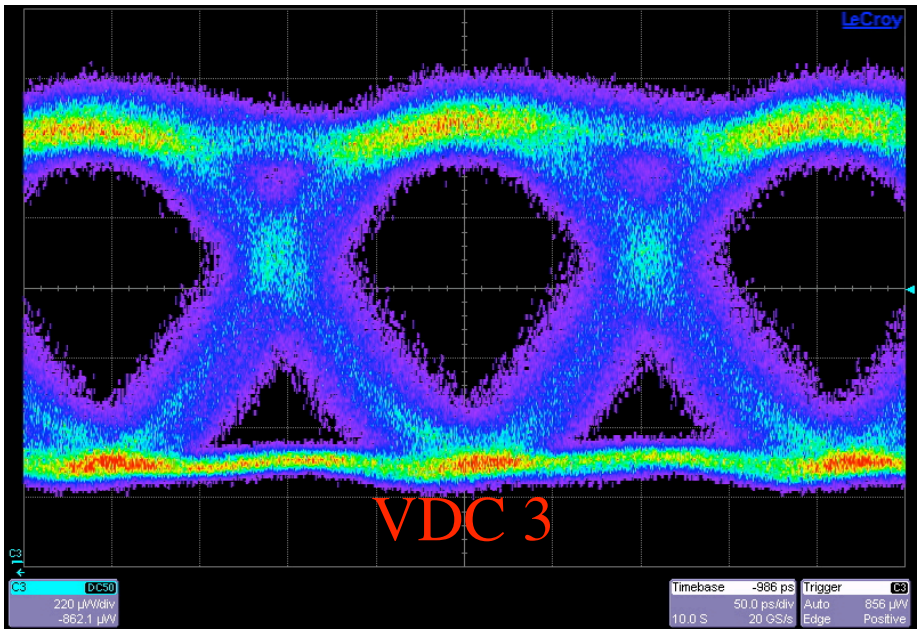


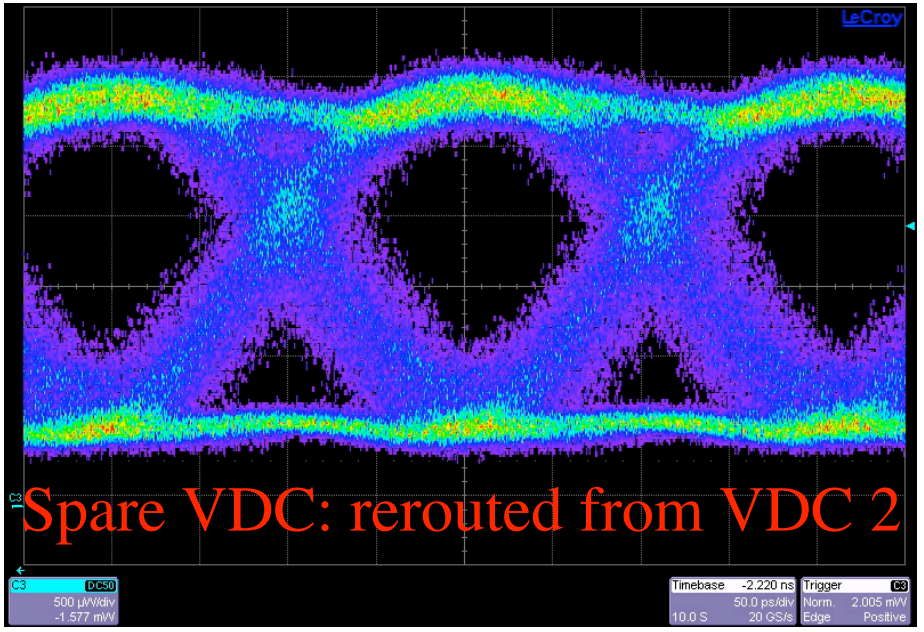
VCSEL Driver with Pre-Emphasis



✔ Pre-emphasis working with tunable width and height

Eye Diagrams @ 4.8 Gb/s



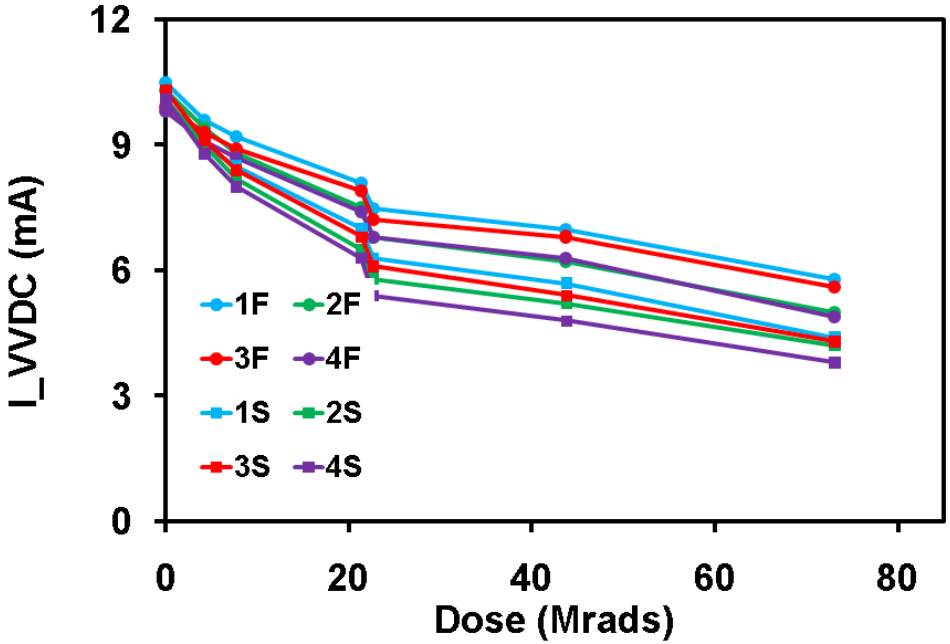


- No pre-emphasis
- Rise/fall times: ~60-90 ps
  - Measured with 4.5 GHz optical probe
- Bit error rate < 5×10^{-13}

Irradiation

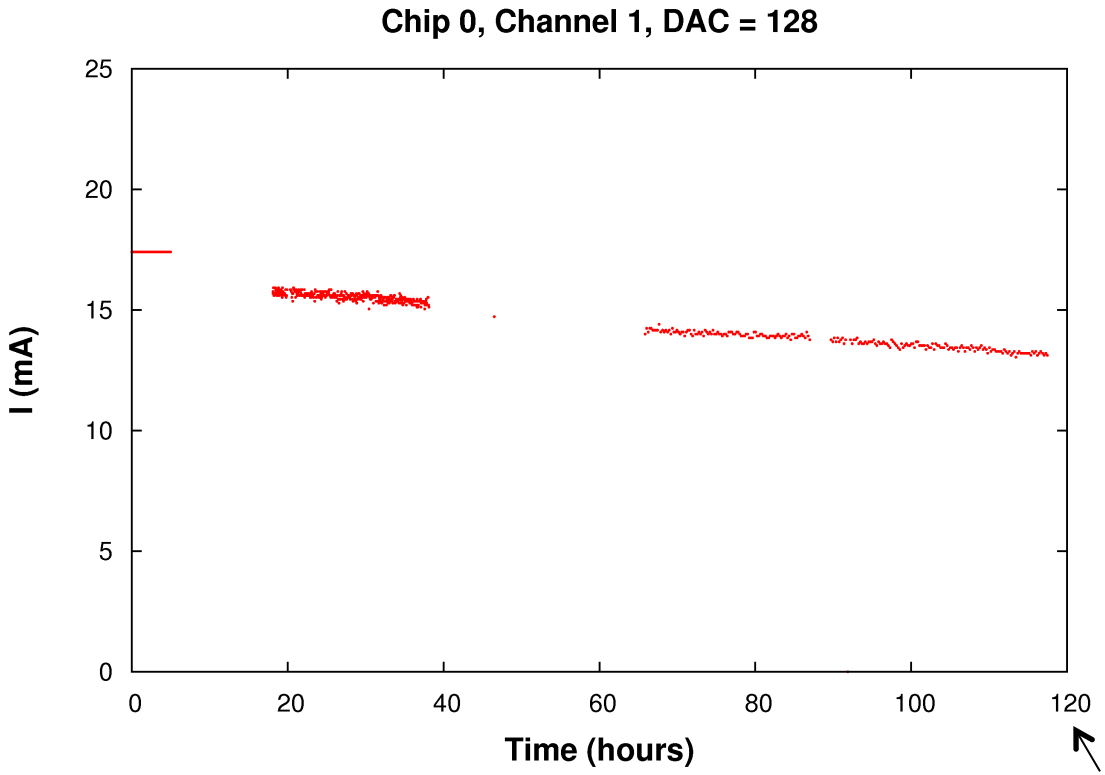
- 2 chips were packaged for irradiation with 24 GeV/c protons at CERN in August
  - each chip contains 4 channels of drivers and receivers
  - total dose: 1.6 x 10^{15} protons/cm^2
  - all testing are electrical to avoid complications from degradation of optical components
    - ⇨ long cables limited testing to low speed
  - ✔ observe little degradation of devices
    - evaluation of full performance await return of devices to labs

VDC Irradiation 2009



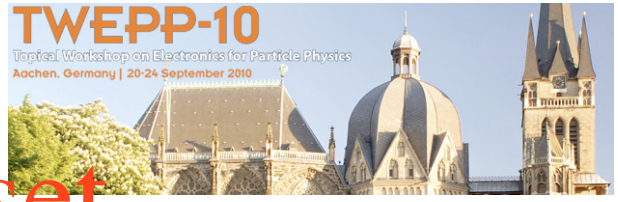
- Previous VDC prototypes (130 nm) were irradiated in 2009
- VDC driving 25 Ω with constant control current
- drive current decreases with radiation for constant
  - driver circuit fabricated with thick oxide process
  - PMOS and NMOS have different threshold voltage shifts
  - ⇨ use only PMOS in the current mirror in 2010 prototype

VDC Irradiation 2010



1.6×10^{15} p/cm^2

- new VDC also drives 25 Ω with constant control current
- Decrease in drive current is small!



Single Event Upset

- SEU harden latches or DAC could be upset by traversing particles
  - 40 latches per 4-channel chip
  - SEU tracked by monitoring the amplitude of VDC drive current
  - 13 instants (errors) of a channel steered to a wrong channel in 71 hours for chip #1
    - similar upset rate in chip #2
    - ⇨ $\sigma = 3 \times 10^{-16}\ cm^2$
    - particle flux $\sim 3 \times 10^{9}\ cm^{-2}$/year @ opto-link location
    - ⇨ SEU rate $\sim 10^{-6}$/year/link

Summary

- prototyped opto-chip for 2nd generation ATLAS pixel opto-links incorporated experience gained from current links
  - add redundancy to bypass broken PIN or VCSEL channel
  - add individual VCSEL current control
  - add power-on reset to set VCSEL current to several mA on power up
  - ✔ VCSEL driver can operate up to ~ 5 Gb/s with BER < 5×10^{-13}
  - ✔ PIN receiver/decoder properly decodes signal with low threshold
  - ✔ little decrease in VCSEL driver output current
  - ✔ very low SEU rate in latches/DAC
  - ✔ all added functionalities work!

All results are preliminary