Digitization and Real-Time Analysis of Detector Signals with GANDALF

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TWEPP 2010

Outline

- New Recoil Proton Detector at COMPASS
- Requirements on front-end electronics
- The GANDALF Module
- Measurements with GANDALF
- Further applications of GANDALF

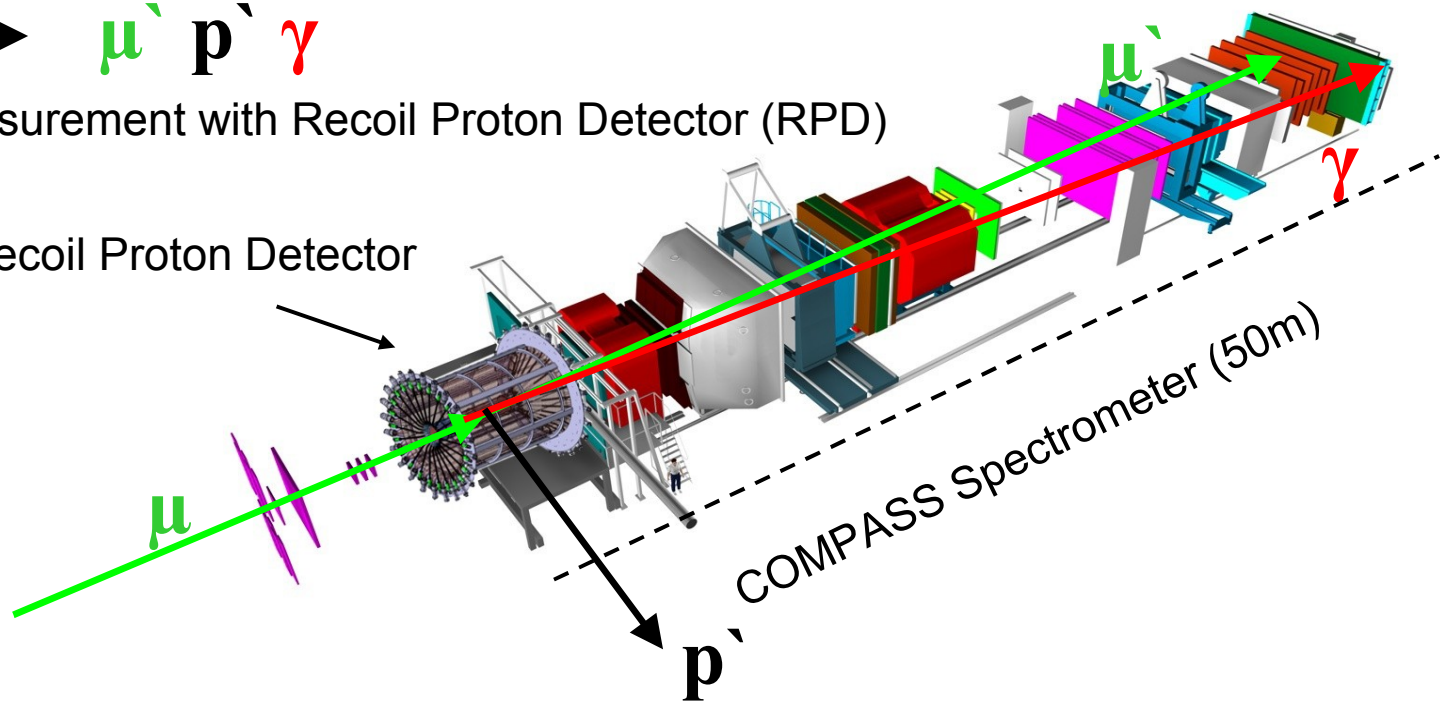
COMPASS Phase II: Generalized Parton Distributions (GPDs)

Understanding the spin of the proton:

- Information about the total angular momentum of constituents from GPDs
- Generalized Parton Distributions from Deep-Virtual Compton Scattering (DVCS)

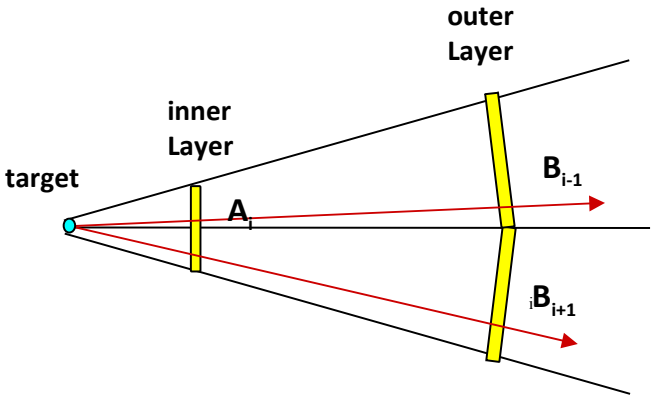
$$\mu\, p \longrightarrow \mu'\, p'\, \gamma$$

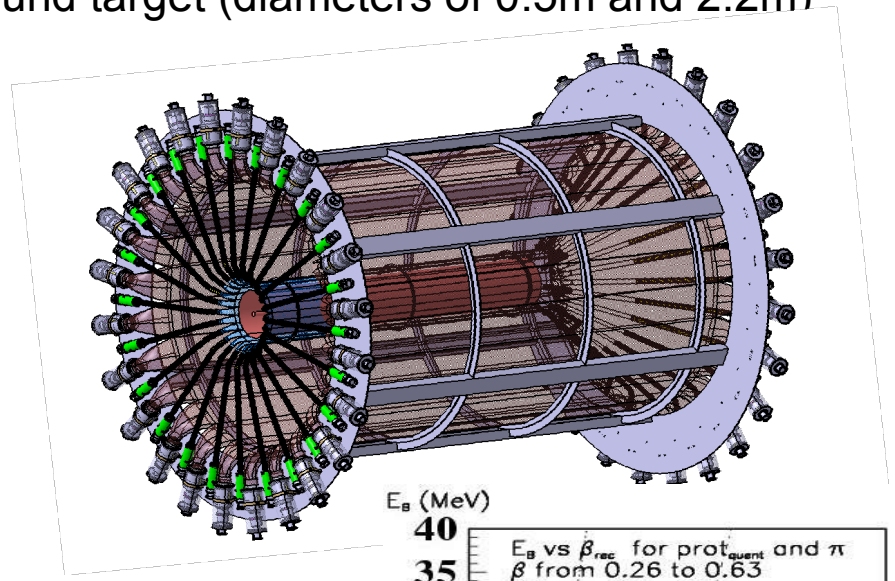
- Exclusive measurement with Recoil Proton Detector (RPD)

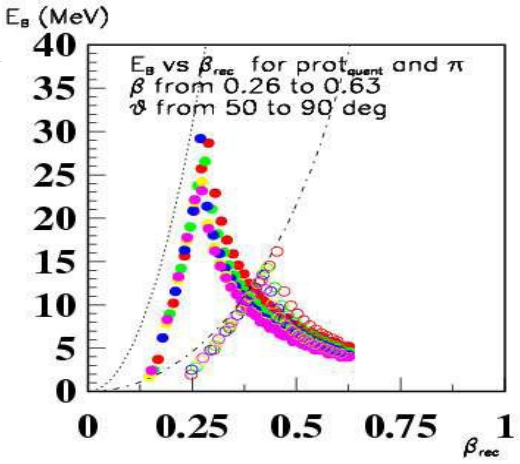


Detection of the Recoil-Proton

- Liquid Hydrogen Target in the center of the Recoil Proton Detector
- Two barrels of scintillating slats around target (diameters of 0.5m and 2.2m)
- Readout at both ends of every slat





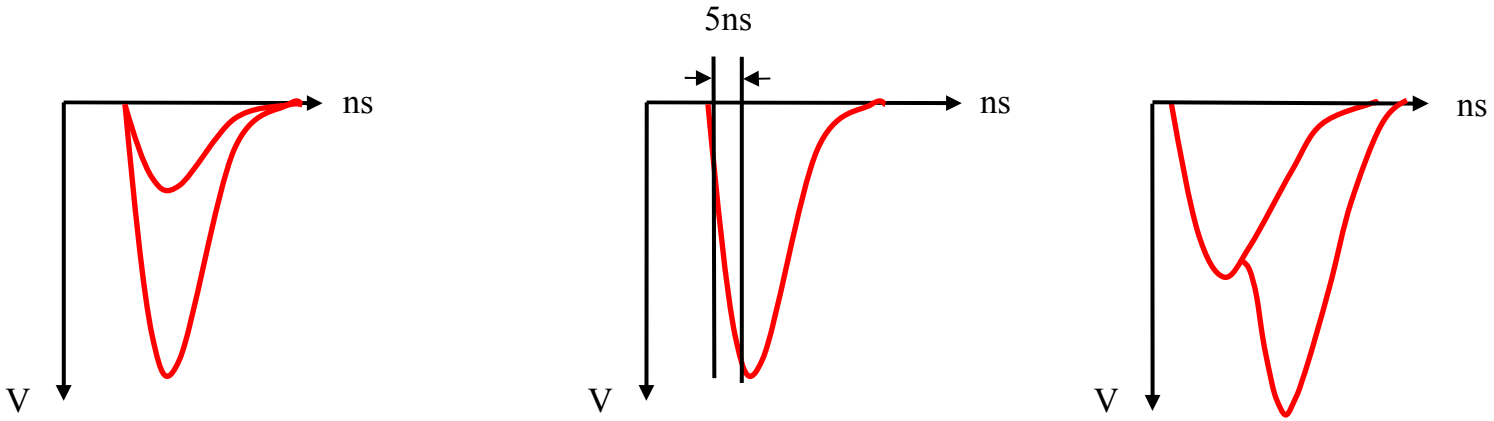


Setup allows

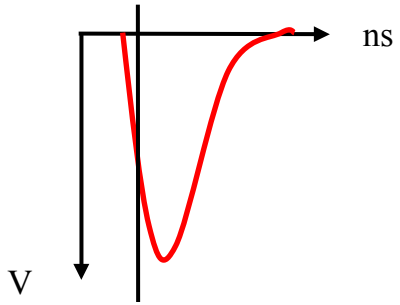
- Particle Identfication with time-of-flight and dE/dx
- Coverage of full proton kinematics

Requirements for Proton Detection

- Digitization of PM-signals with different amplitudes, short rise-times, double pulses

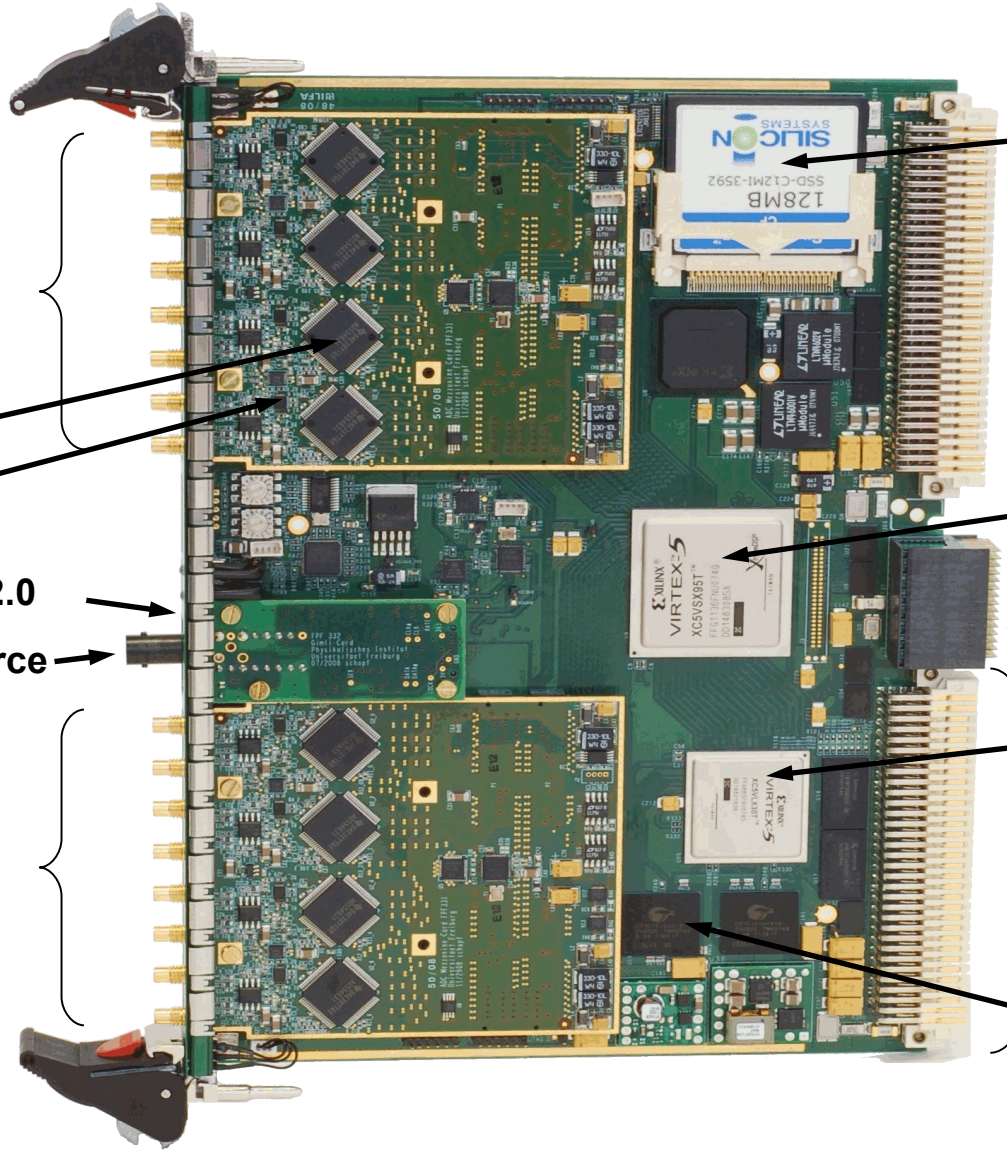


- Time resolution of σ ≤ 200 ps for amplitudes from -4V to -50 mV



- Real-time processing and high-speed transmission of data for Proton Trigger Generation

The GANDALF Module



8 analog inputs on Analog Mezzanine Card

12 bit ADC (500 MHz)

16 bit DAC

USB 2.0

TCS input & clock source

8 analog inputs on Analog Mezzanine Card

8 GB CompactFlash

VME64x interface

Virtex-5 SXT FPGA

VXS interface

Virtex-5 LXT FPGA

S-Link interface

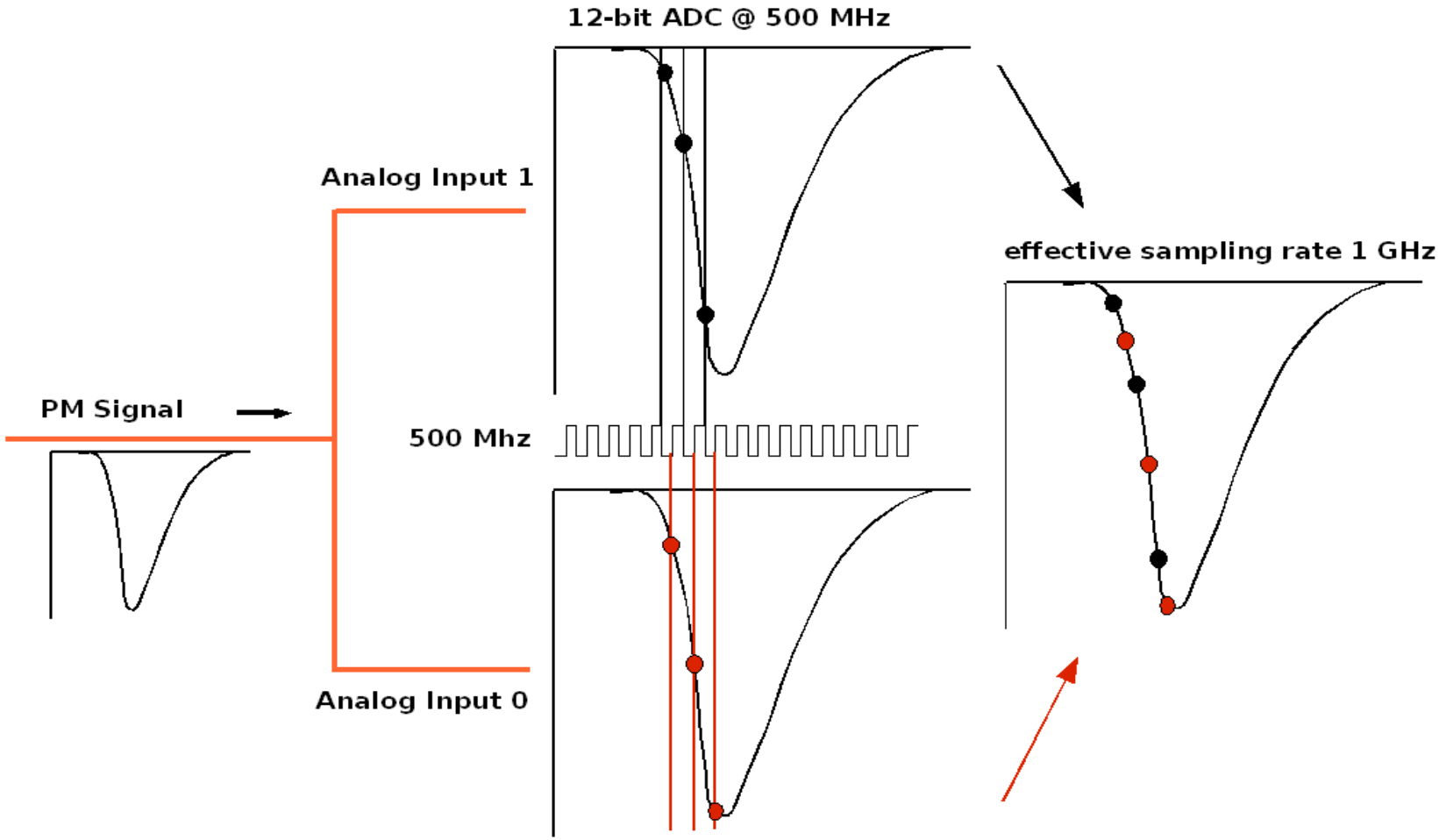
144 Mbit QDR II+ RAM

4 GBit DDR2 RAM

Time-Interleaved Mode

- Analog Signal is split and directed to two Analog Inputs 0 and 1
- 180° Phase-shift between corresponding sampling clocks

effective sampling rate of 1 GHz

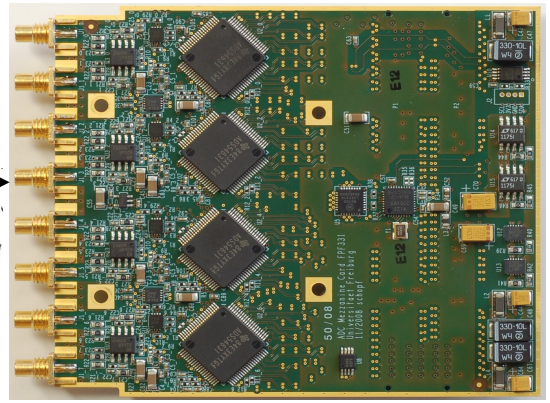


Quality of Digitization

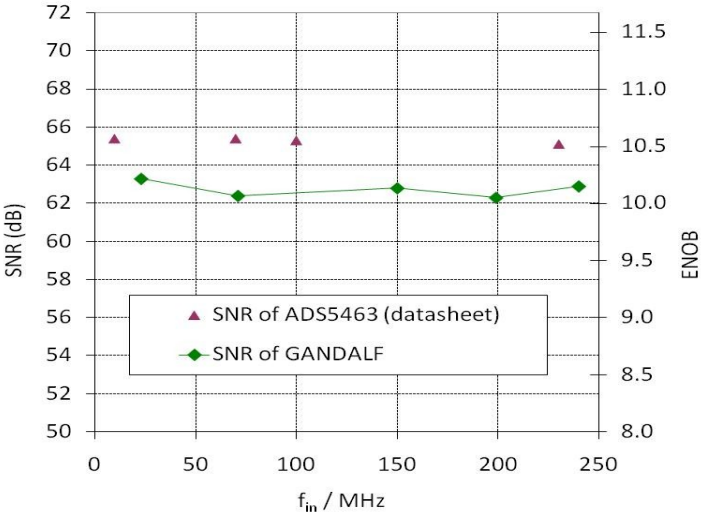
- Required Effective Number of Bits (ENOB) : ENOB ≥ 10 bit
- ENOB of 12-bit ADC ADS5463 (TI): ENOB = 10.4 bit
- ENOB measurement with signal path and ADC over full input bandwidth

N = (SNR - 1.76) / 6.02 (N: effective bits, SNR: Signal-to-noise ratio in dB)

sine wave

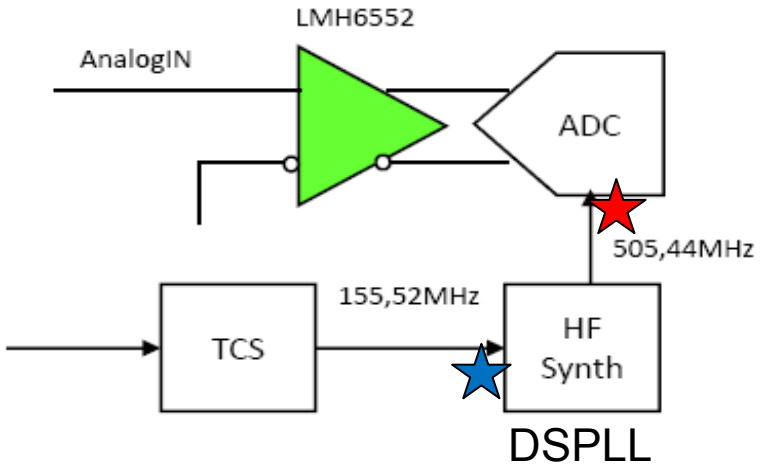


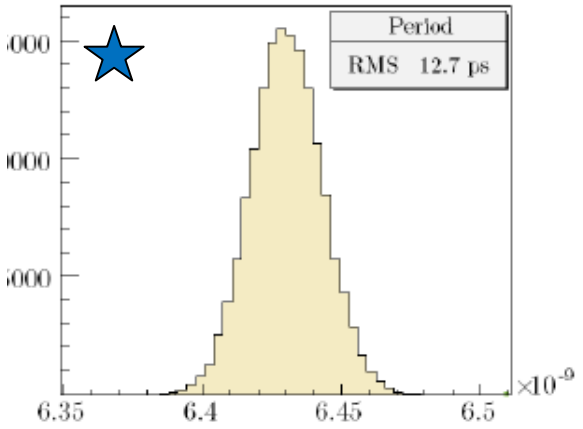
Fast-Fourier Transformation of data



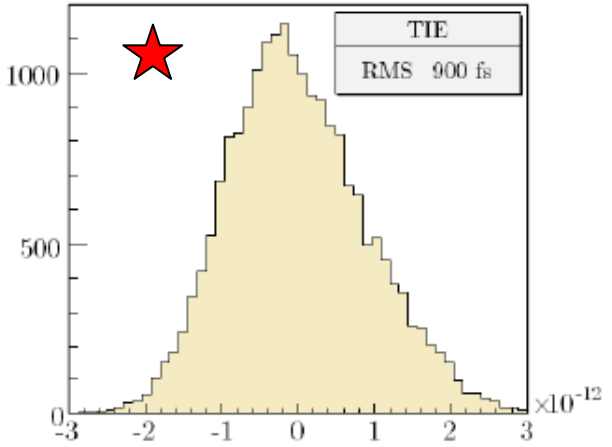
ENOB > 10 over full bandwidth

Performance of the sampling clock





Period Jitter (RMS 12.7 ps)

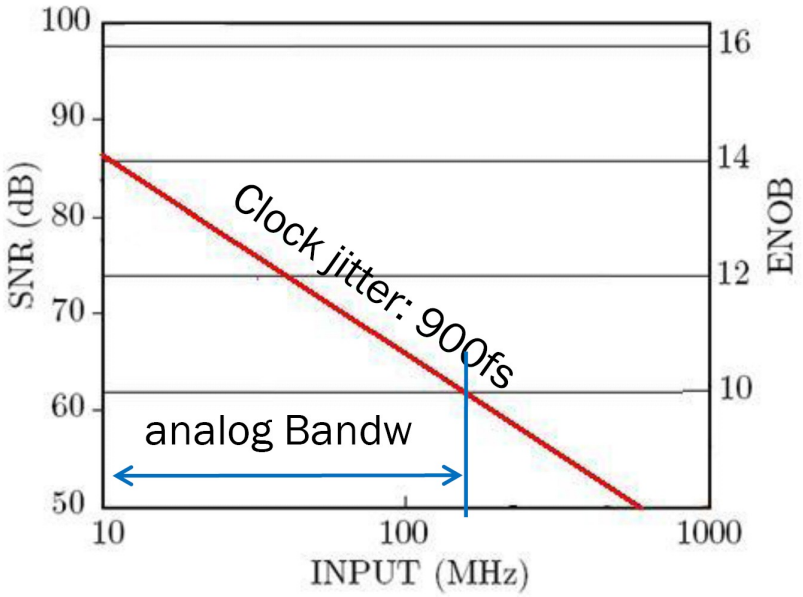


Time Interval Error (RMS 900 fs)

Sampling Clock Generation:

- 155.52 MHz Clock Extraction from TCS
- Digital Clock Multiplication to 505.44 MHz

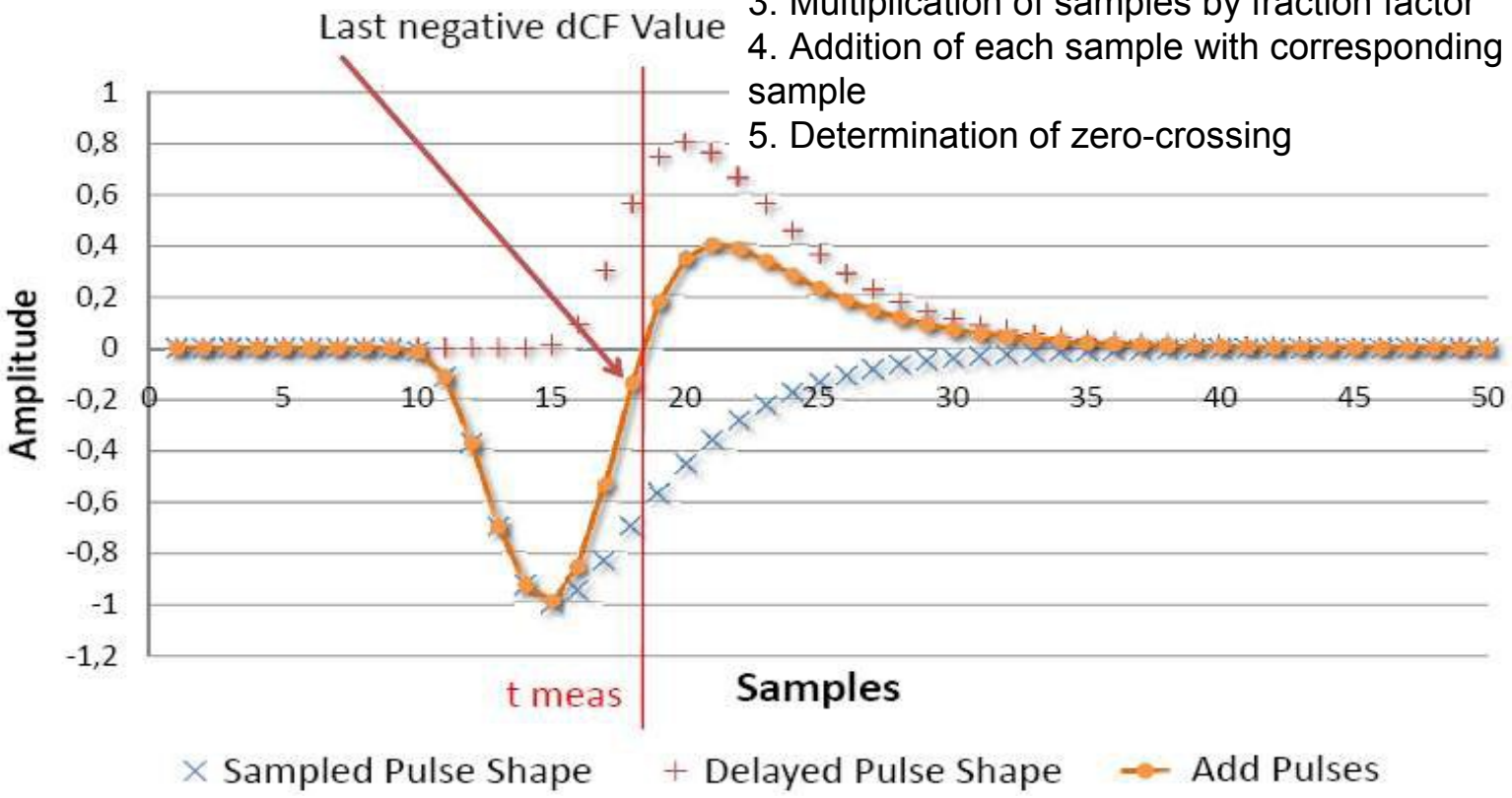
➡ Jitter requirements fulfilled



Time Extraction

by Digital Constant Fraction Discrimination (dCFD)

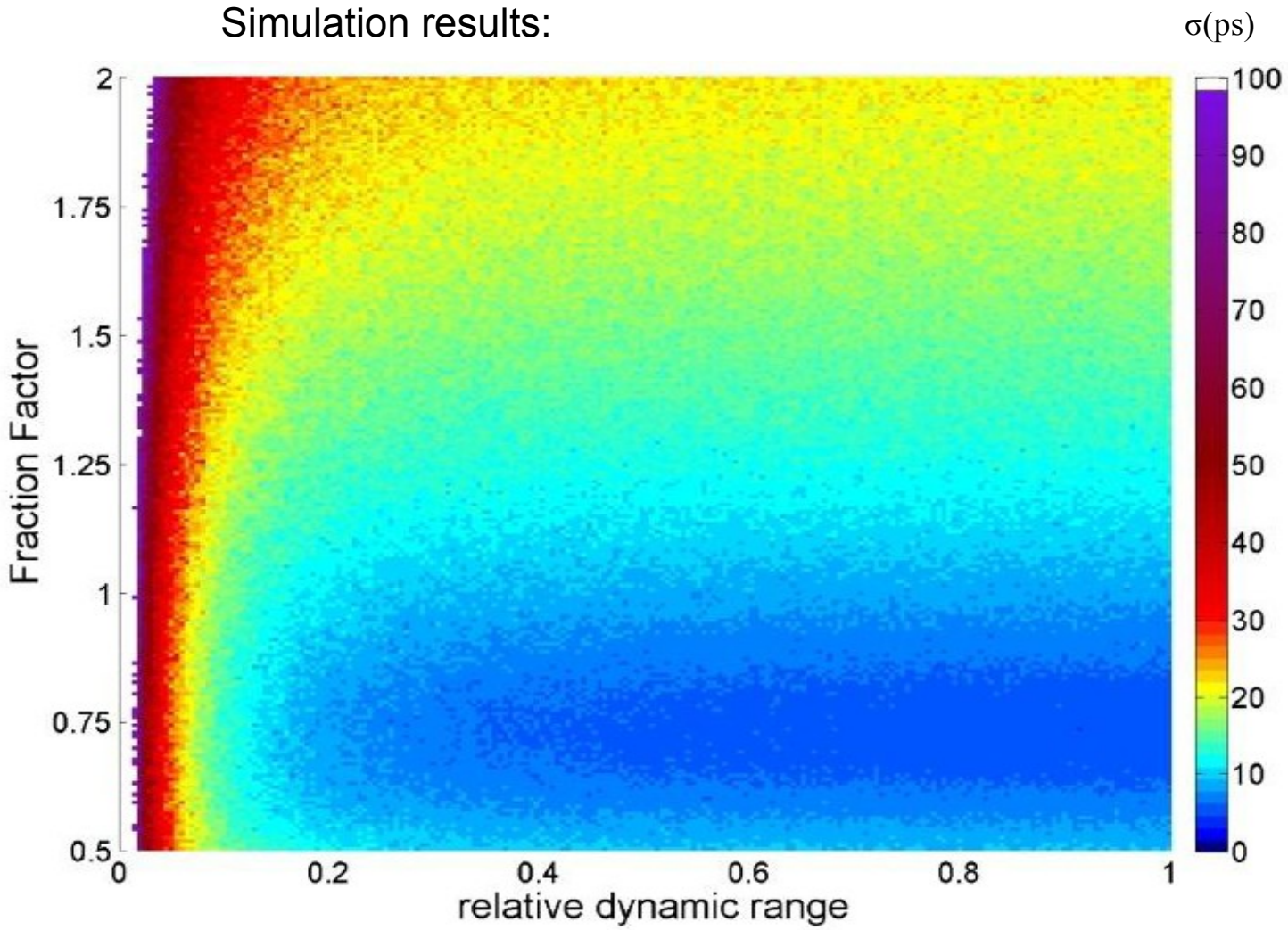
1. Inversion of samples
2. Delay of samples
3. Multiplication of samples by fraction factor
4. Addition of each sample with corresponding original sample
5. Determination of zero-crossing



Time Extraction

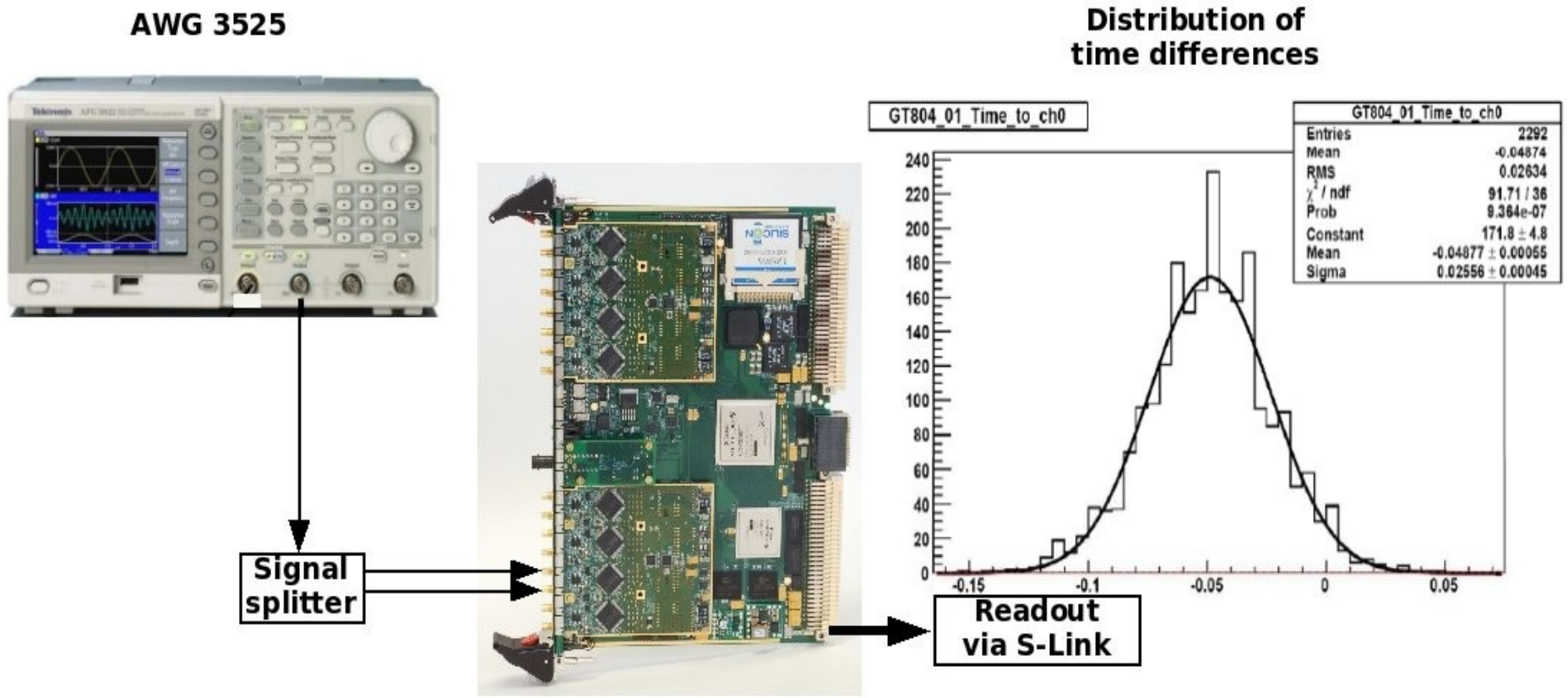
by Digital Constant Fraction Discrimination (dCFD)

Simulation results:



Time Resolution Measurements

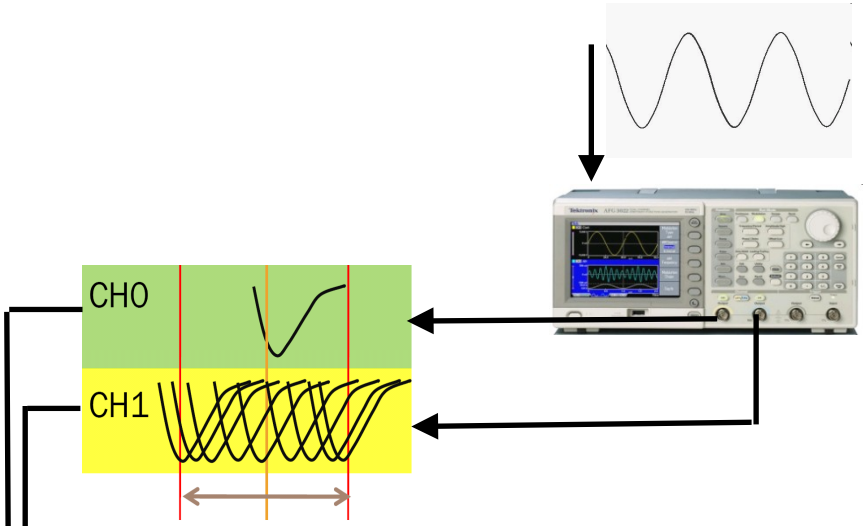
signals from Analog Wave Generator and signal splitting

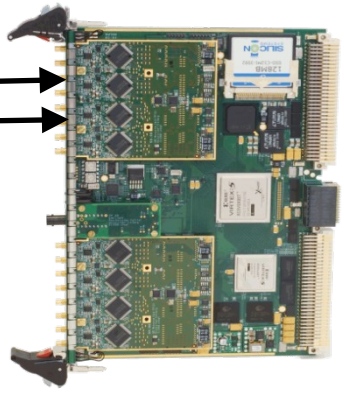


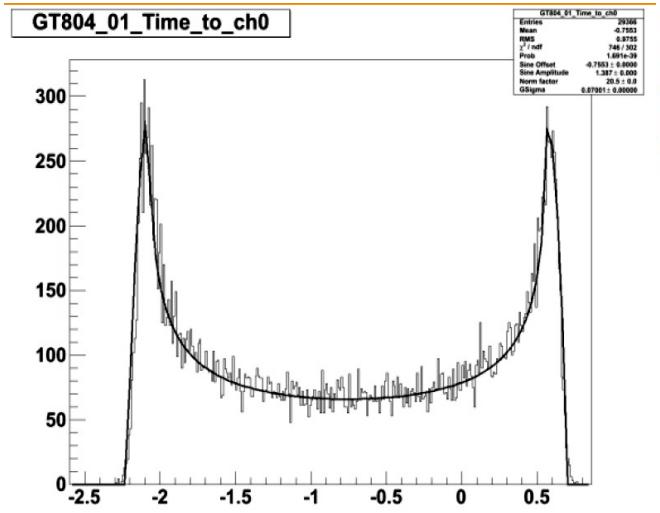
- Timing resolution for pulses of 30% of relative dynamic range: 0.006 x t_{bin} = 11.9 ps
- Timing resolution for pulses of 5% of relative dynamic range: 0.025 x t_{bin} = 49.5 ps

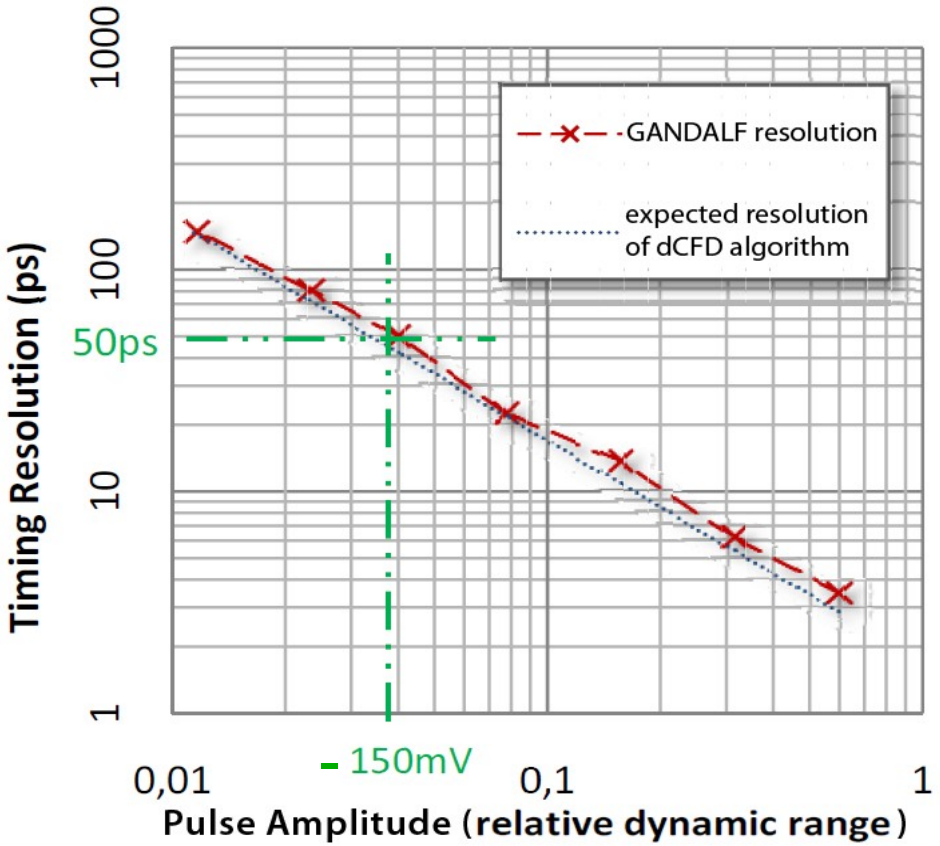
Time Resolution Measurements

signals from Analog Wave Generator and phase modulation



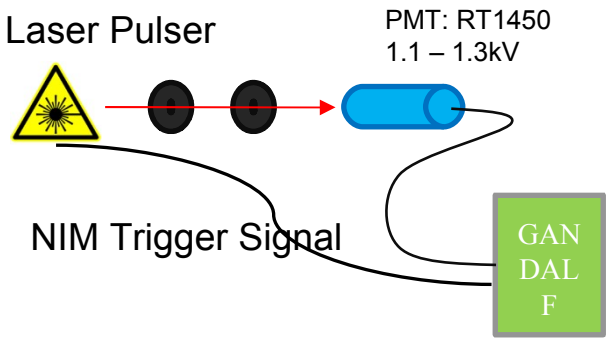


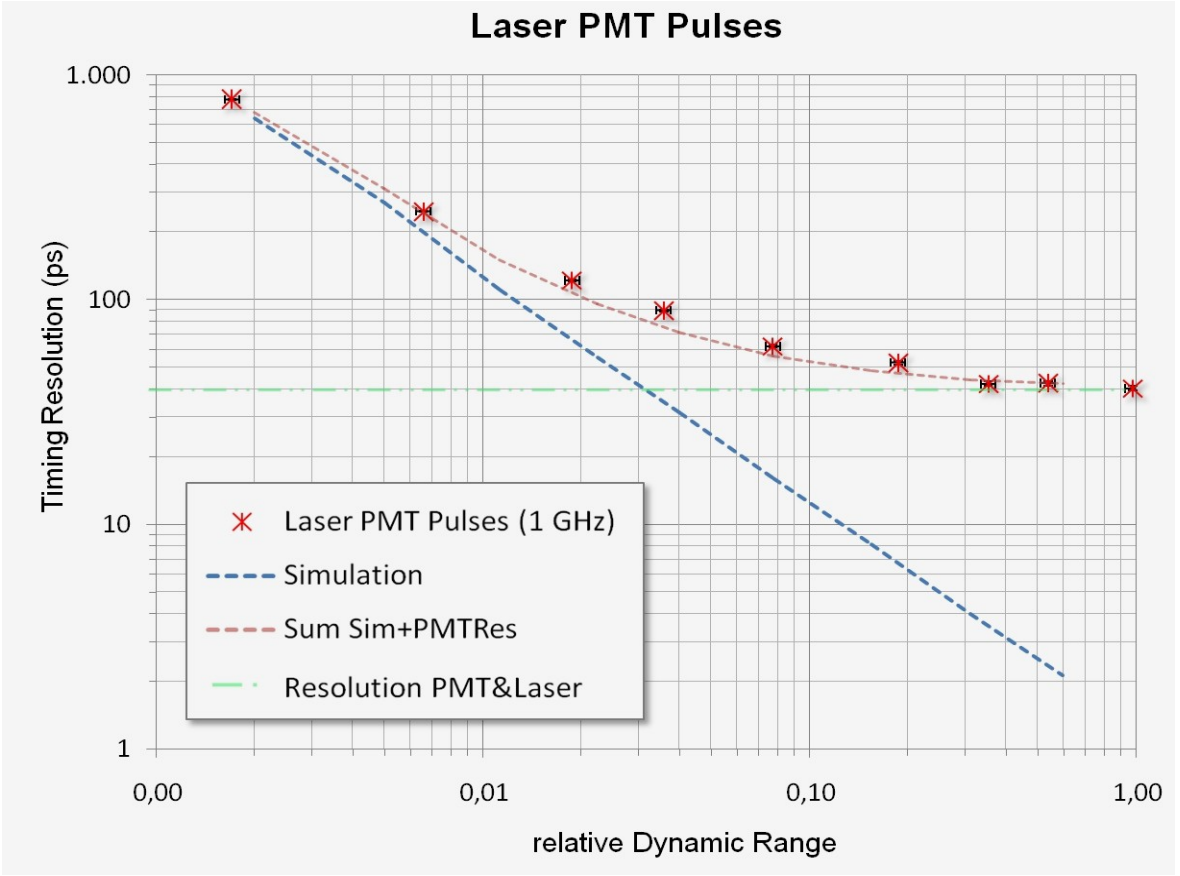




Time Resolution Measurements

System of Laser and Photomultiplier

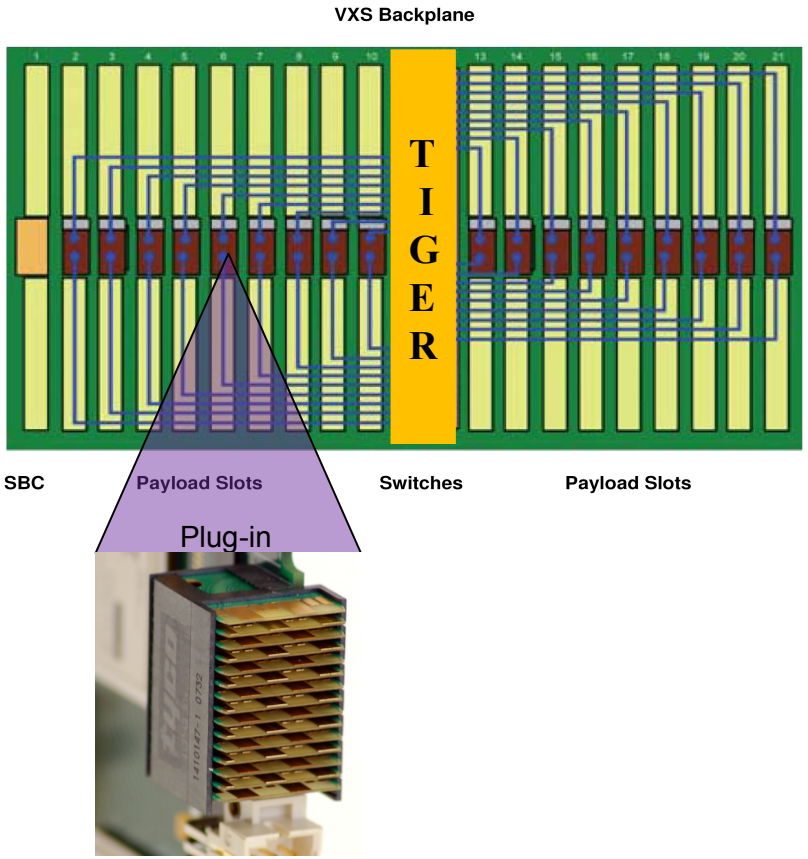


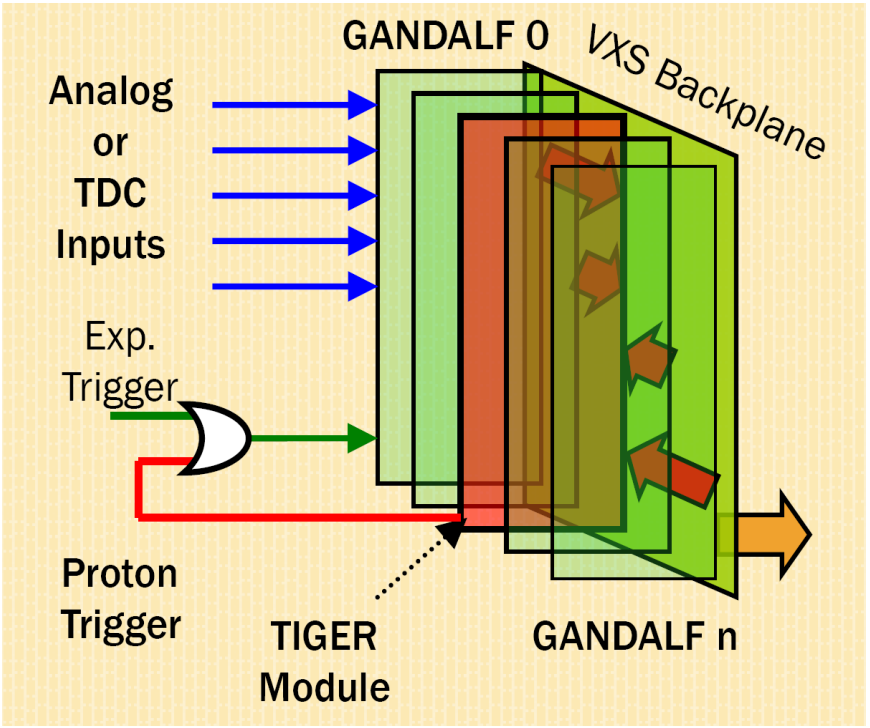


Proton Trigger

Trigger Implementation of GANDALF Electronic Readout (TIGER)

- TIGER module as VXS Switch Card



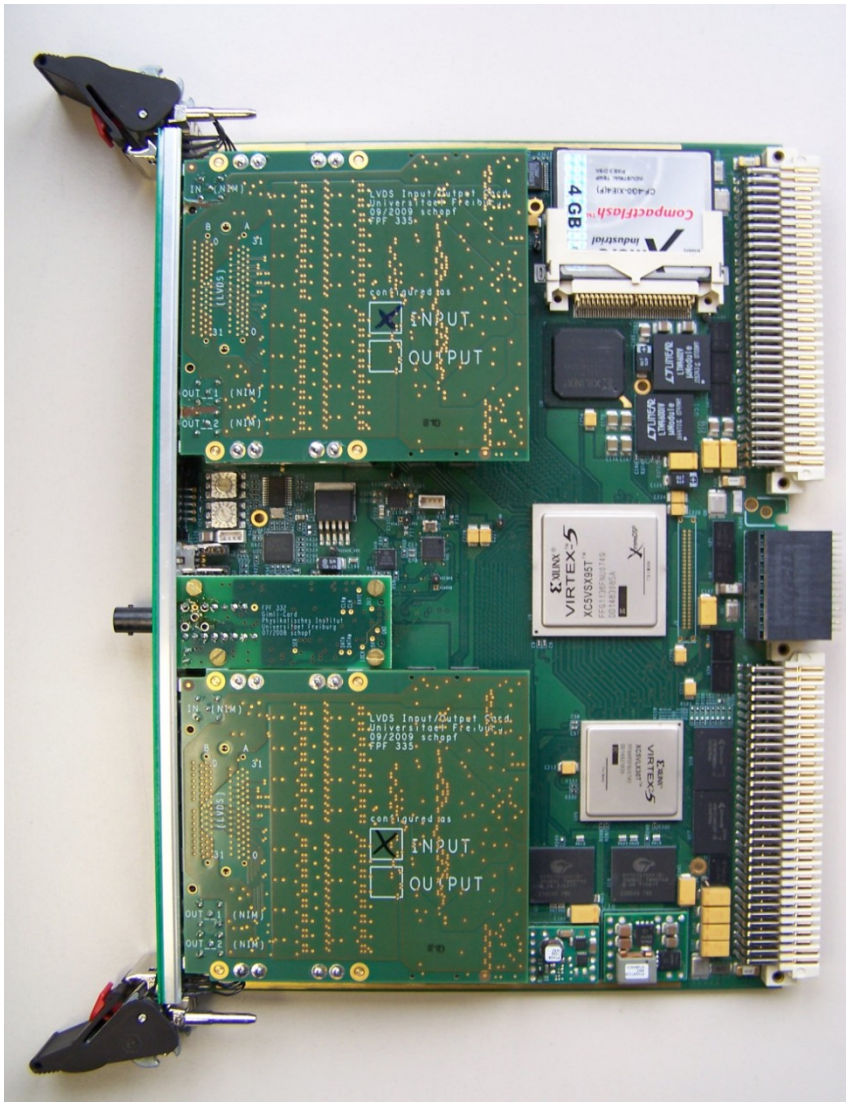


TIGER data acceptance:

18 x 16 bit x 500 MHz = 18 GB /s

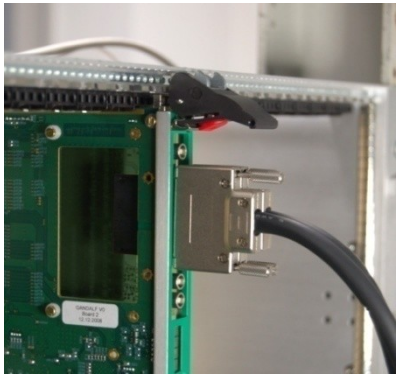
- GANDALF High-speed P0 connector with 16 differential pairs

GANDALF as TDC/Logic Module



Digital Mezzanine Card (DMC)

- 64 LVDS channels (input or output)
- 1 NIM input
- 2 NIM outputs



With full logic implemented in FPGA

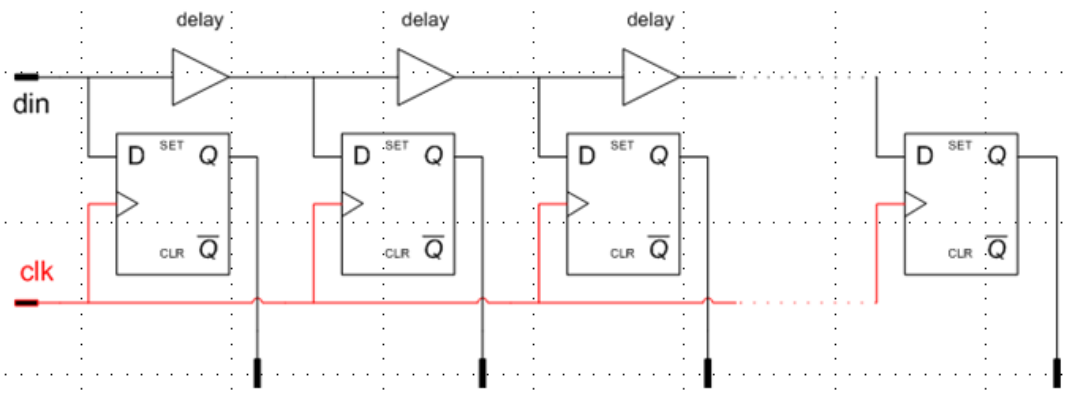
GANDALF serves as

- 128 channel TDC module
- 64 channel mean timer
- 128 channel scaler module

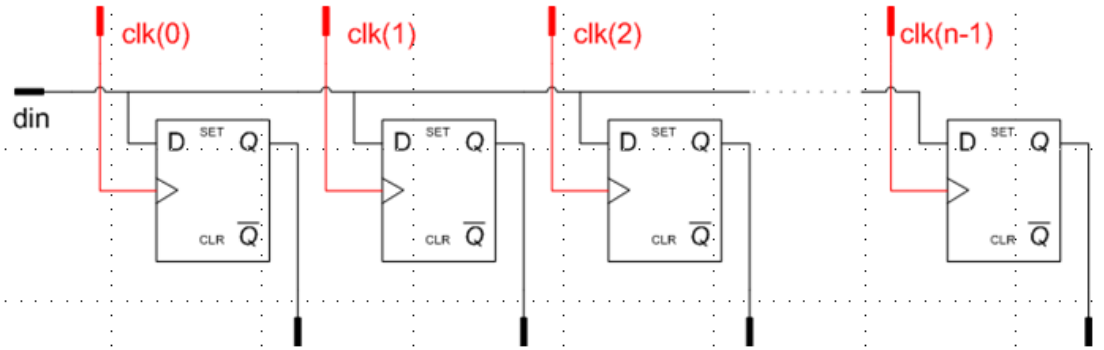
Backup

Subclock Resolution

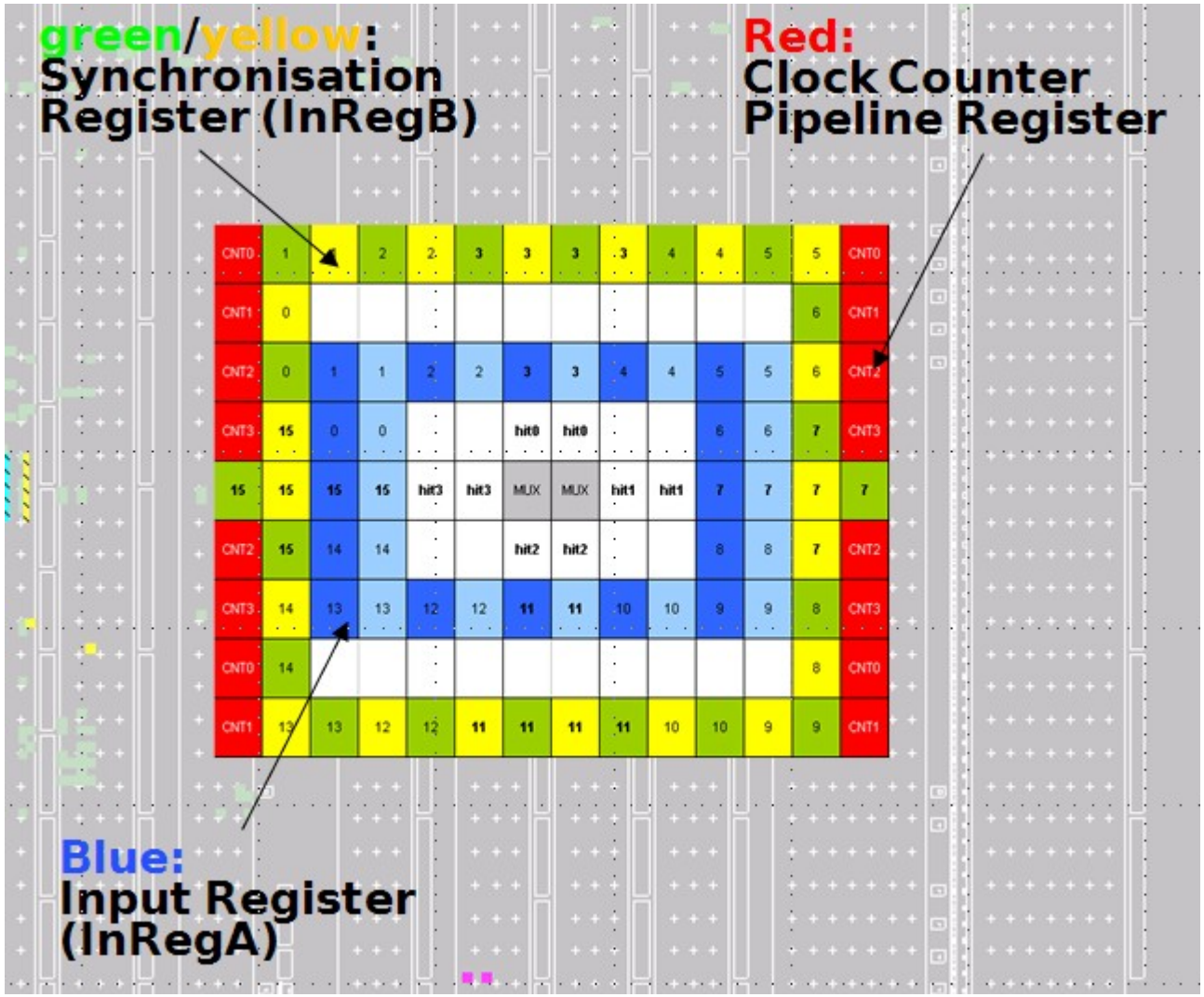
- Delayed Data Sampling (-> common clock)



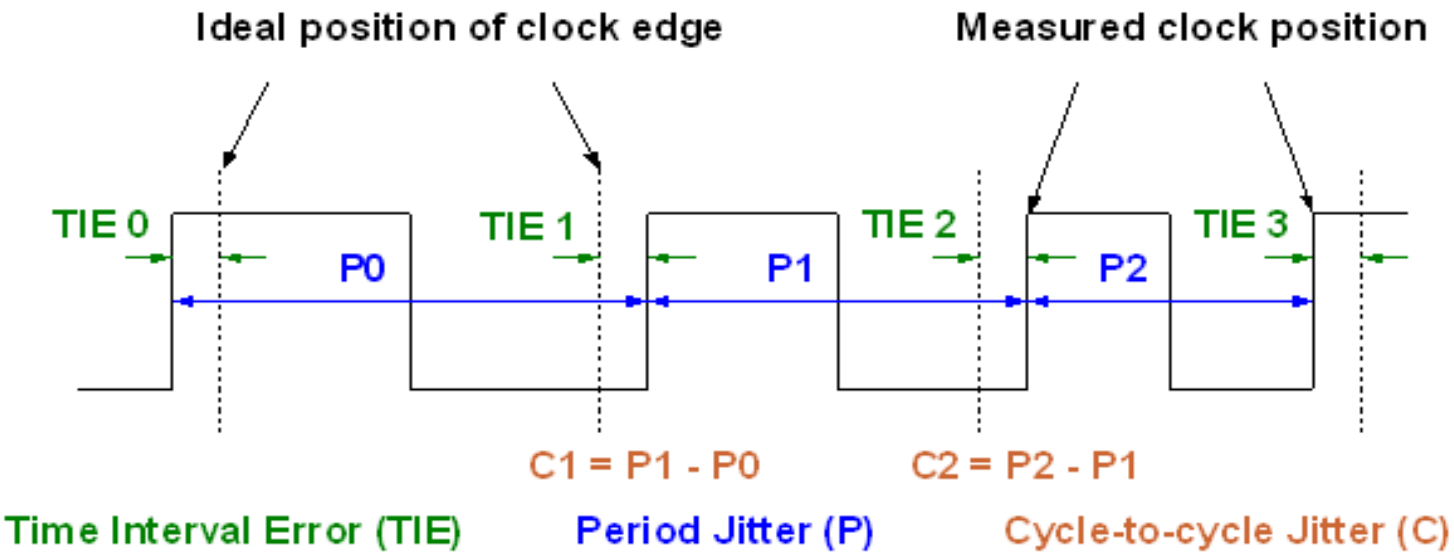
- Shifted Clock Sampling (-> common data input)



Order of the elements in the FPGA

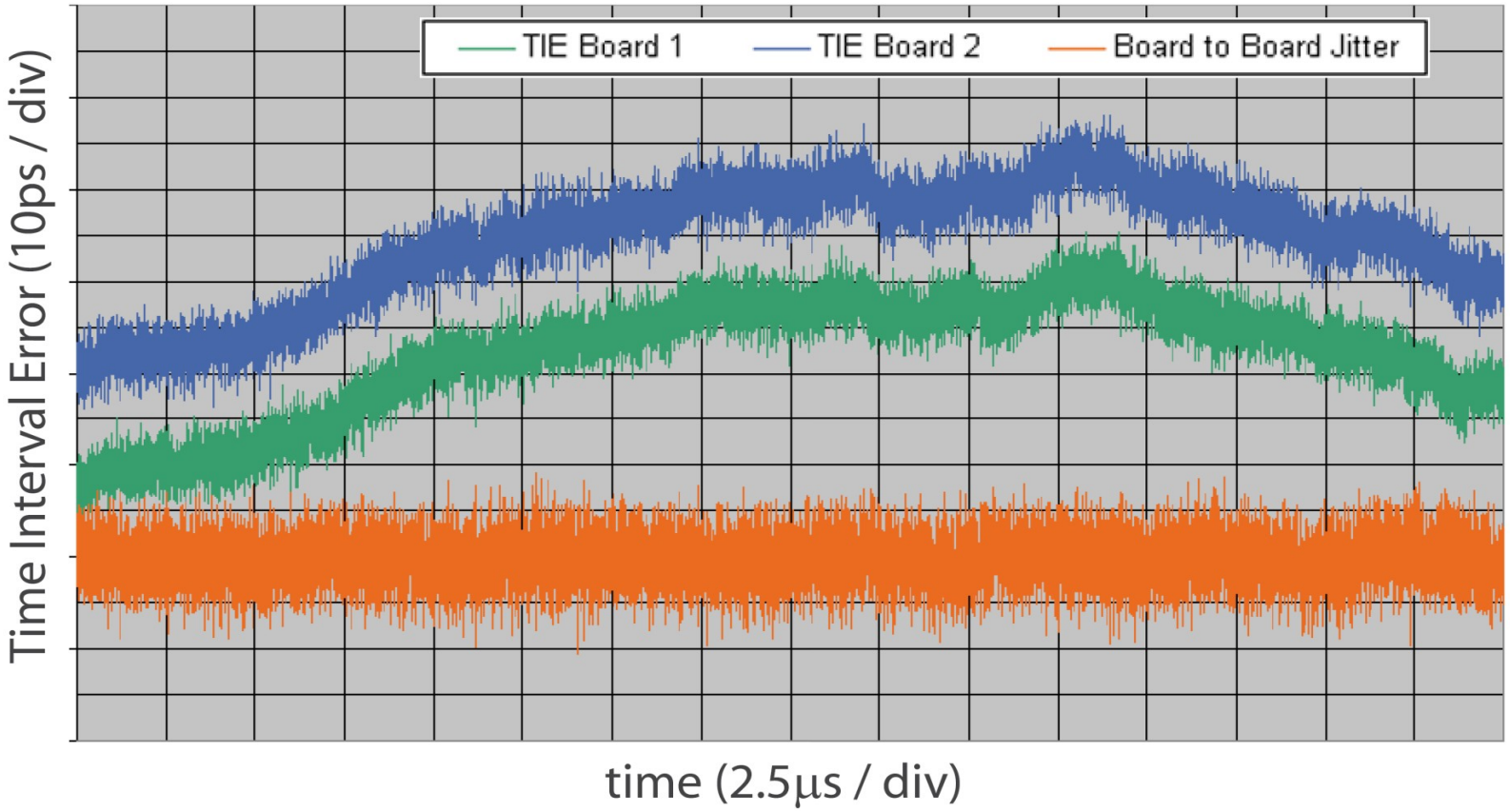


Jitter measurements



Board-to-Board Jitter

Measurement of the Board-to-Board Jitter



Time resolution (Board-to-Board)