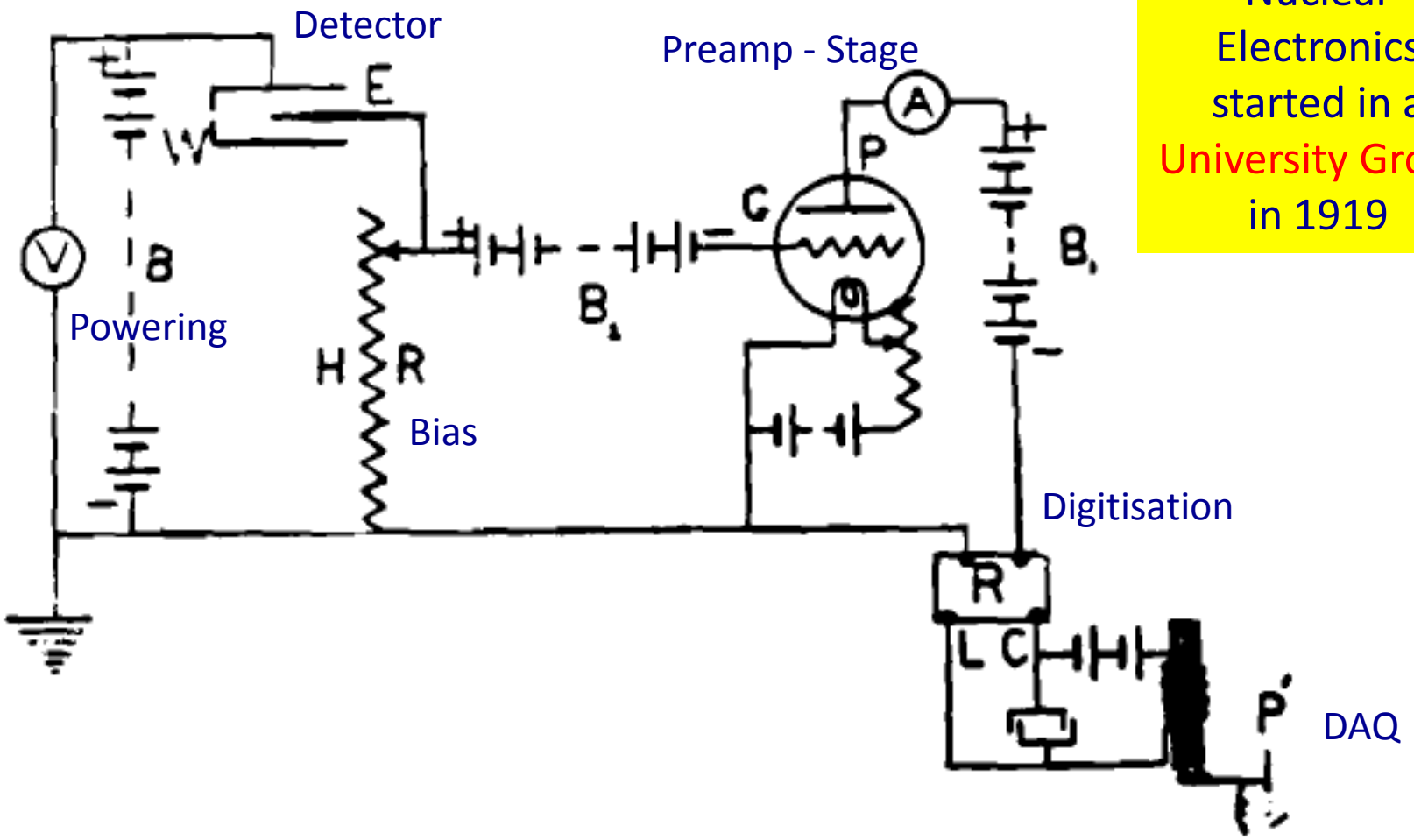
Advanced Electronics for Particle Physics and Beyond – Projects at German University Labs

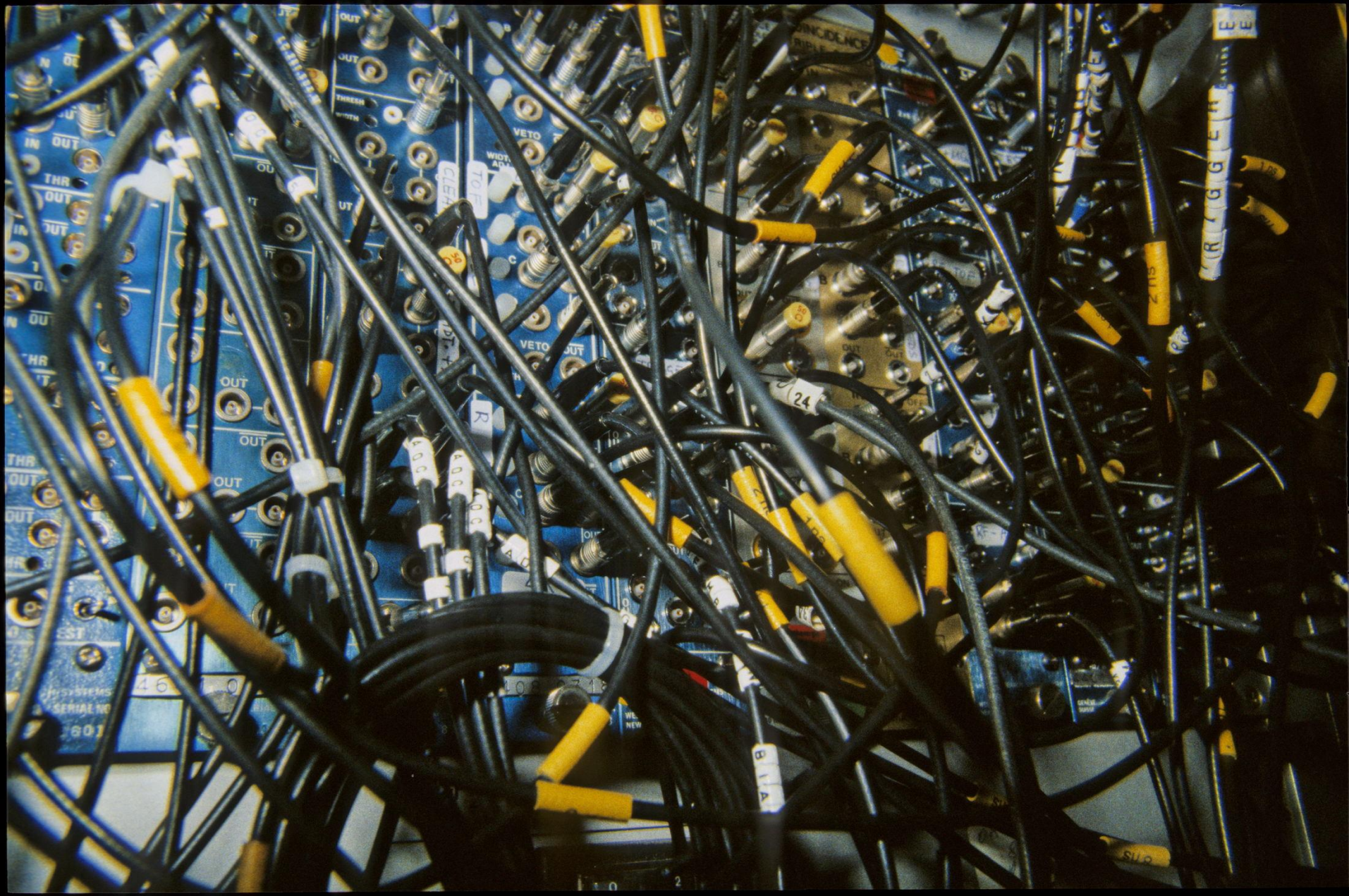
Karlheinz Meier
Kirchhoff-Institut für Physik
Heidelberg University

Topical Workshop for Electronics in Particle Physics
TWEPP 2010
Aachen

Nuclear Electronics started in a University Group in 1919



On the automatic registration of
α-particles, β-particles and Y-ray and X-ray pulses
Alois F. Kovarik, Sloan Laboratory, Yale University, 1919



Off-the-Shelf Modules (UA2 at CERN)

ATLAS

Level-1 Calorimeter Trigger

No Off-the Shelf Modules

> 1000 PCBs
ASICs, FPGAs, MCMs

➢10 Years development Time in universities and research institutes

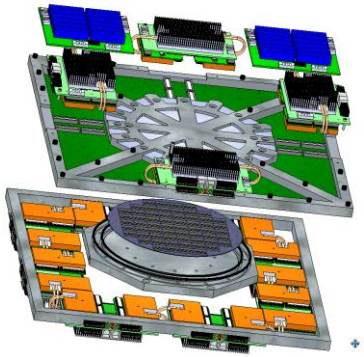
Questions for University Groups

- Can we handle this ?
- Is it worth the effort ?
- Is it science ?
- Is it plumbing ?
- What next ?

FAIR

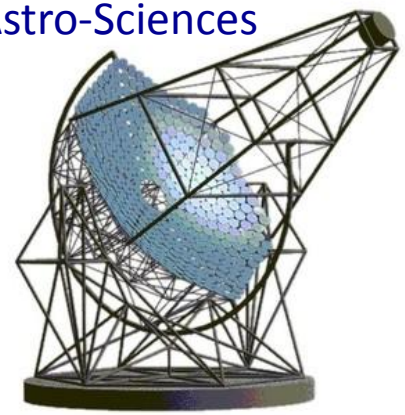
European XFEL

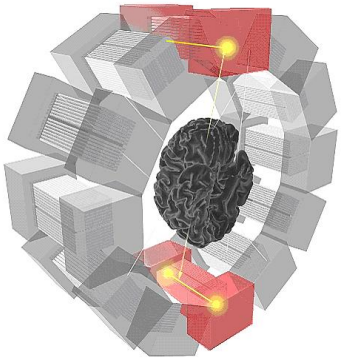
Fundamental information science



Other large scale projects with similar requirementas

Astro-Sciences





Medical Diagnostics and Therapy

BOSCH

Life perspective in industry for physics students

Electronics as an academic subject in

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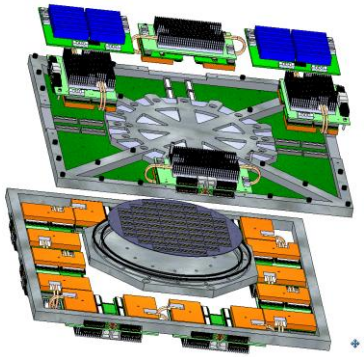
European XFEL

Fundamental information science



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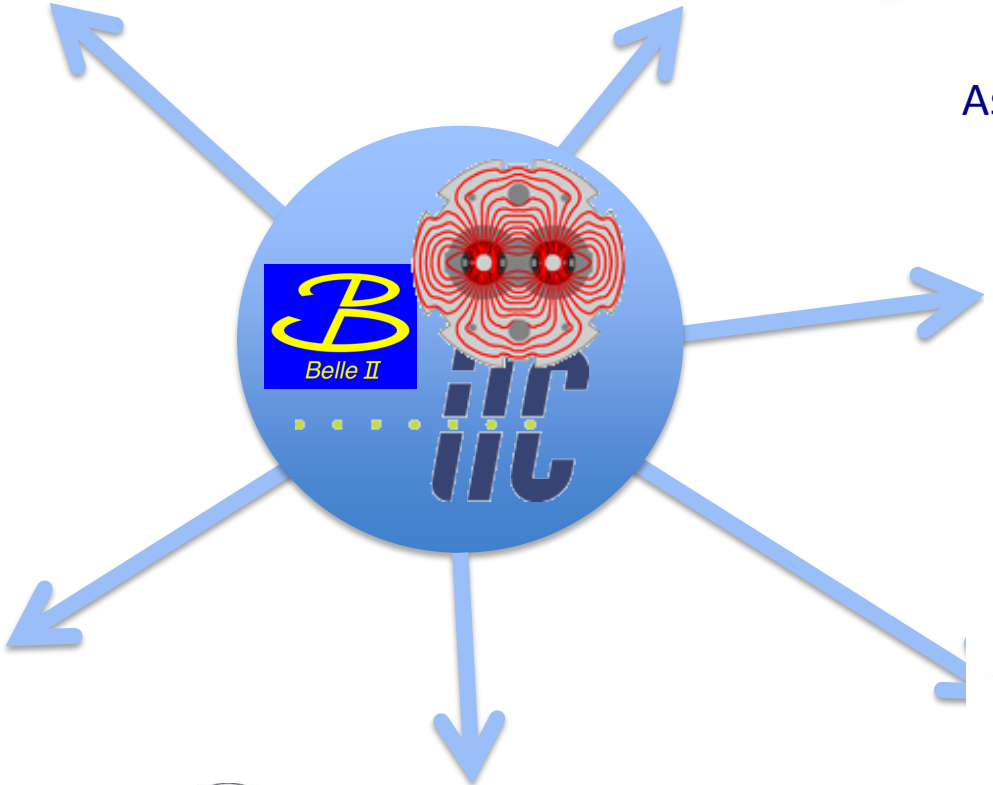

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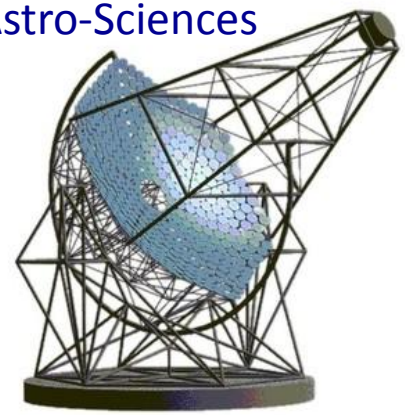

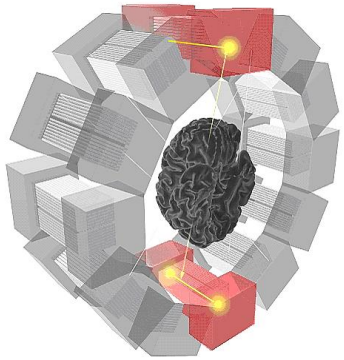

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Electronics as an academic subject in physics

SURVEY OF EUROPEAN PARTICLE PHYSICS 2009

Detector and Future Experiment Workforce in Germany

Experimental Particle Physics (generic activities and future facilities)		48.70
24.	Generic detector R&D	19.10
25.	High performance computing for particle physics	49.45
26.	Upgrades of LHC experiments (SLHC)	39.20
27.	ILC/CLIC experiments	8.40
28.	FAIR experiments	24.60
29.	super-Belle or super-b experiments	

189.45 FTE

National coordination of HE Particle Physics in Germany

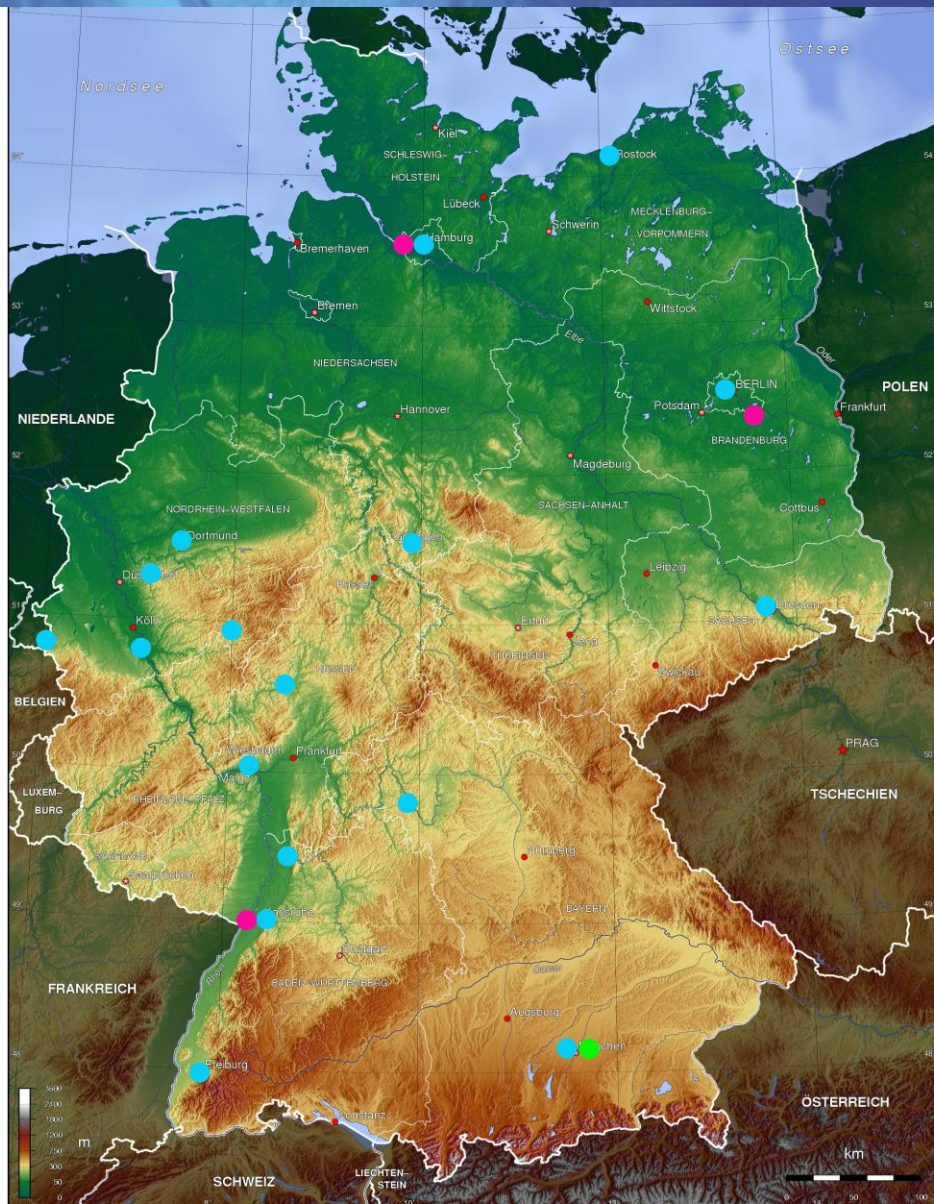
National Network of Complementary Excellence between

2 Helmholtz Centres
DESY and FZK (GridKa)

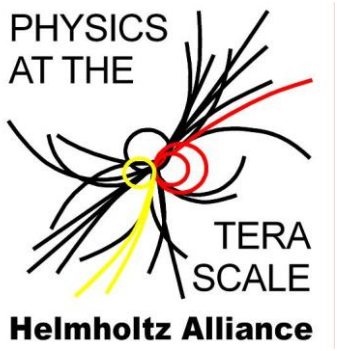
17 Universities
all German Institutes
working at energy frontier

1 Max Planck Institute
Munich

http://www.terascale.de/



HGF Alliance Laboratory for Detector Technologies (VLDT)



- Ensure a visible, efficient and sustained contribution of German groups to the future projects ILC and sLHC
- Develop, provide and maintain infrastructures and make them available to the Alliance
- Three branches, electronics system development, sensor development and general detector test facilities
- Central nodes of the VLDT are DESY, the University of Bonn and the University of Heidelberg. Additional infrastructure is made available to the Alliance by Aachen, Hamburg and Karlsruhe

VLDT Support offered to Users

- Access to Lab Equipment (clean rooms, high performance meaurement devices)
- Access to assembly facilities (bonders, BGA placers)
- Well maintained S/W CAE Tools
- Instrumentation Tutorials (Testing, Bonding, Packaging)
- Software Support (Layout, Simulation)
- Submission Support (MPW, Engineering Runs, Full Runs)
- Submission Readiness Reviews
- ASIC Designer Style Guides

AMI SEMICONDUCTOR

Mentor Graphics

austriamicrosystems
a leap ahead in analog

XILINX®

IBM

ALTERA®

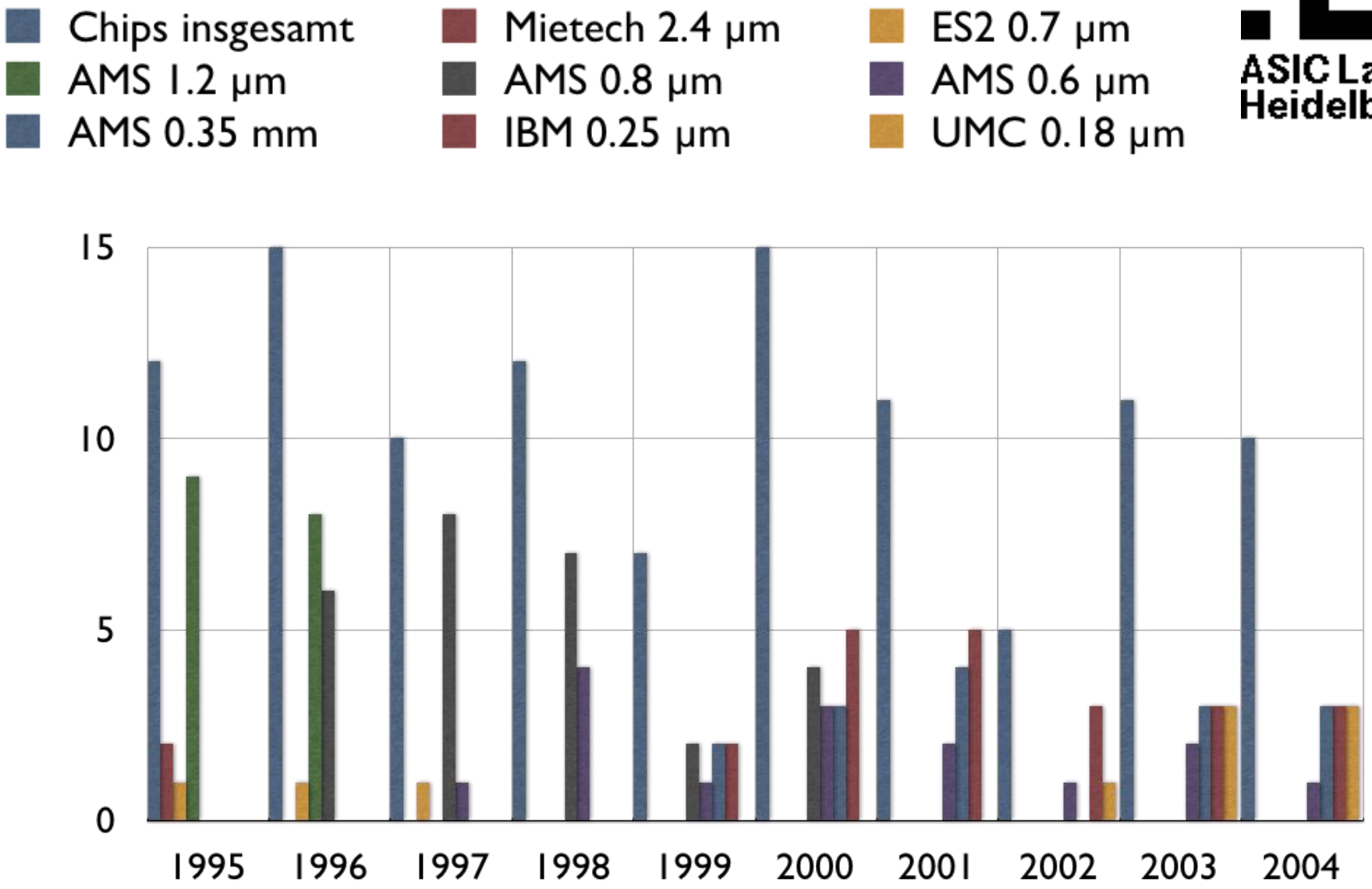
tsmc®

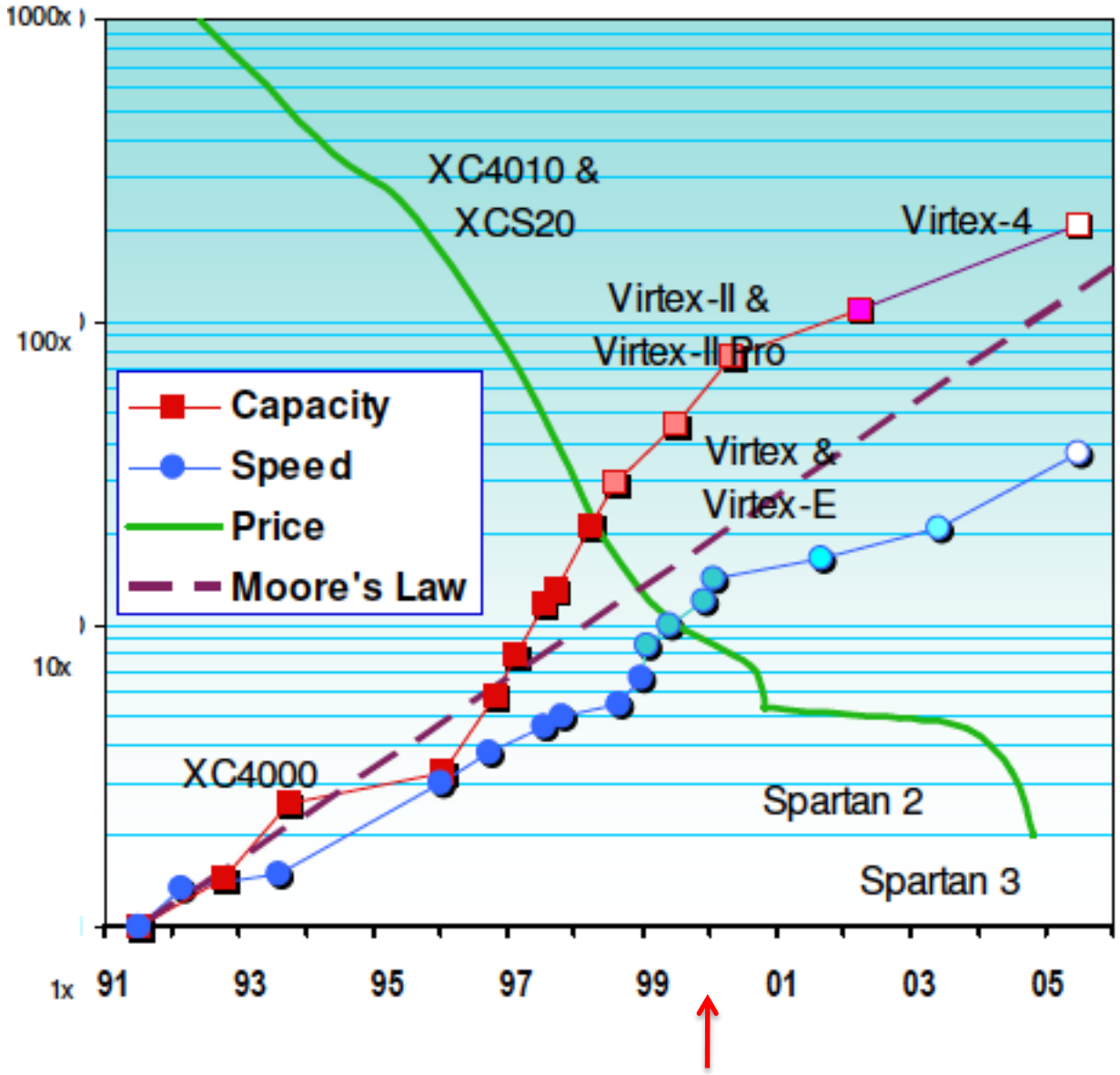
cadence

SYNOPSYS®

Example Heidelberg ASIC Lab : 108 Chip Submissions in 10 Years

ASIC Labor Heidelberg





The Rise of Field Programmable Gate Arrays

Logic x 200

Speed x 40

Lower Power x 50

Lower Cost x 500

S. Trimberger (XILINX)

many LHC (frontend) technology decisions

Easy access to „custom digital design“ for university groups without expensive equipment

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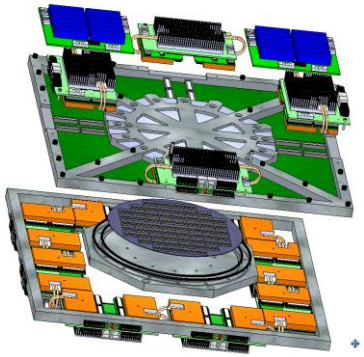
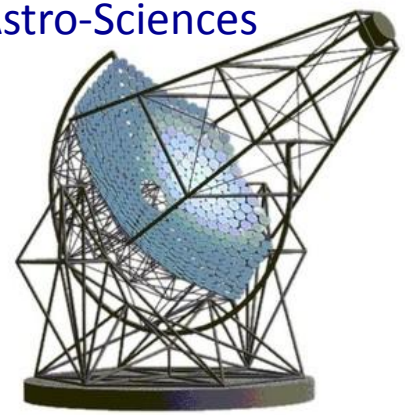
Fundamental information science

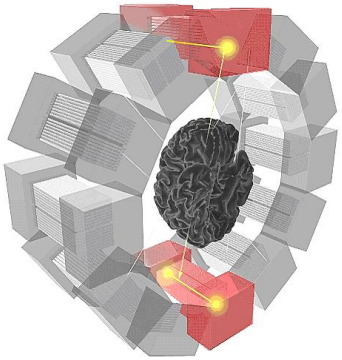


Other large scale projects with similar requirementas

Belle II

Astro-Sciences





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Electronics as an academic subject in

Frontend FE-I4 for ATLAS pixel detector upgrades
IBL Project (2014) and sLHC
Common design effort: Bonn, CPPM, Genua, LBNL, NIKHEF

- Rad.-hardness >200 MRad TID (FE-I3: >50 Mrad)
- ToT coded in 4 bits.
- detector leakage current > 100 nA

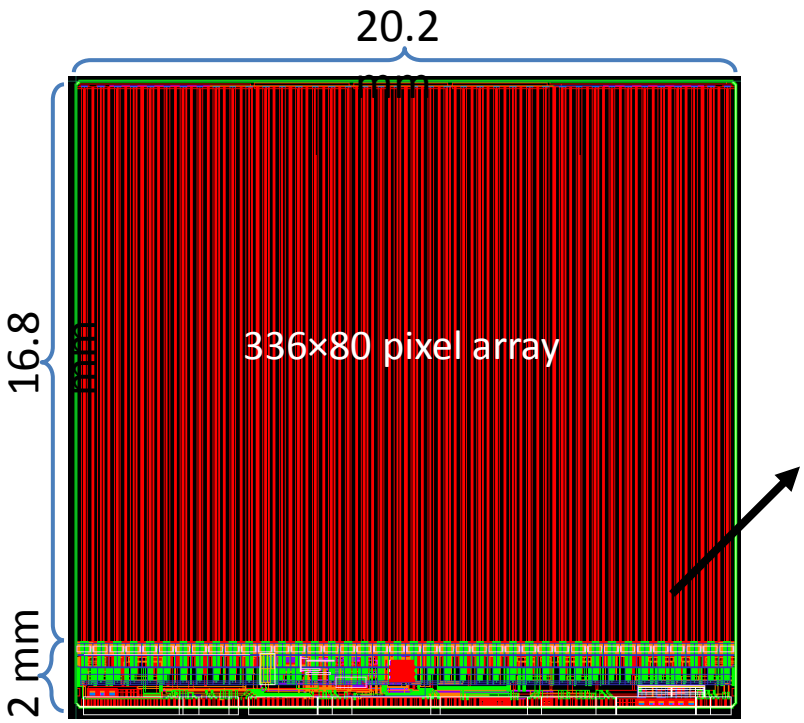
	FE-I3	FE-I4
Pixel Size [µm²]	50×400	50×250
Pixel Array	18×160	80×336
Chip Size [mm²]	7.6×10.8	20.2×19.0
Active Fraction	74 %	89 %
Analog Current [µA/pix]	26	10
Digital Current [µA/pix]	17	10
Analog Voltage [V]	1.6	1.4
Digital Voltage [V]	2	1.2
LVDS out [Mb/s]	40	160

½ current pixel size!

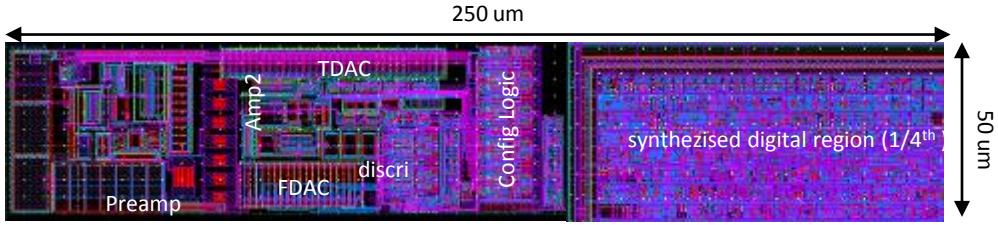
largest in HEP to date

analog / digital power

tuned for IBL occupancy



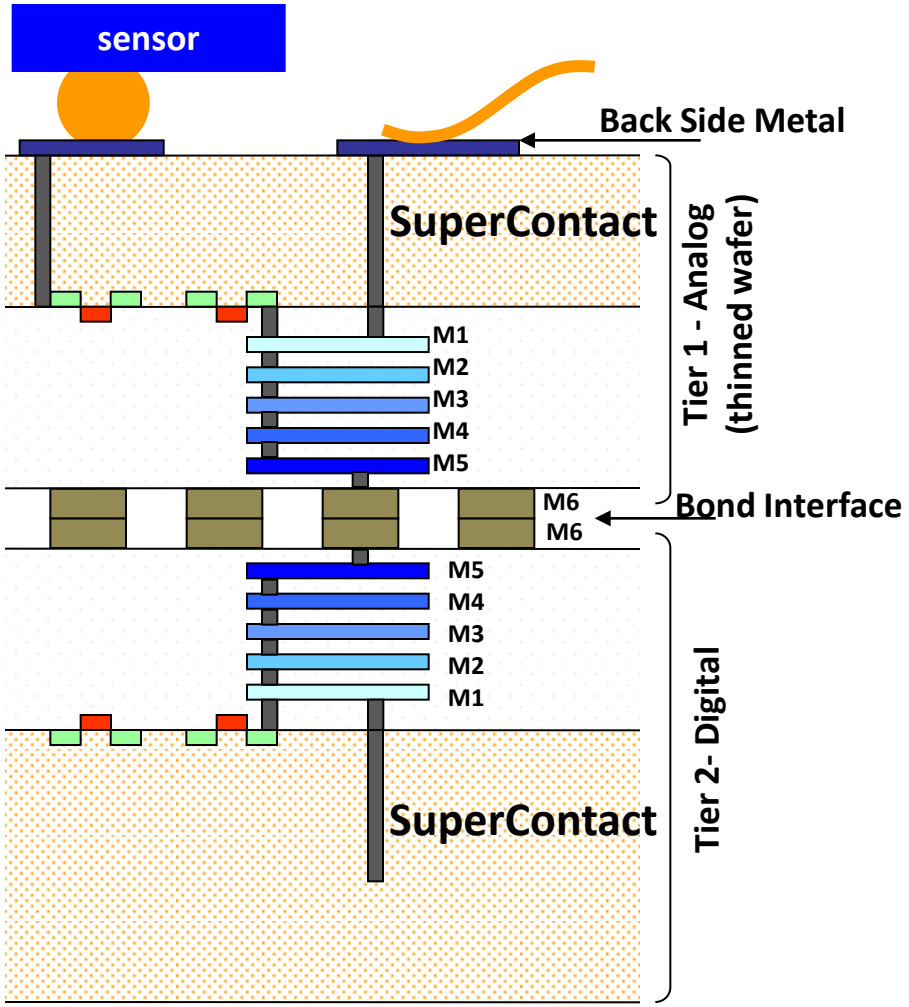
- Full scale engineering prototype: FE-I4A



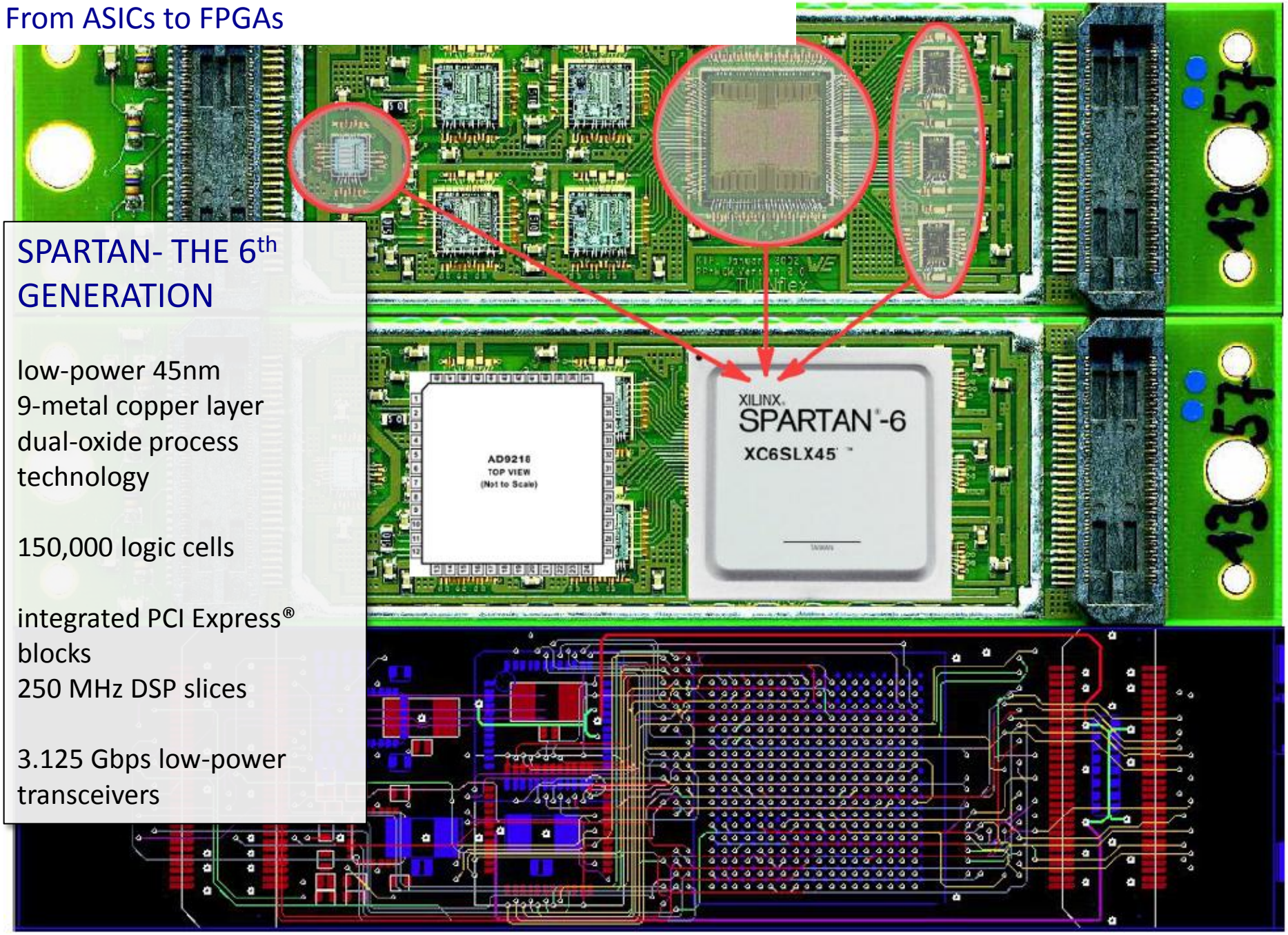
TWEPP 2010 :
Vladimir Zivkovic (NIKHEF)
Laura Gonella (Bonn)
Jens Dopke (Wuppertal)

ATLAS sLHC Pixel Upgrade : 3D Technology for Smaller Pixels

- Collaboration of Bonn (Germany), CPPM (France) and LBNL (USA).
- Goal: 50×125 µm^2 pixel size with split analog and digital functionalities
- Technology:
  - Chartered 130nm
  - Tezzaron 3D
- Prototype submitted in std. Chartered 130nm technology as a test bench: ➔ Good performance
- 3D analog + digital stack submitted, processing has started



ATLAS – Level-1 Calorimeter Trigger Upgrade (Heidelberg)
From ASICs to FPGAs



SPARTAN- THE 6th GENERATION

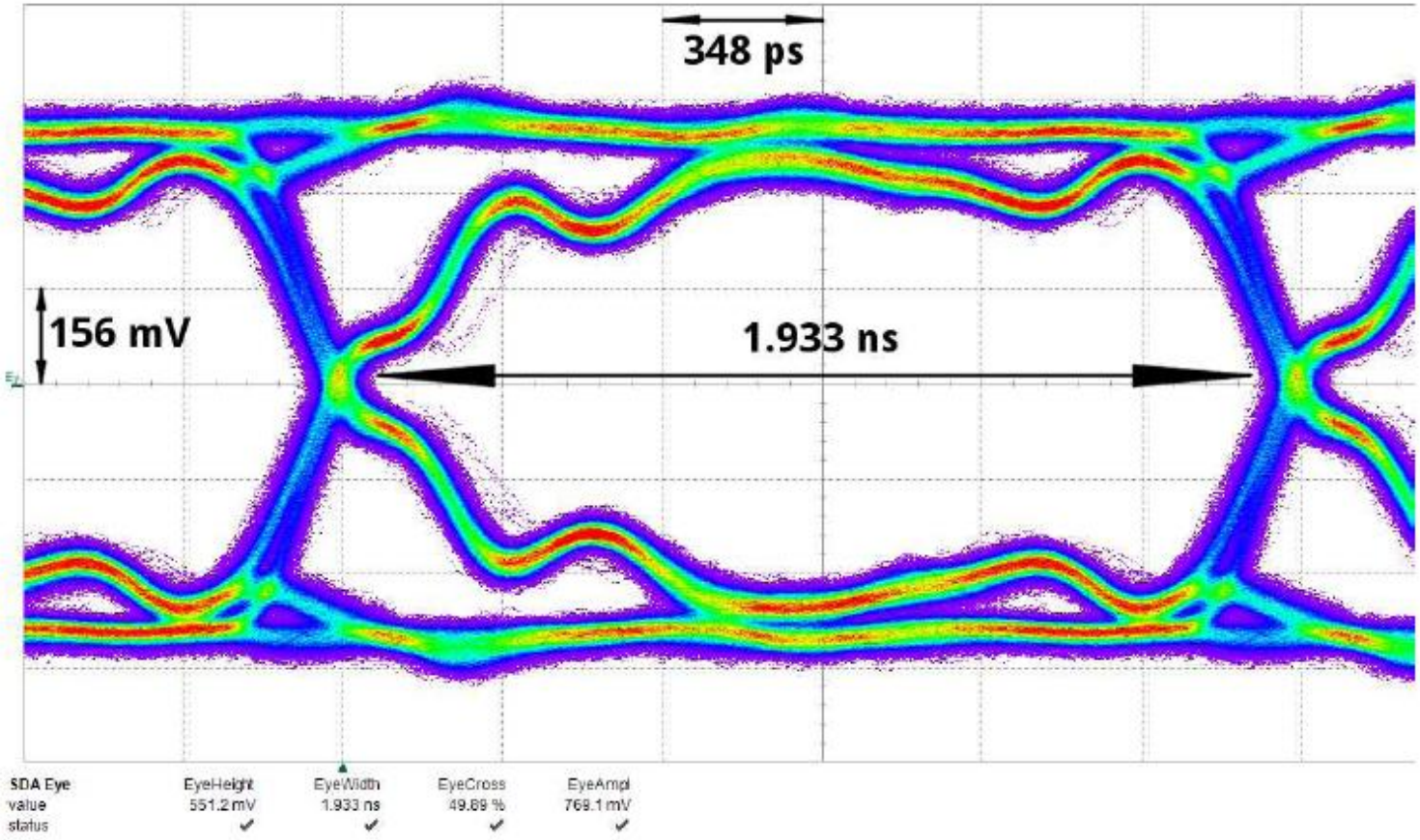
low-power 45nm
9-metal copper layer
dual-oxide process
technology

150,000 logic cells

integrated PCI Express® blocks
250 MHz DSP slices

3.125 Gbps low-power transceivers

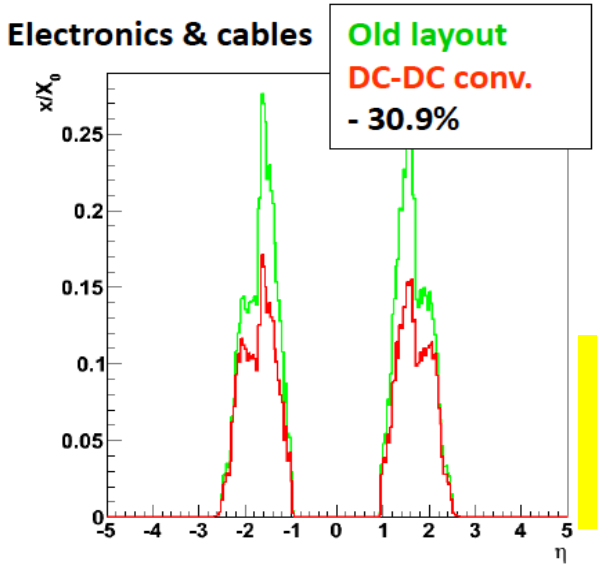
480 Mbits/s LVDS link driven by Spartan-6 FPGA



Implemented using Spartan-6 output serialiser blocks (OSERDES2).

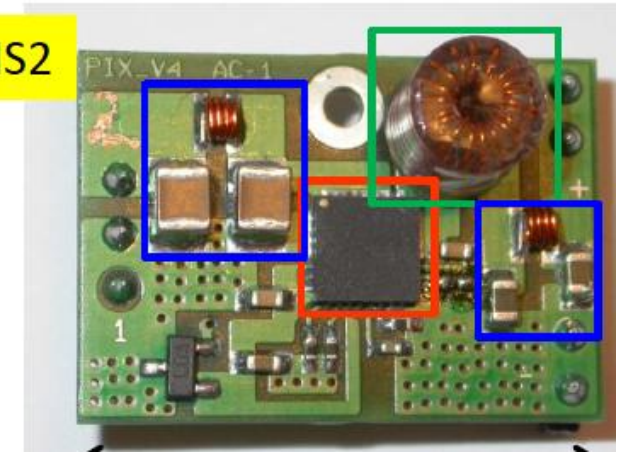
TWEPP 2010 : Andrei Khomich (Heidelberg)

DC-DC Powering CMS Tracker (Aachen)



TWEPP 2010 :
Katja Klein (Aachen)
Jan Sammet (Aachen)

AMIS2

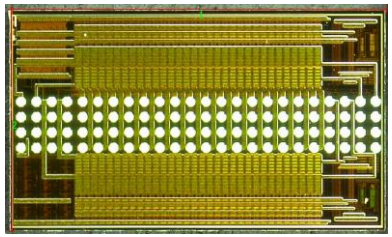


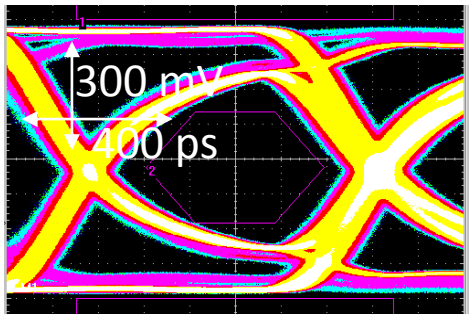
Radhard (MGy) AMIS2 Chip by CERN
DC-DC System with aircore coil (4T CMS field)

V_{in} = 3-12 V
I_{out} < 3A
V_{out} = 1.2, 2.2, 3.3 V
f_s = 600 kHz – 4MHz

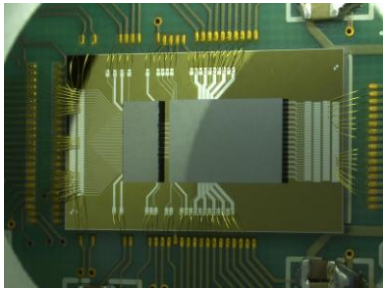
Belle DEPFET Vertex Detector
Complete Electronics Chain (Barcelona, Bonn, Heidelberg)

Data handling processor DHP 0.1 (IBM 90nm)
C4 bump bonds, full data processing, Gbit link,
Analog blocks (U Barcelona)



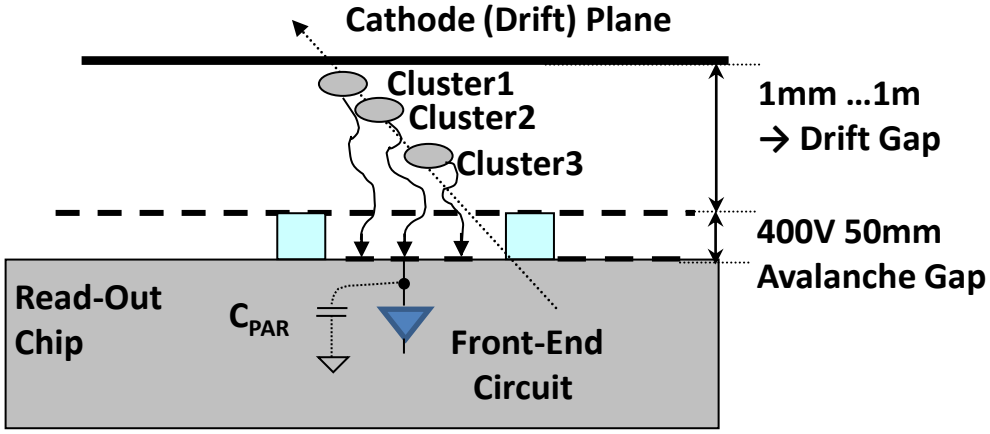


Switcher : radiation-hard
switching of on-detector 20 V
signals



DEPFET Current Digitiser (DCD)
256 channels, 10-bit, 10 MHz ADCs, 65 400 MHz Links

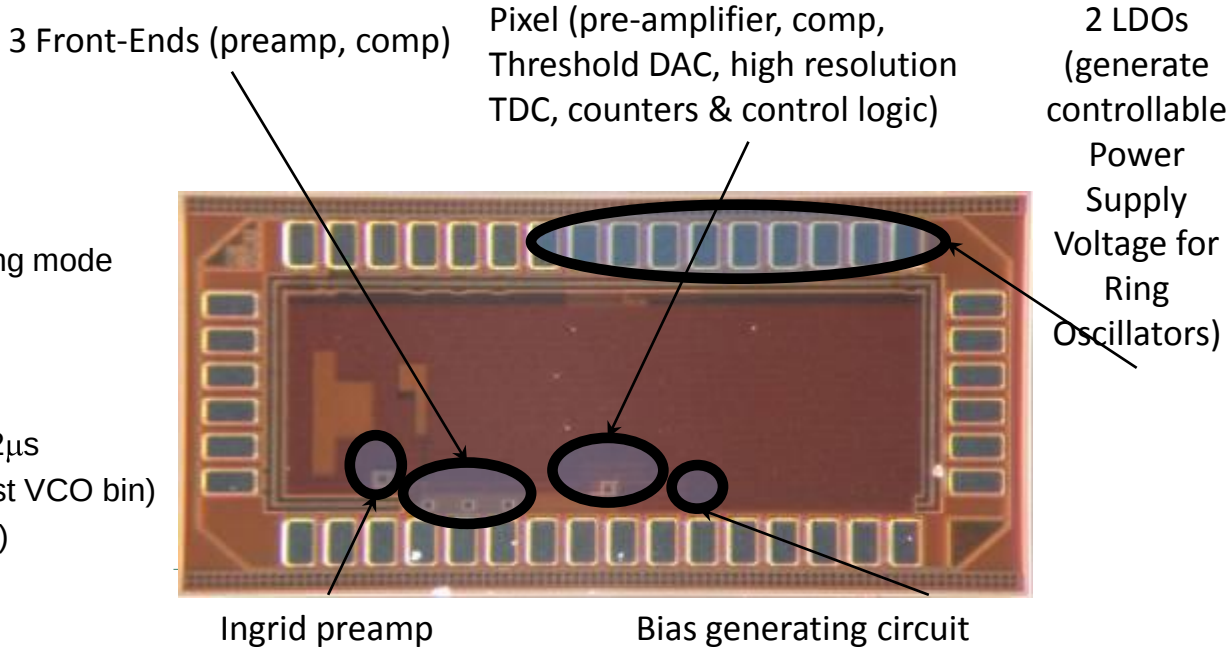
Read-Out of Micro-Pattern Gas Detectors
Gas-avalanche detector with a CMOS readout pixel array (ILC Study)
Bonn, NIKHEF



TWEPP 2010 :
Andre Konrad Kruth (Bonn)

GOSSIPO-3 Test Chip

- Prototype for TPC read-out
- IBM 130nm CMOS (8 metal layers)
- 60μm x 60μm pixels (high granularity)
- Time Measurement mode and Hit Counting mode
- Local TDC in every pixel
- Design Goals:
  - 3μW per channel
  - Arrival time measurement up to 102μs
  - Arrival time accuracy 1.6ns (one fast VCO bin)
  - ToT accuracy 200e^- accuracy (27ns)
- Design effort lead by NIKHEF with contributions from Bonn



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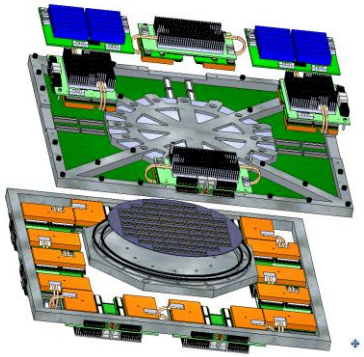
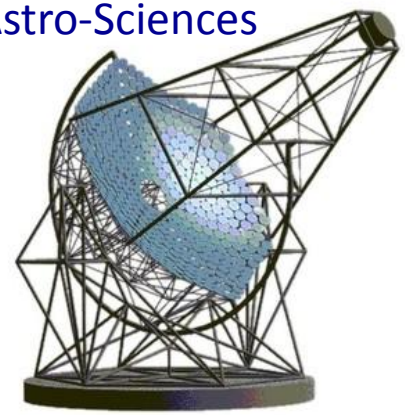
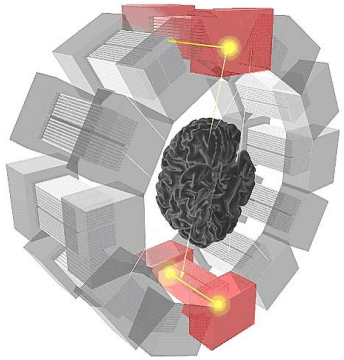
Fundamental information science



Other large scale projects with similar requirementas

Astro-Sciences





Medical Diagnostics and Therapy

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Life perspective in industry for physics students

Electronics as an academic subject in

Silicon Photomultiplier Readout Systems Heidelberg

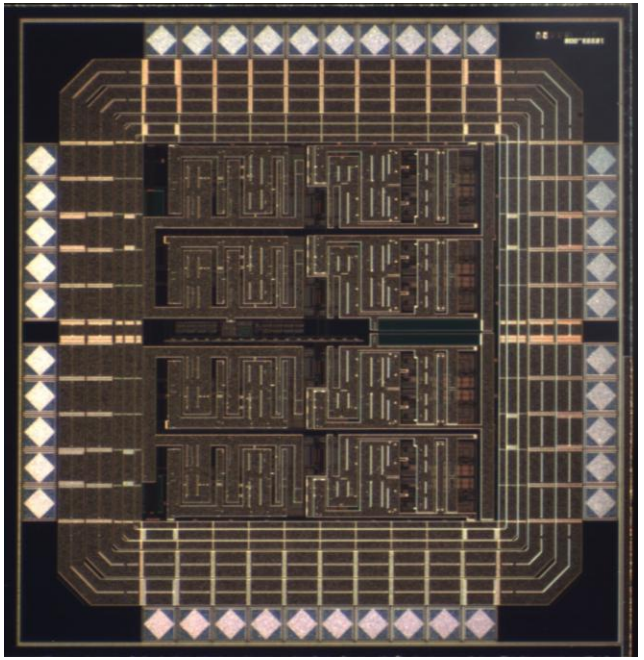
CALICE

KLauS: Charge Readout Chip

[Kanäle für Ladungsauslese von SiPMs]

AMS 350nm CMOS technology; 4 channels;
SPI interface controlled by FPGA; Bias DAC tunable;
high Signal/Noise Ratio [>10, 40 fC signal charge];
fast trigger available [pixel signal jitter < 1ns];
large dynamic range up to 150pC

Upgrade version to be part of SPIROC III
S. Callier et. al, IEEE NSS/MIC, 2009;
0.1109/NSSMIC.2009.5401891



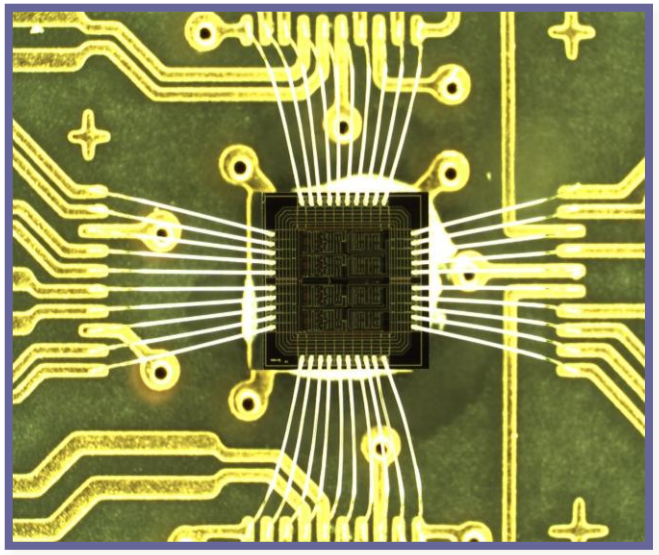
PET and ToF

STiC: SiPM Timing Chip

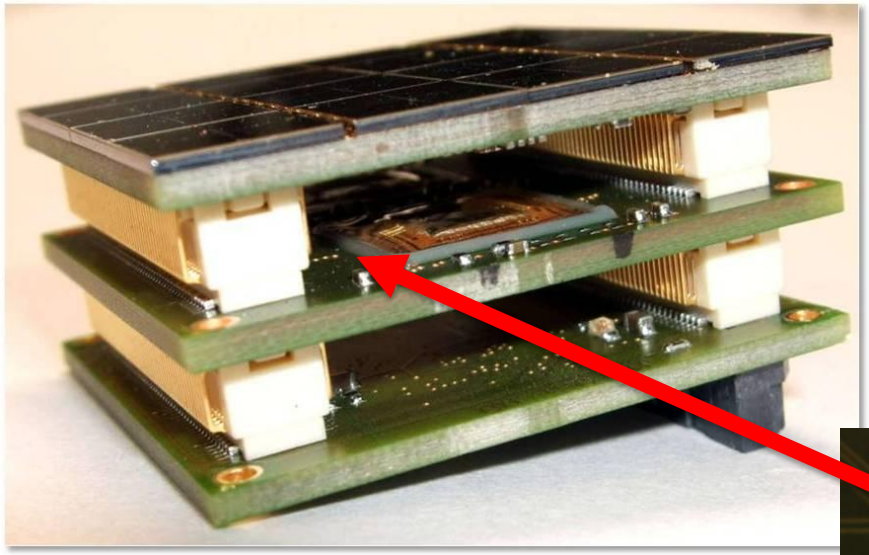
[Fast Discrimination for ToF]

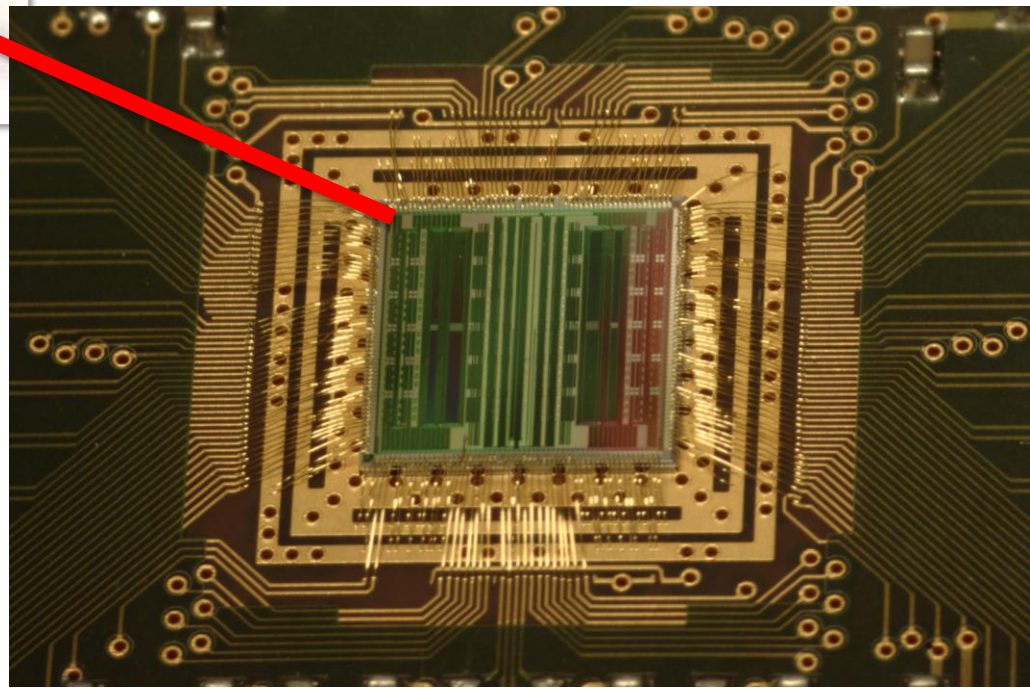
AMS 350nm CMOS , 4 channels;
Leading edge & Constant fraction Trigger;
Bias DAC tunable ~ 1 V; power < 10mW/ch
Pixel jitter ~300 ps, time of flight capability

W. Shen et. al, IEEE NSS/MIC,
2009; 10.1109/NSSMIC.2009.5401693



Readout of APD Array for PET-MR (Heidelberg)





40 Channel Readout Chip

- fast low-noise differential amplifiers
- O(100µV noise)
- timestamping with 50ps binwidth
- integrator
- > 9Bit ADC

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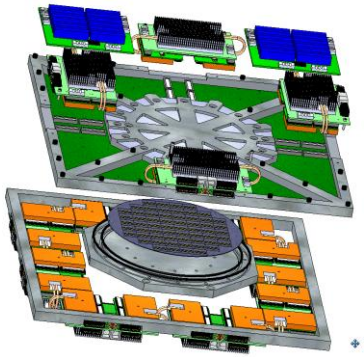
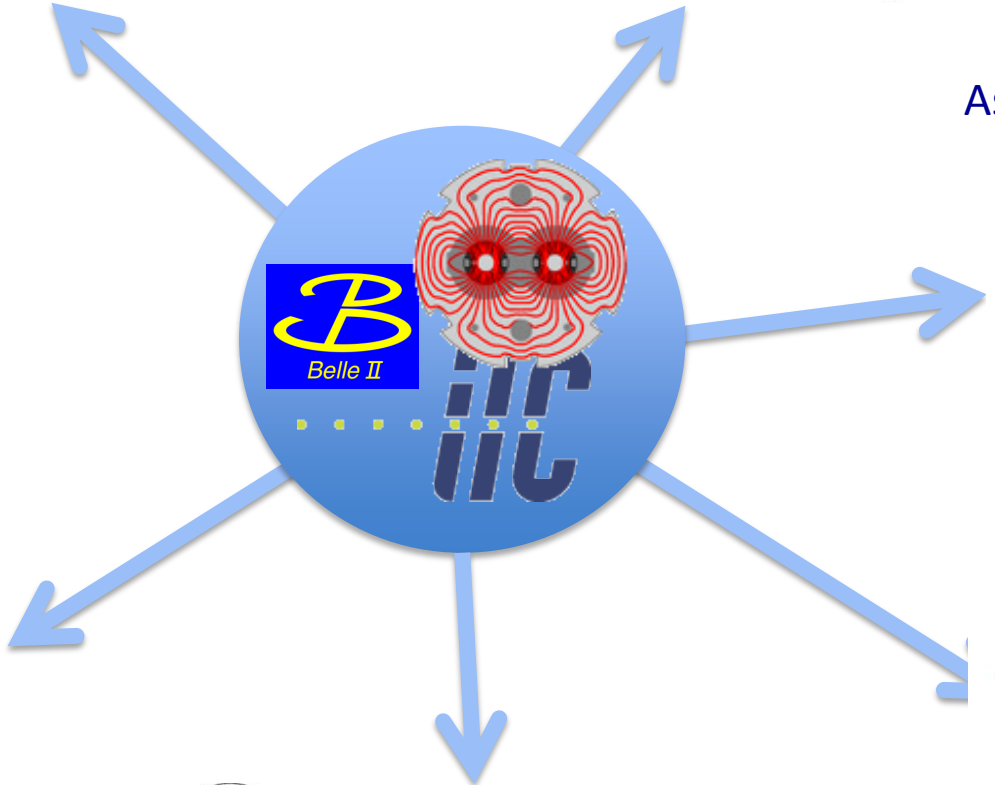
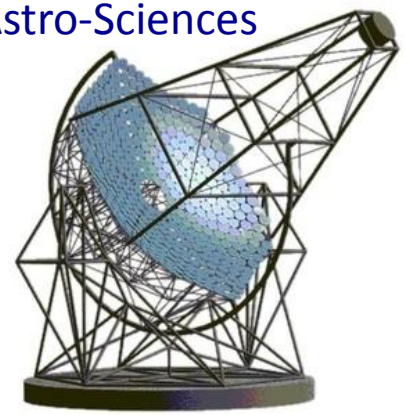
Fundamental information science

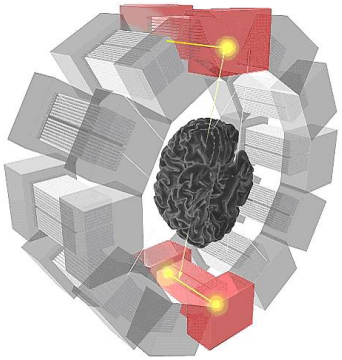


Other large scale projects with similar requirementas



Astro-Sciences





Medical Diagnostics and Therapy

BOSCH

Life perspective in industry for physics students

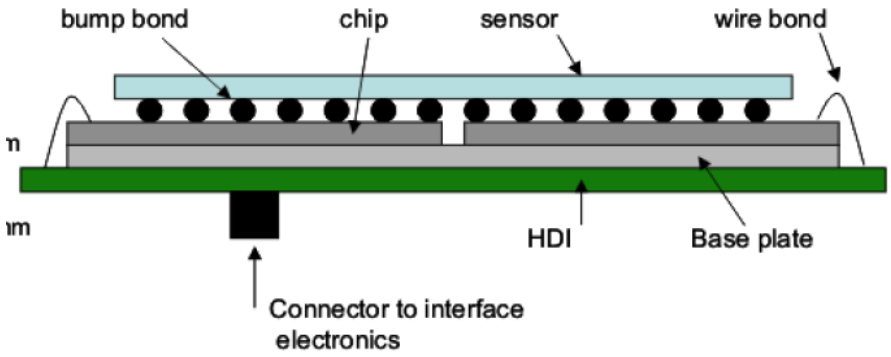
Electronics as an academic subject in

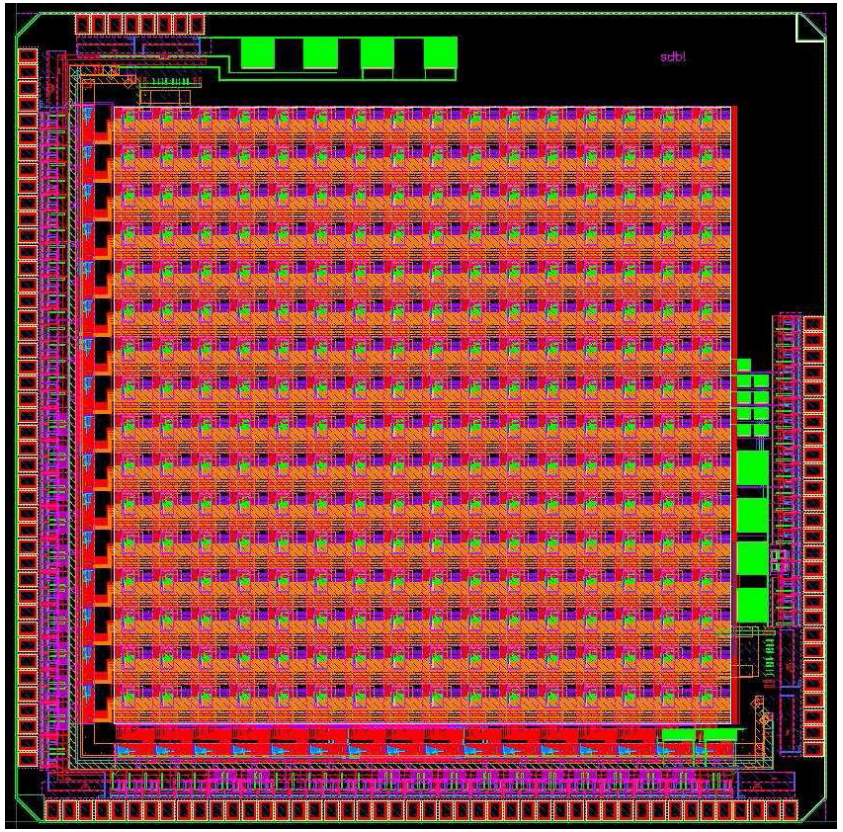
AGIPD (Adaptive Gain Integrating Pixel Detector) for XFEL (DESY)

DESY Hamburg und Bonn University

Challenges

- high dynamic range (1 - 1.4 x 10^4)
- single photon sensitivity,
- long storage chain (≥ 200)
- long hold time (99 ms)
- high radiation dose (up to 100 MGy)





Prototype test chip with a 16 x 16 pixel matrix
130nm (IBM cmrf8sf DM) CMOS technology
10 x 10 storage cells / pixel.

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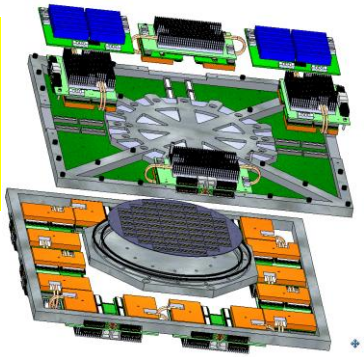
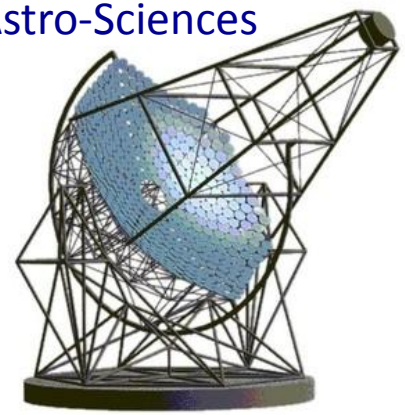
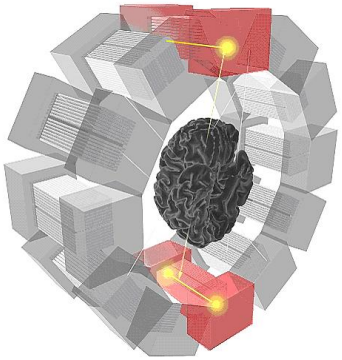


Other large scale projects with similar requirementas

Astro-Sciences



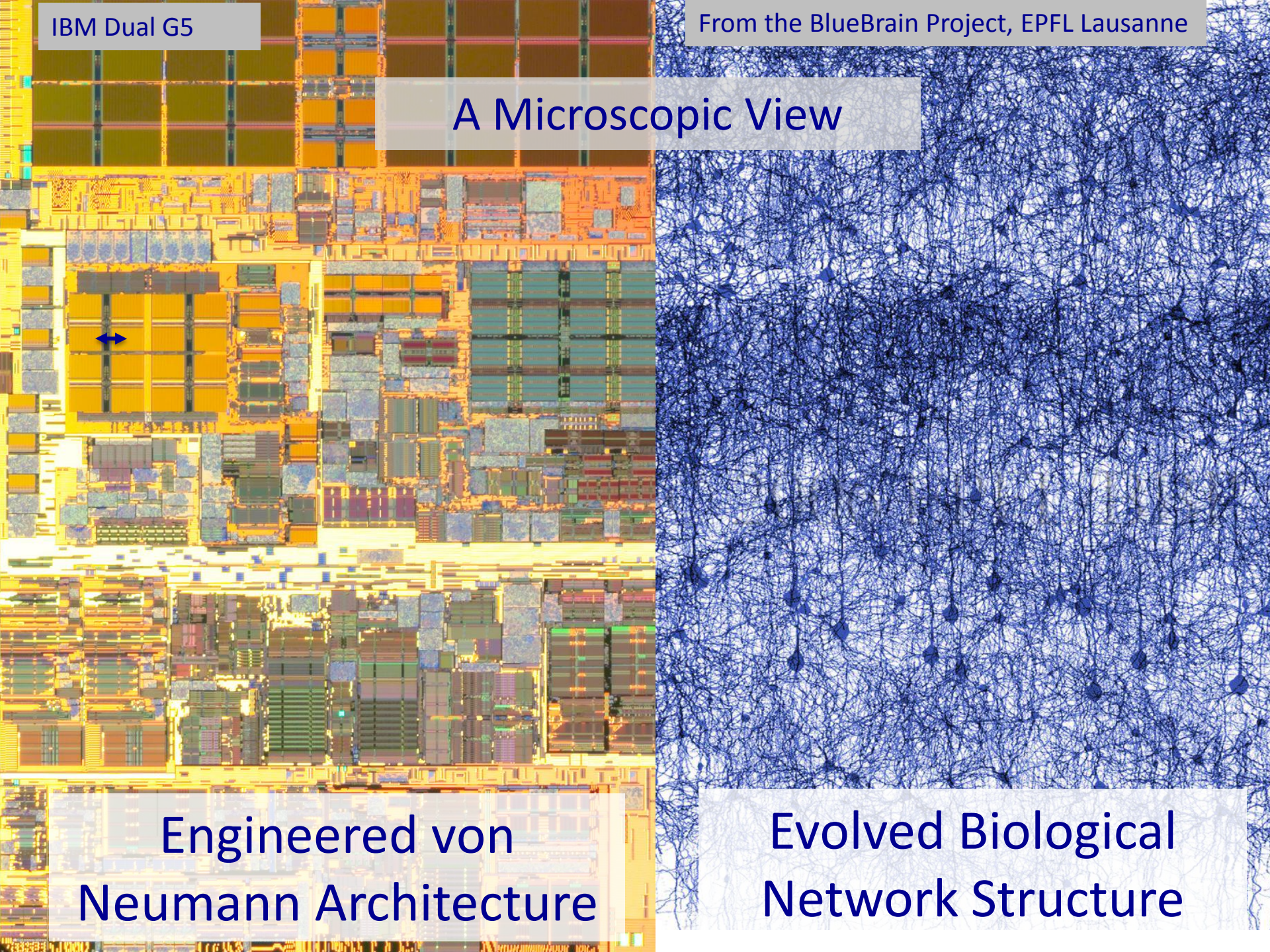


Medical Diagnostics and Therapy

BOSCH

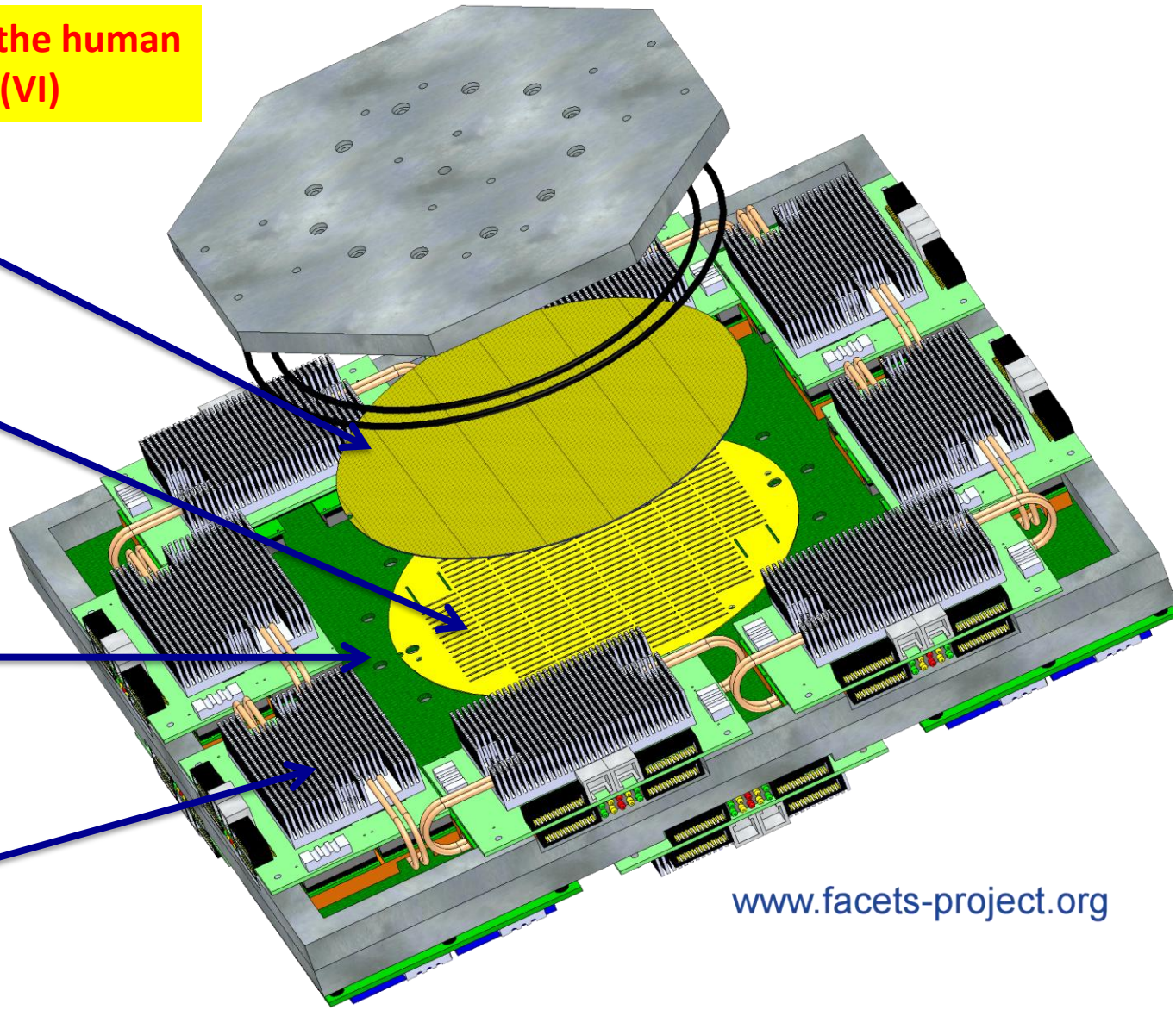
Life perspective in industry for physics students

Electronics as an academic subject in

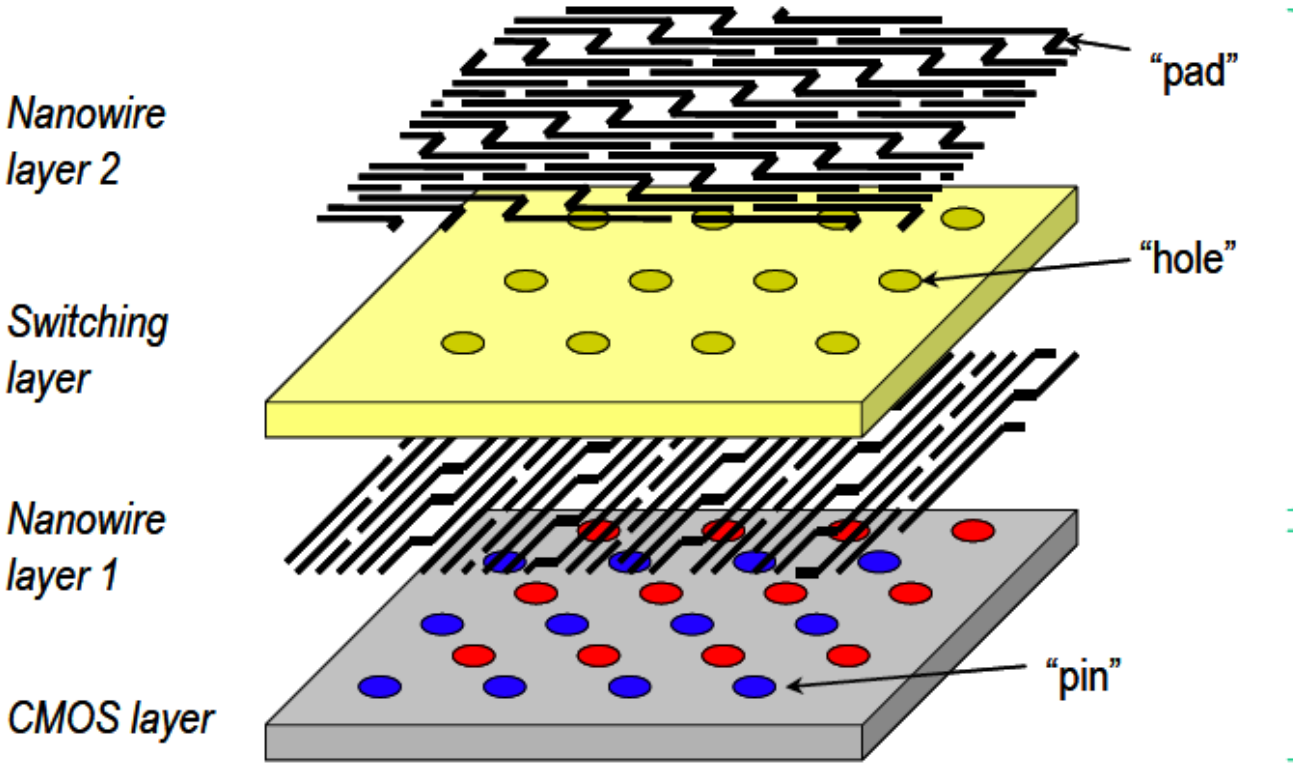

IBM Dual G5
From the BlueBrain Project, EPFL Lausanne
A Microscopic View
Engineered von Neumann Architecture
Evolved Biological Network Structure

Neural Processing Unit, 200.000 Neurons, 50.000.000 Synapses
Demonstrate self-organized, fault tolerant, low power, acceleratred information processing

Approx. 1/10.000 of the human visual system (VI)



HP FPNI : Field Programmable Nanowire Interconnect



@ 0.1 F_{CMOS} = 100x CMOS

Nano redundancy → defect tolerance
Small size, high yield → low cost
Low energy

G. Snider et al, IEEE Trans. Nano (2007)

Joining reliable CMOS and faulty nanoelectronics

Concluding Remarks

- Universities can and do drive advanced electronics development

- Their strengths are : Independent thinking and excellent students

- Their weakness is : Maintaining and developing infrastructure

Ways out :

- Joint efforts : National (HGF Alliance) and EU (e.g. AIDA)

- Export knowledge in other fields