Front end electronics for Hybrid Avalanche Photo Diode

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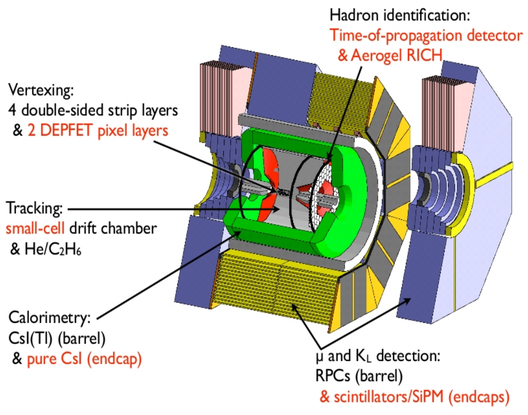
Motivation

Belle II experiment:study of rare B and D meson decays

For the upgrade of the Belle detector (Belle-II) at the KEK collider, we are developing a proximity focusing ring imaging Cherenkov detector using aerogel as radiator, which will allow efficient separation of kaons from pions (4σ) in the wide range of particle momenta up to 4Gev/c.



Proximity focusing Aerogel RICH

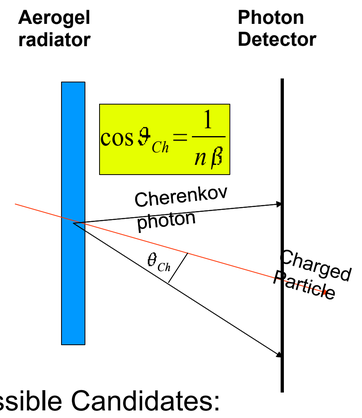
- The elements :
  aerogel radiator
  expansion volume
  position sensitive photon detectors
  photon detector read-out system
- Number of detected photons/ring

$$N_{det} = \frac{\alpha}{\hbar c} L \int \sin^2 \vartheta_{Ch} T \varepsilon \, dE$$

- **Design goal**: Separation power at 4 GeV/c where for n=1.05

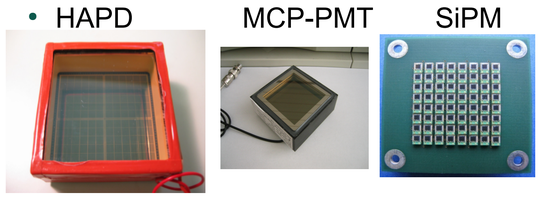
$$\vartheta_{Ch}(\pi) - \vartheta_{Ch}(K) = 23\,mrad$$

- Requerments for the photon detector:
  - Operation in high B (1.5T)
  - Position resolution: pad size ~5mm



Possible Candidates:

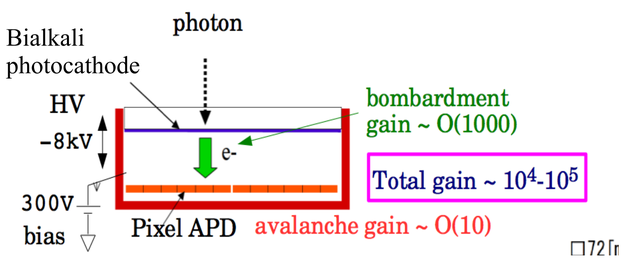
- HAPD
- MCP-PMT
- SiPM



Baseline design

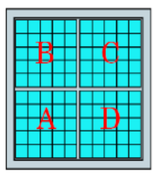
Hamamatsu Hybrid Avalanche Photo Diode (HAPD)

•Principle of operation:

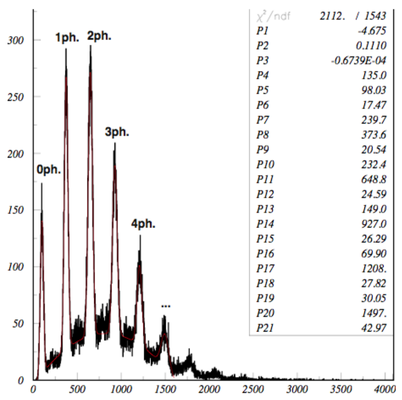


•Specif cations:

Package	72x72mm2
Typical QE	25%
No. of pads	12x12
Pad size	5x5mm
Photosensitive area	67%
Gain	~10000
Bias Voltage	350V
I(leak)	30nA

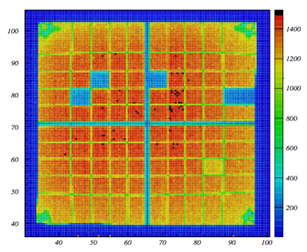


4 chips in HAPD



Pulse height distribution:

•Excelent separation



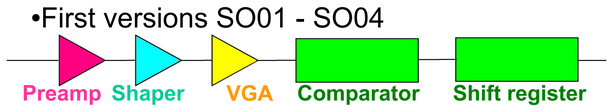
2D response of the HAPD to the perpendicular light beam.

Electronic readout

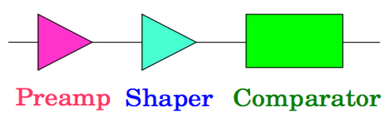
The HAPD readout will consist of 4 readout chips and an FPGA which will allow efficient data compression and transfer. The design has to take into account very limited space available and very harsh environment. The analog signals from HAPDs will be first fed into Asic chips having amplification, shaping and comparator capabilities for 36 channel per chip.

•Asic development

•First versions SO01 - SO04

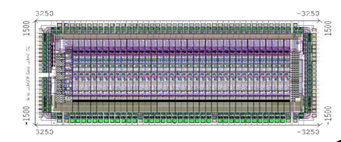


- Next iterations SA01 - SA02 without shift registers
  - Better S/N
  - 36 channels/chip
  - two kind of comparators
  - shaping time adjustmen
  - gain reduction



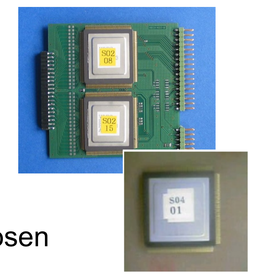
SO01 Specif cations:

•Production at VDEC (Tokyo Univ)
•Process: ROHM CMOS 0.35 um
•Noise Level: 1200e @ 80pF(HAPD)
•Std. Input Signal: 12000 e
•18 ch/chip
• Readout: Pipeline with shift register
•S/N = 10
•Power Consumption = 3 mW/ch
•Shaping time 0.3 ~ 2.0 us
• Variable gain 1.25 ~ 20
•Individual offset adjustment.

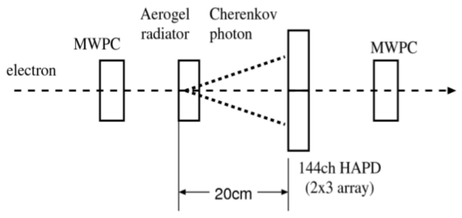


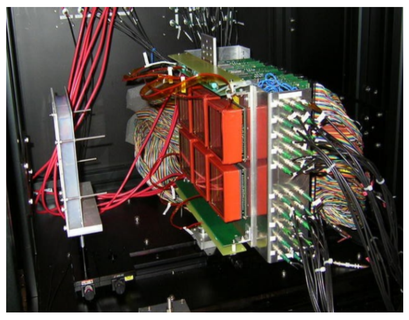
Beam test

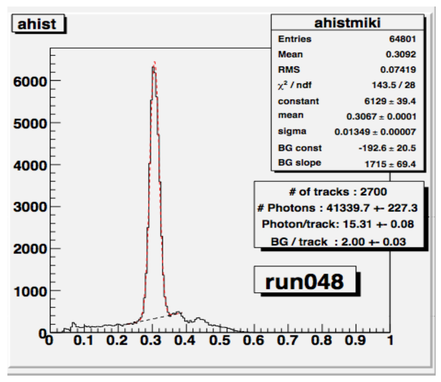
Setup

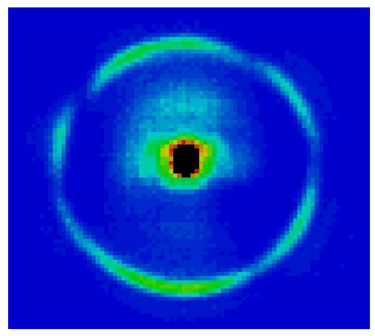


• Electron Beam p=2GeV/c
• Tracking using 2 MWPC
• 2 × 3 array of 144 ch HAPD
• HV at –7kV.
• Bias voltage of HAPD is chosen at avalanche gain = 40.
•Readout: 48 ASICs SO version.
•ASIC offset is adjusted so that the noise is below the threshold.
•Threshold ~ 0.5 photo electron level
•Aerogel radiator
n1 = 1.054,n2=1.065,
d1= d2 = 2cm
Transmission length @ 400nm: 47mm and 55mm,







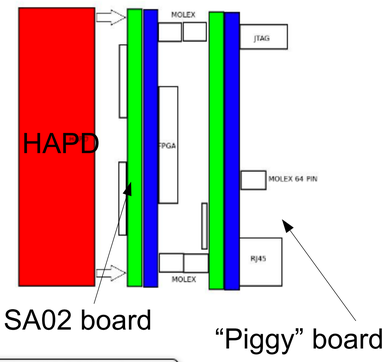


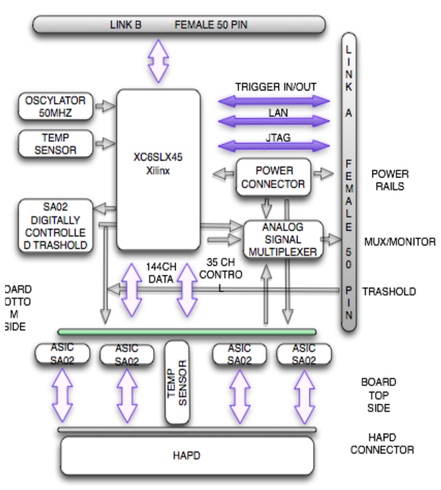
•Clear Cherenkov ring is observed!
•15.3 photo-electrons per track.
•Resolution 13.5 mrad per photon
•Single track resolution 5.7 mrad corresponding to 6.7σ Kaon/Pion separation

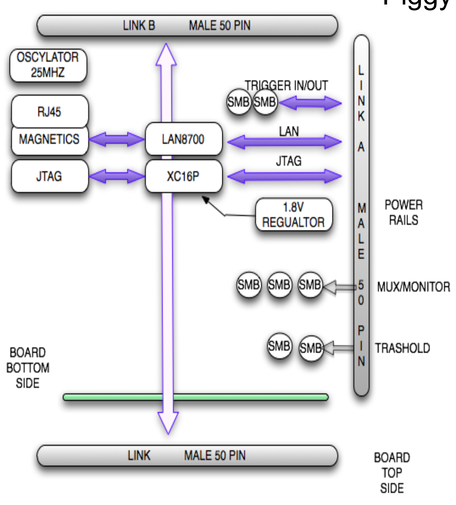
SA02 board design

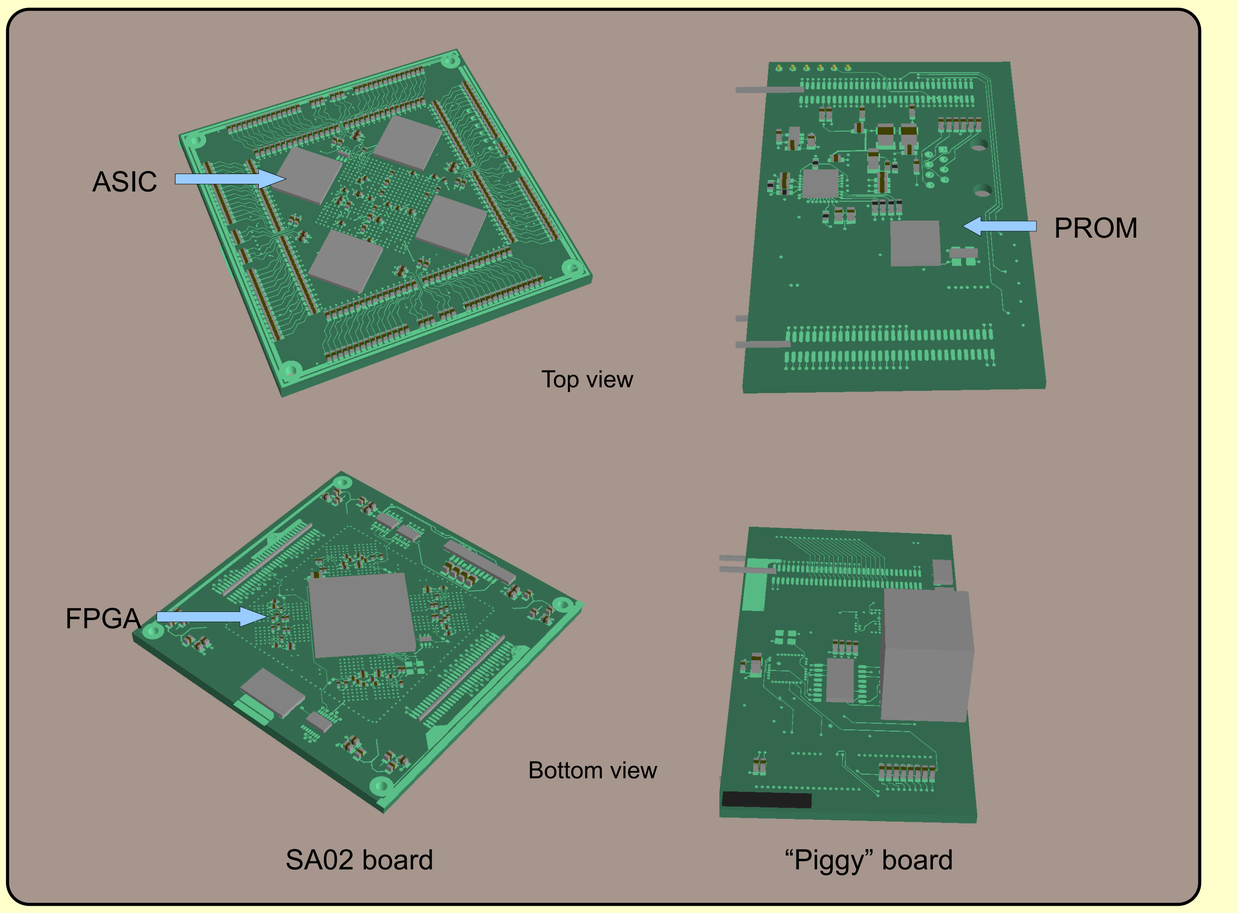
Requirement: 5cm space behind the photon detector

Implementation:
•Single board with four SA02 ASICs and Spartan6 FPGA
•Health monitor
•Easy adaptable communication and programming with Piggy back board
•LVCMOS 33IO, Ethernet SiTCP









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