Design and Verification of a Bit Error Rate Tester in Altera FPGA for Optical Link Developments

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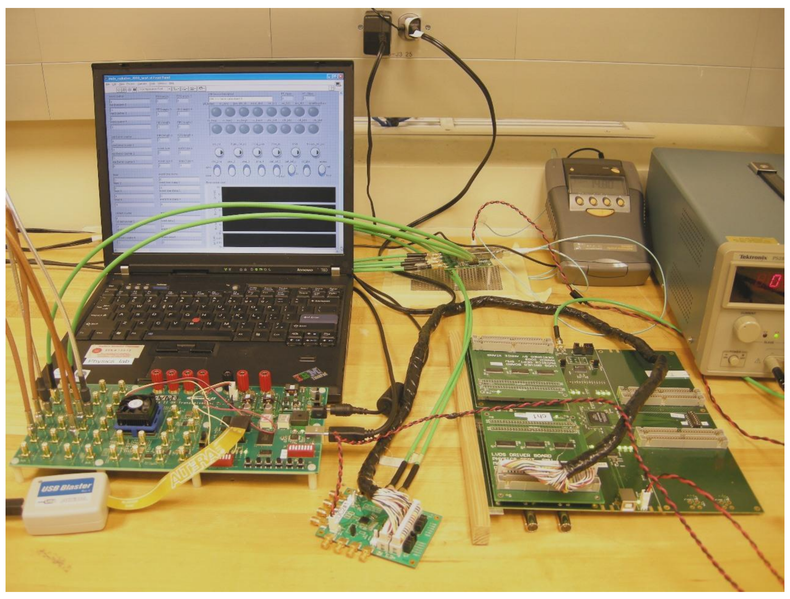
Introduction

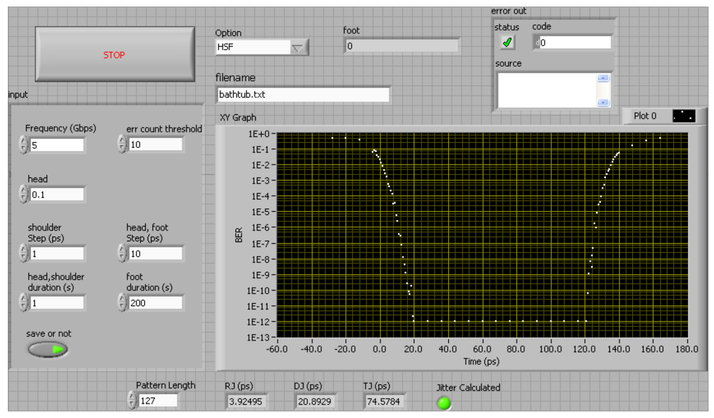
Multi-gigabit per second serial optical links are widely conceived to support data transmission in future particle physics experiments. In order to qualify components and verify link designs, their performances need to be evaluated in the laboratory and sometimes in a radiation environment. Bit Error Rate (BER) testing is the fundamental measure of the integrity of each digital communication link. It traditionally requires expensive equipment with table-top testers. With the integration of high-speed SERDES inside FPGA, the embedded solution provides a cheaper alternative with the flexibility of customization to fit field irradiation test scenarios .

We develop a test bench based on Altera' s Stratix II GX Transceiver SI Development kit. A parallel to serial PRBS generator and a bit/link status error detector are deployed to characterize serial data link performance. The auto-correlation pattern generates long stress signals without using a lot of memory and enables receiver synchronization without specifying protocol at the physical layer. An error logging FIFO records both bit error data and link operation events. An optimized data flow is established to maximize throughput with shortest dead time. The tester operates up to 6.5 Gbps in 4 duplex channels

Test Bench



Signal Integrity



- FPGA embedded transmitter and receiver are characterized by eye diagram and BER scan measurements.
- Jitter contributions of link components are derived as following

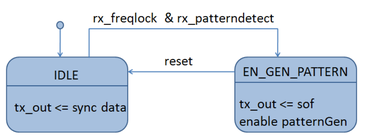
$$DJ_{sys} = DJ_{TX} + DJ_{RX} + DJ_{CH}$$

$$RJ_{sys} = \sqrt{RJ_{TX}^2 + RJ_{RX}^2 + RJ_{CH}^2}$$

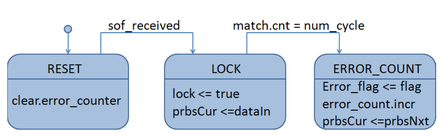
Characteristic

- VHDL codes and LabVIEW VIs are developed for the tester. The former governs the data flow logic functions and the transceiver hardware. The latter provides user GUI and remote access of test operations.
- A Pseudo Random Bit Sequence (PRBS) generator produces long stress patterns without using a lot of memory. PRBS also enables the link re-establishment from transmitter or receiver separately, independent of protocol at the physical layer.
- The tester operates up to 6.5 Gbps in 4 duplex channels with analog parameters, preemphasis, equalization, DC gain, and VOD adjustable during run-time.

Pattern Generation State Machine



Data Verification State Machine

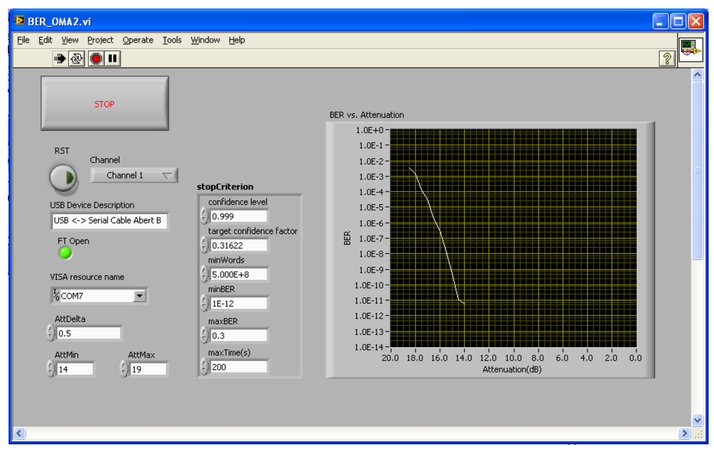


Error Logging

- Commercial BERT IPs generally do not provide enough data acquisition capability for SEU analysis.
- In our tester, we implement an error logging FIFO that records both bit error data and link operation events. Five types of events are logged as shown in the table below.
- The recorded time stamp and XOR pattern of received and expected data can reproduce transmitted and received data, given the pattern is a known PRBS.
- When a link-lost event occurs, it is always time stamped and logged in the reserved portion of the FIFO.
- Currently, the error log FIFO is 4K in length, 12 byte in width, with a throughput of 5Mbps.

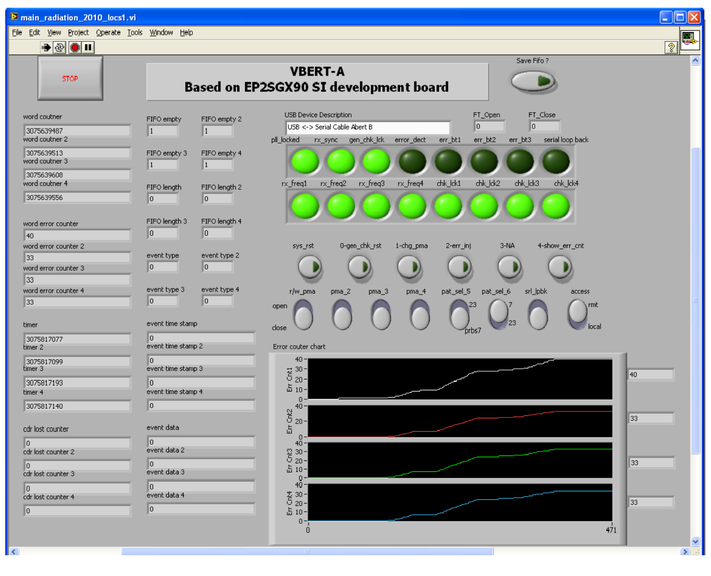
Event	Event flag	Time stamp	Event data	Note
SEE	001	48bit	XOR	
Locked	010	48bit	Exp'd data	Error detector locked to generator
Link Lost	011	48bit	Exp'd data	Receiver CDR lost synchronization
FIFO Full	100	48bit	Exp'd data	Stop recording SEE events
FIFO Ready	101	48bit	Exp'd data	Resume recording SEE events

Basic BER



- The above LabVIEW GUI shows the results of a basic BER vs. optical power. A variable optical attenuator is inserted in the fiber loop to induce transmission degradation.

Irradiation Test



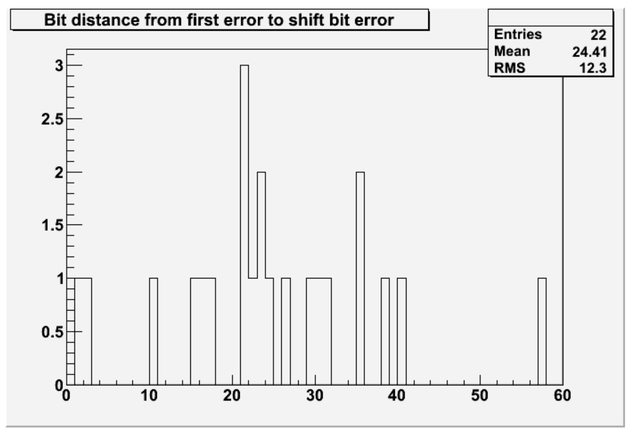
- The above LabVIEW GUI is implemented during a proton beam test for a 5Gbps serializer developed at SMU.

Irradiation BER Result

- Proton beam: 200 MeV at IUCF.
- Flux: stepped from 1.3×10^{7} to 1.4×10^{10} proton/cm^2/sec.
- Fluence: 2.3×10^{14} proton/cm^2, corresponding to 13 Mrad(Si) total dose.
- Two serializer chips inside the beam with incidence angle 0, 30, 45 and 60 degrees with respect to the normal of the chip surface. A third chip outside the beam as reference.
- No error was observed with flux up to 3.0×10^{9} proton/cm^2/sec. When flux reached 1.4×10^{10} proton/cm^2/sec, a few errors occurred in both channels under irradiation.
- Taking the operating condition at the ATLAS liquid argon front-end crate location in sLHC as an example, the upper limit of the error cross section translates to a proton induced bit error rate of 6×10^{-18}.

Error Type	Synchronization Error		Single-Bit Error	
Module ID	6	12	6	12
Number of errors	8	17	5	0
σ(cm^2)	3.4×10^{-14}	7.3×10^{-14}	2.1×10^{-14}	4.3×10^{-15}

SEE Analysis



- Post-test analysis shows that two types of SEE events occurred during high flux irradiation run.
- One type of SEE event is single bit flips, with 0 – 1 or 1 – 0 transition. The other type of SEE event display itself as exact one bit shift forward or backward, after a period of error propagation.
- Error propagates are constrained within two frame clocks as shown in the plot above.

Availability and Updates

- Reference designs are available for interested users. Please contact corresponding author with a short description of intended application.
- In near future updates, auto-resynchronization will be enabled to avoid needing the attention to reset system during long irradiation runs.
- FIFO data acquisition will be implemented on more interfaces such as Ethernet and high-speed serial port.

Summary

- A customized Bit Error Rate test bench using FPGA with embedded transceiver is demonstrated.
- The test bench implements PRBS generator and detector to product long stress patterns and error logging FIFO to record both bit error data and link operation events.
- The test bench is used in a proton test on custom serializer chips where two types of SEE events are recorded. Besides single bit flip, the other type of error is analyzed and determined to be single bit shift.

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