Universitat de Barcelona

Institut de Ciències del Cosmos

Wideband pulse amplifier for the integrated camera of the Cherenkov Telescope Array

E. Delagnes[a], A. Sanuy[b], D. Gascón[b]

on behalf of the **NECTAr** collaboration

Irfu /CEA/Saclay [a]

LPNHE / Paris

LPTA / Montpellier

ICC / Universitat Barcelona (ICC-UB) [b]

TWEPP – Aachen – September 21th 2010

Outlook

I. Introduction

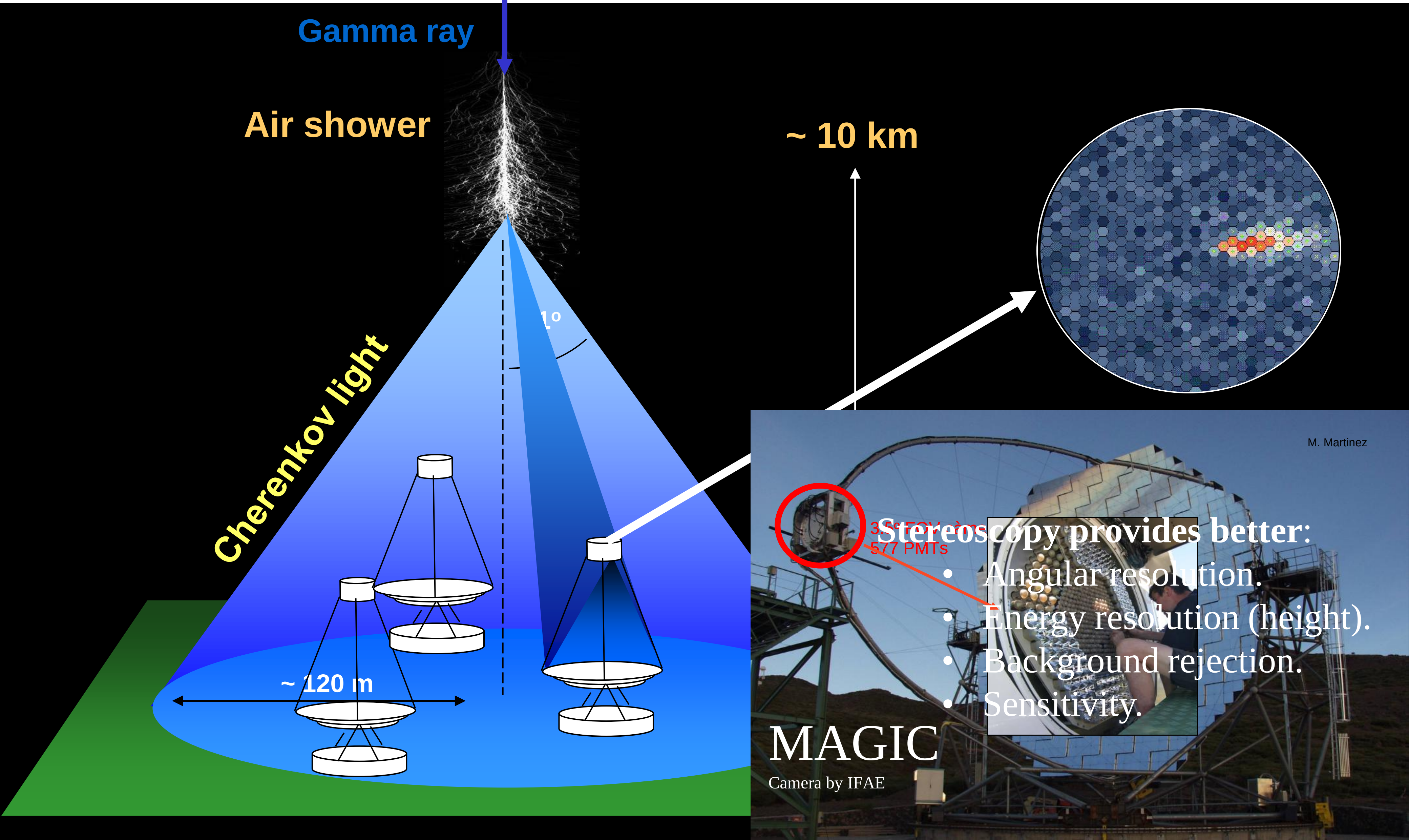
II. Basic building blocks

III. First prototype: *ACTA*

IV. Second prototype: *ACTA3*

V. Summary

I. Introduction: Cherenkov telescopes

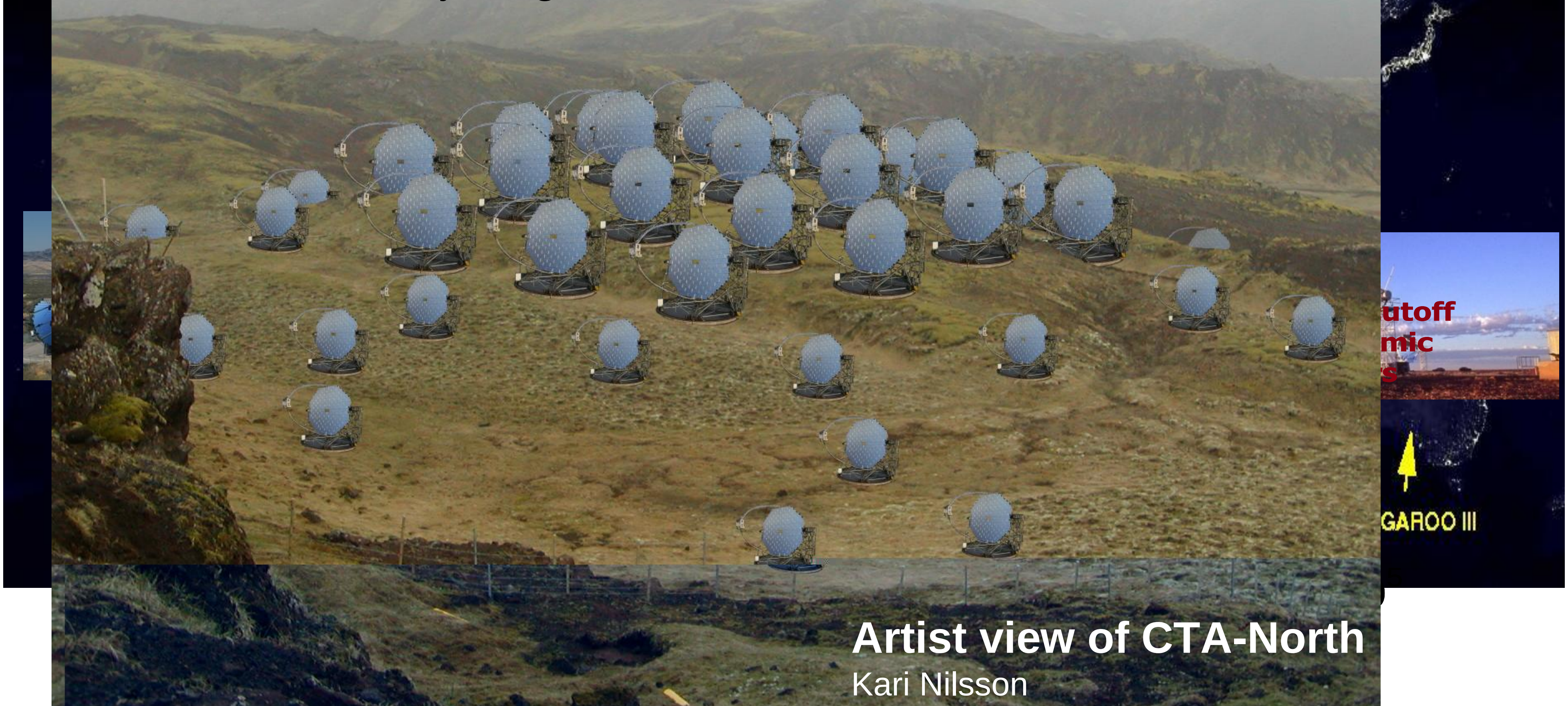


Stereoscopy provides better:

- Angular resolution.
- Energy resolution (height).
- Background rejection.
- Sensitivity.

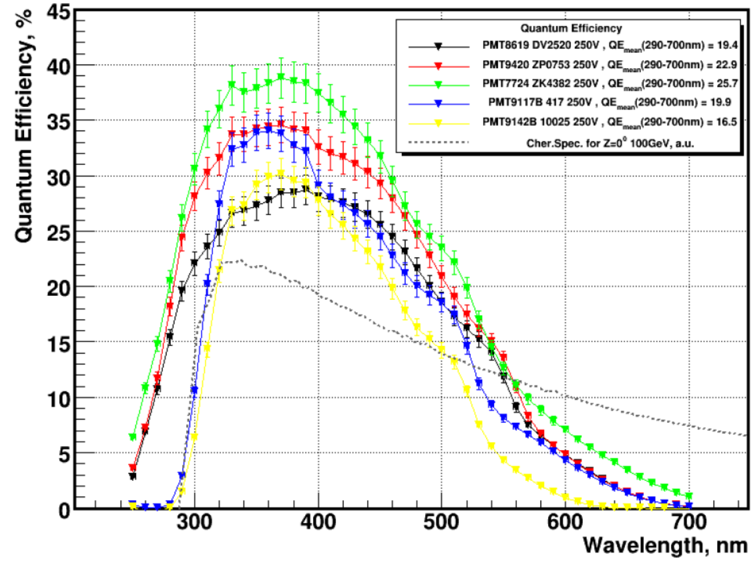
I. Introduction: the Cherenkov Telescope Array (CTA) observatory

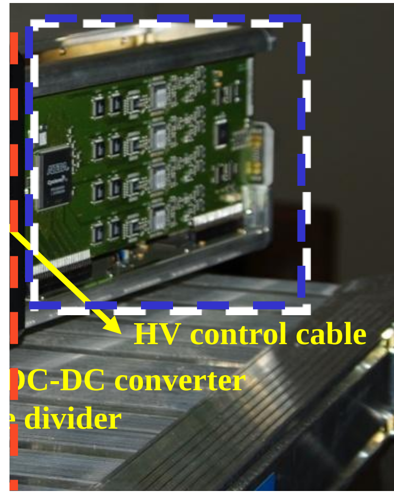
- How CTA aims to extend energy range and increase sensitivity?
  - Large array (>1 km^2)of Cherenkov telescopes (50-100)
  - Different sizes: dish from 6 to 24 m
- Camera and electronics must be optimized in terms of
  - Performance
  - Cost and reliability: integration



Artist view of CTA-North
Kari Nilsson

I. Introduction: the camer





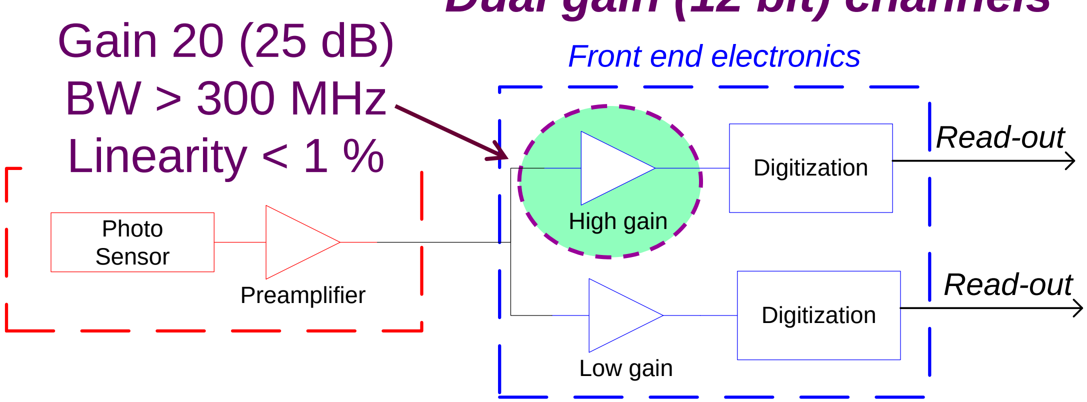
HESS cluster

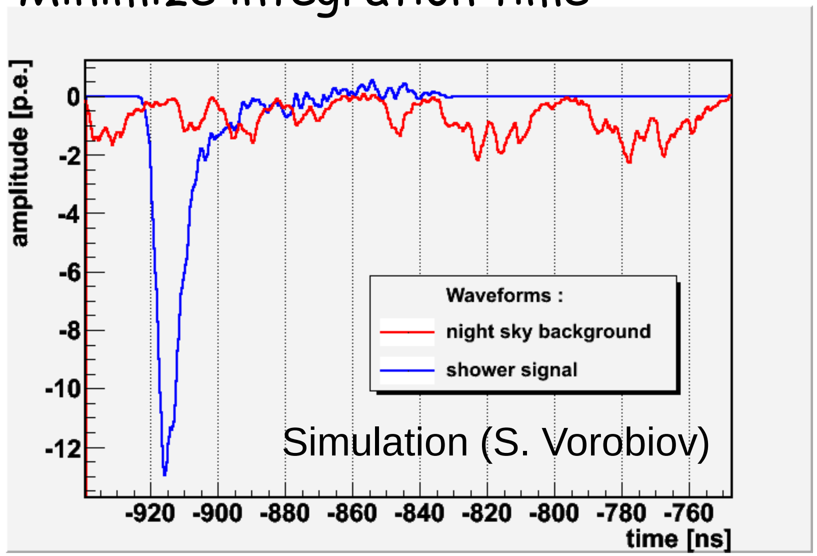
- Front end electronics:
  - Pixel: fast phototosenrors
    - High QE PMTs // SiPM
  - Modularity: cluster of 7/8 p
  - Front end electronics in the
  - Digitization & trigger

- High BW (>300 MHz):
  - Night Sky Background:
    - Up to 100 MHz
  - Minimize integration time

- Huge dynamic range: 16 bits
  - Signals up to 6 Kphe
  - Single phe resolution for calibration:
    - Series noise < 3 nV/√Hz

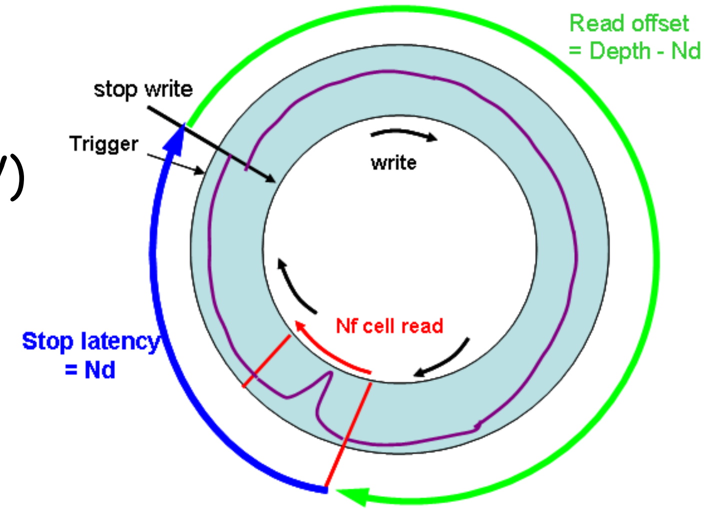
Dual gain (12 bit) channels



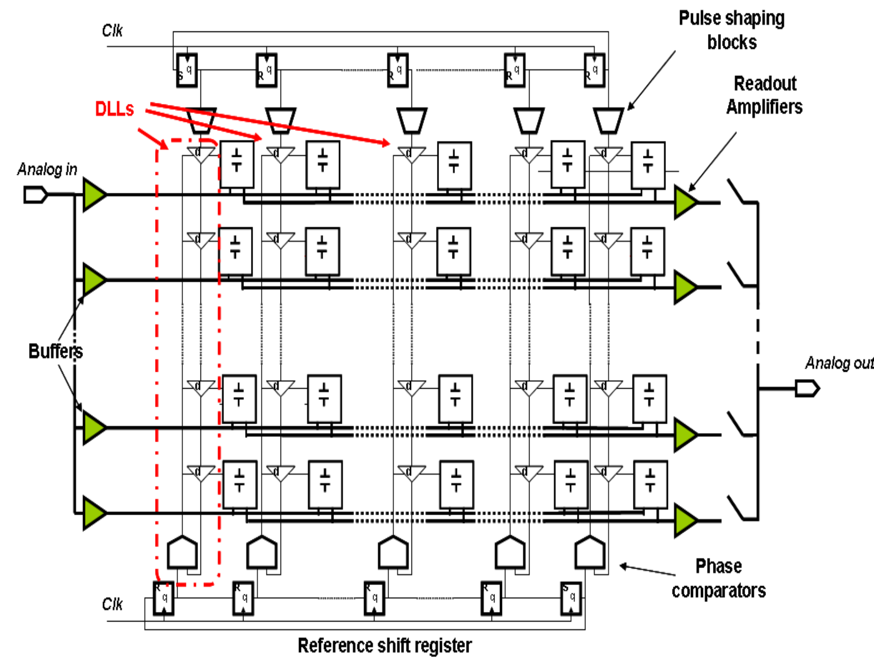


I. Introduction: readout electronics

- Analogue memory + slow digitization
  - Sample and hold in a capacitor array
    - High speed: up to 3 GS/s (> 300 MHz analogue BW)
  - Slow digitization for selected events
    - Trigger system
  - Custom ASICs developed in the community
    - Domino Ring Sampler (DRS) by PSI
      - For CTA: **DRAGON** poject
    - Sampling Analogue Memory (SAM) by Irfu
      - For CTA: **NECTAr** project



- Flash ADCs
  - Commercial component
  - Limited to 500 MS/s
    - High Cost and power consumption
    - For CTA: FlashCam collaboration
      - No trigger needed

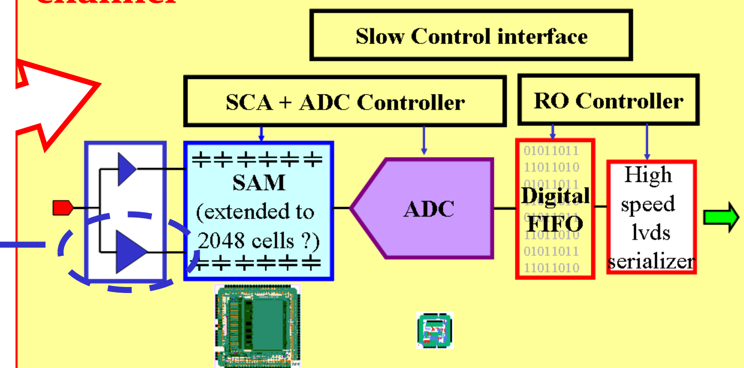


I. Introduction: NECTAr (Irfu/Saclay, LPNHE, LPTA and ICC-UB)

- From HESS chip (SAM: only analogue memory) to a single chip integrating full acquisition channel:

Accuracy	1-3 %
Bandwidth	400 MHz
Output range	1.5 to 2 Vpp
Gain	20
Temp. Coeff.	< 0.05 %/K
Power	< 50 mW
Slew rate	1500 V/µs
Series noise	< 3 nV/√Hz
Fully differential	

Chip 1 = full integrated acquisition channel



- **Input signal amplif. (2 gains),**
- **Analog memory (depth adapted to CTA trigger latency)**
- **ADC Wilky (already exists),**
- **FIFO**
- **Sérializer ~300Mb/s.**

AMS CMOS 0.35 um

- SAM technology

Outlook

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II. The circuit

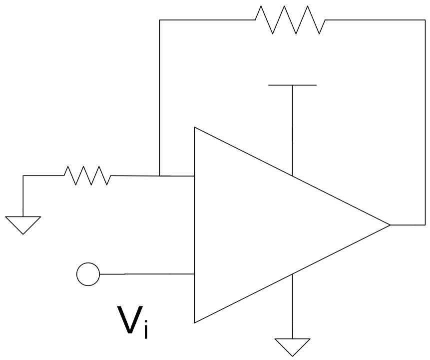
III. First prototype: ACTA

IV. Second prototype: ACTA3

V. Summary

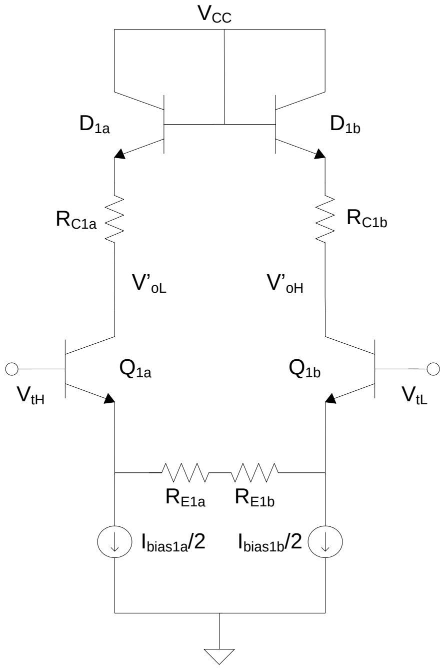
II. The circuit: classical topologies for linear voltage amplifiers

- Global feedback



  - Good linearity
  - OpAmp with GBW > 8 GHz !!
    - Reported: < 1 GHz in 0.35 um
    - Very difficult even with VDSM

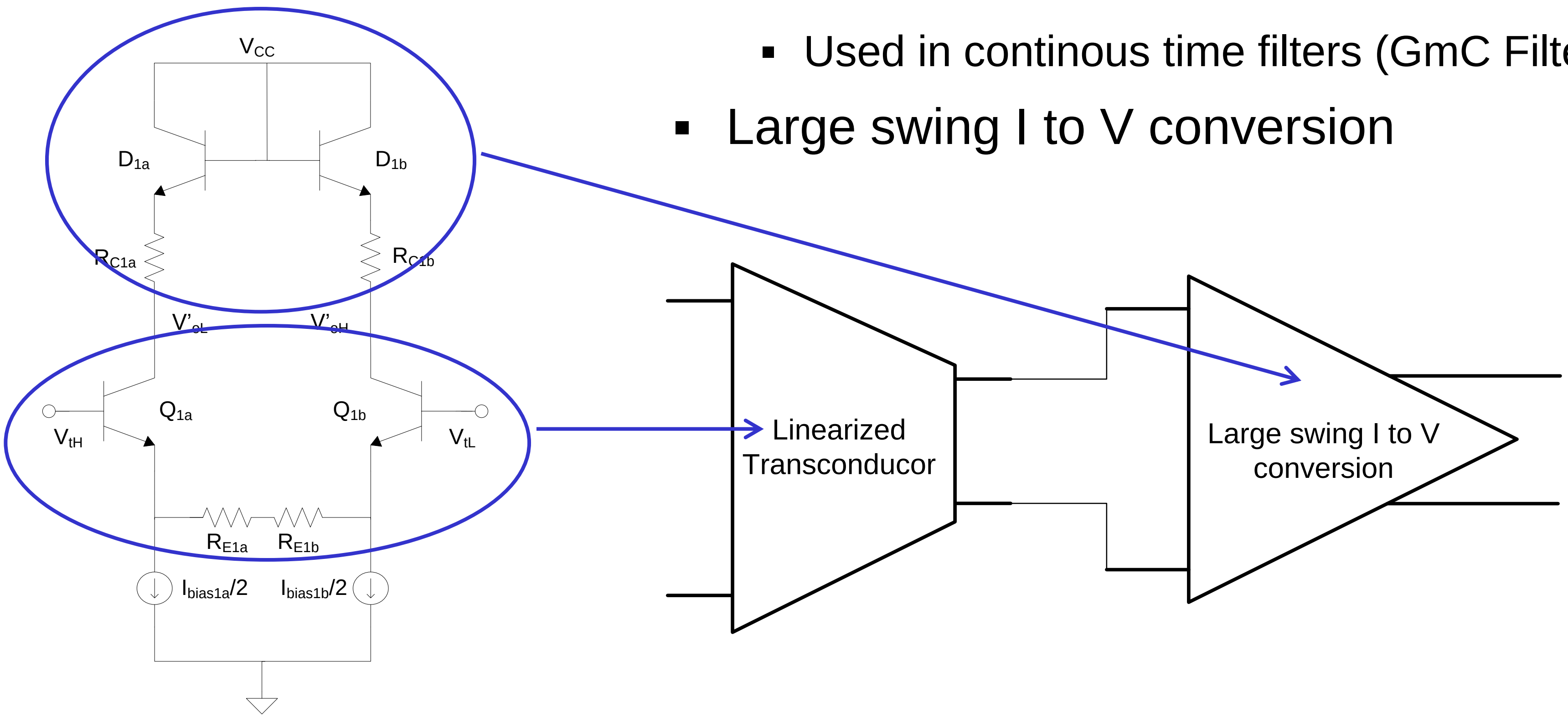
- Bipolar style “open loop”



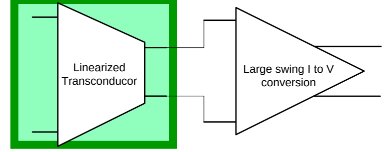
  - Limited linearity
  - Dynamic of 2 V impossible @ 3.3 V

II. The circuit: new approach

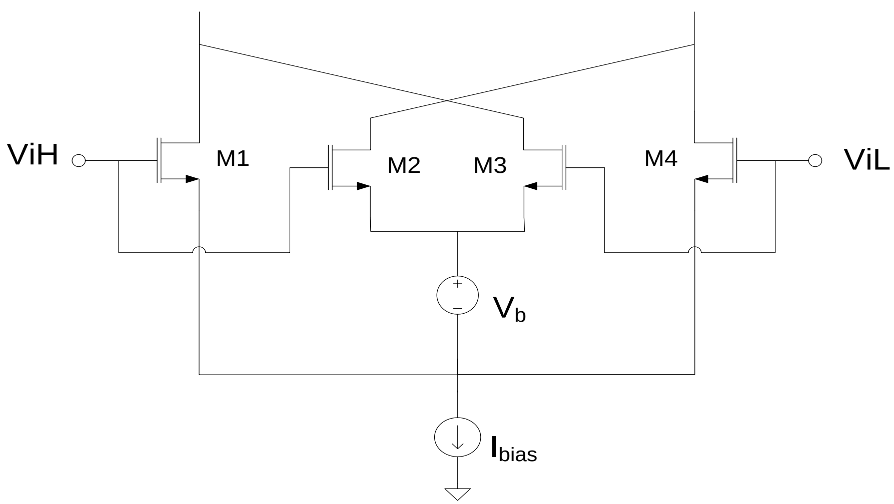
- Dedicated CMOS topologies
- Local feedback
  - Linearized HF CMOS transconductor
    - Used in continous time filters (GmC Filters)
  - Large swing I to V conversion



II. The circuit: bias-offset cross coupled differential pair



- Completely linear $$I_{oD} = K V_b V_{iD}$$ $$K = \frac{1}{2} \mu C_{ox} \frac{W}{L}$$
  - First order:
    - Linear using square law MOS: saturation $\longrightarrow$ $$|V_{in}| \leq \sqrt{\frac{I_{bias}}{K} - \frac{3}{4} V_b^2} - \frac{V_b}{2}$$
  - Tuneable gain
- Second order effects on linearity
  - Channel length modulation $\longrightarrow$ Control V_{DS} variations: next slides
  - Mismatch $\longrightarrow$ Large WL and common centroid
  - Mobility reduction $\longrightarrow$ Scaling M1-4 vs M2-3 (for a given G_m)
  - Body effect $\longrightarrow$ Cannot use PMOS (large K needed)

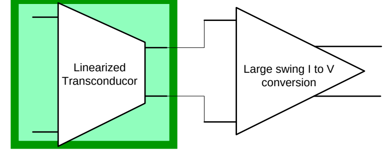


GBW & Noise

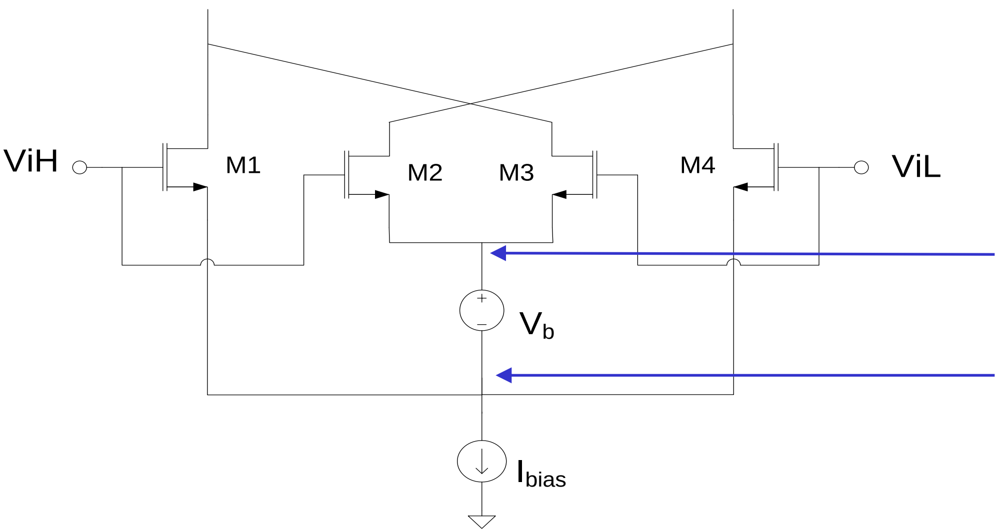
$$G_m = K V_b \geq 5\ mS$$

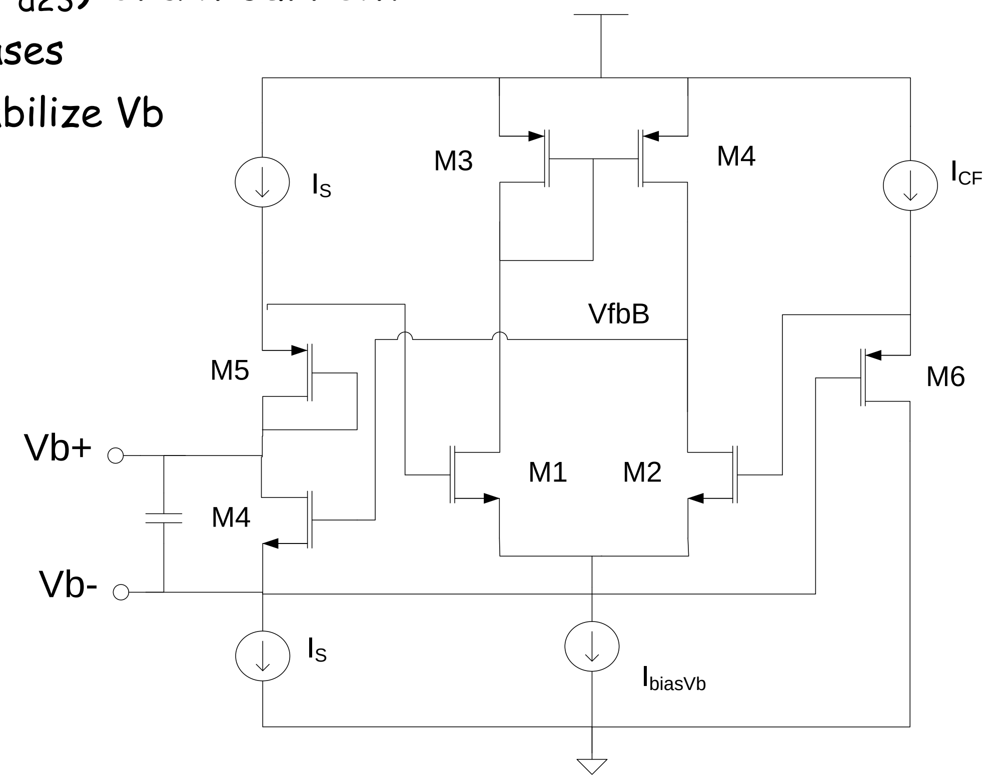
- L $\Rightarrow$ minimal (0.35 um)
  - Maximize GBW
  - Vds must be stable!
- W about 150 um
  - GBW and noise
  - Saturation

II. The circuit: floating voltage source

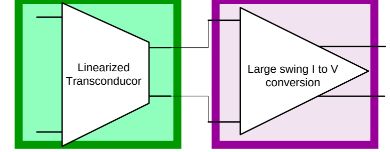


- A floating voltage source is needed (Vb)
- Bias voltage is offset in Vgs of two matched PMOS (M5 - M6)
  - Offset by different drain currents: Ib (fixed) vs Icf (control)
- In closed loop (negative feedback) to decrease r_{out} of Vb
  - Must be independent of M2/M3 (I_{d23}) drain current
    - Vgs of MP3 increases if Id23 increases
    - Error amplifier changes VfbB to stabilize Vb



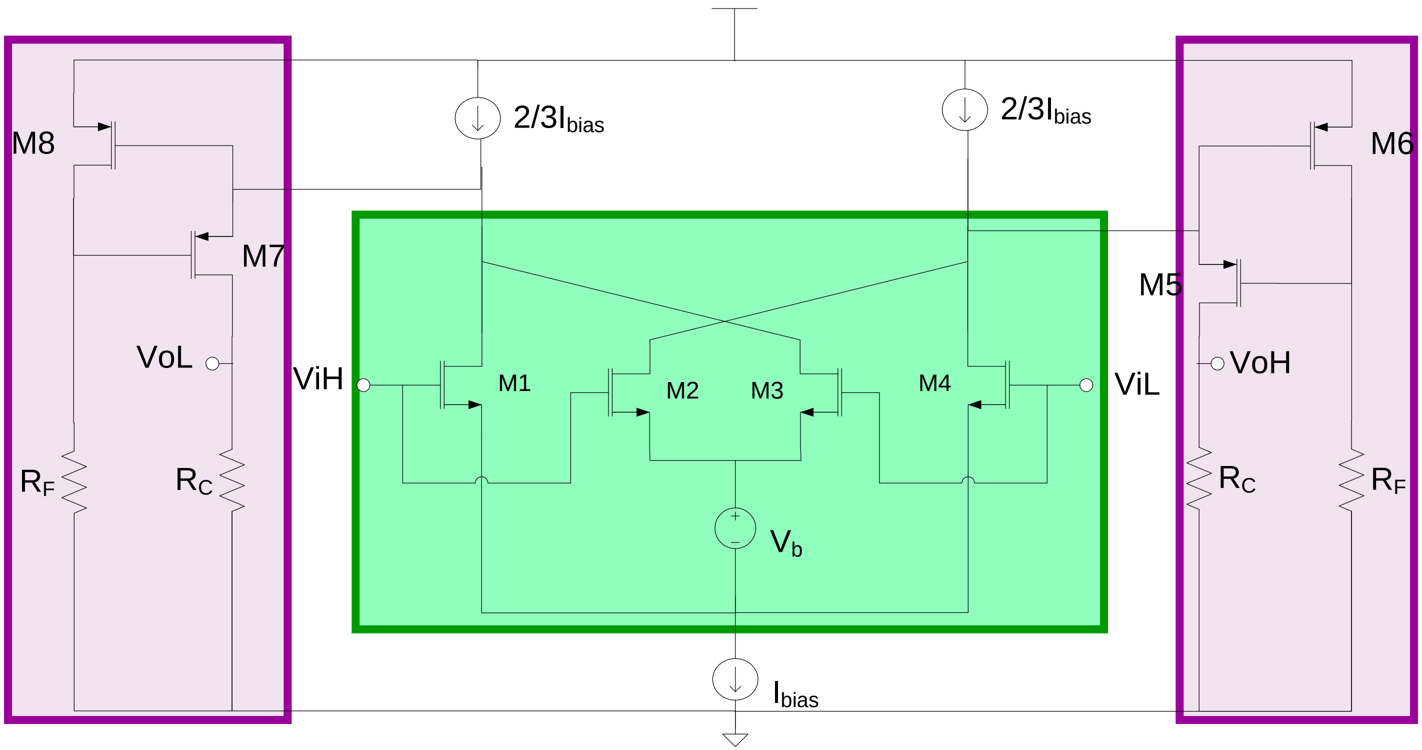


II. The circuit: folded regulated cascode common gate



- Regulated cascode
  - Folded: large voltage swing
  - Low input impedance
    - BW
    - Linearity
      - » Channel length modulation in input pair

R_C	< 1.5 KΩ	BW
Gm	> 5 mS	Gain (noise)
Ib	4 – 6 mA	Linearity
Vb	< 300 mV	Range



Outlook

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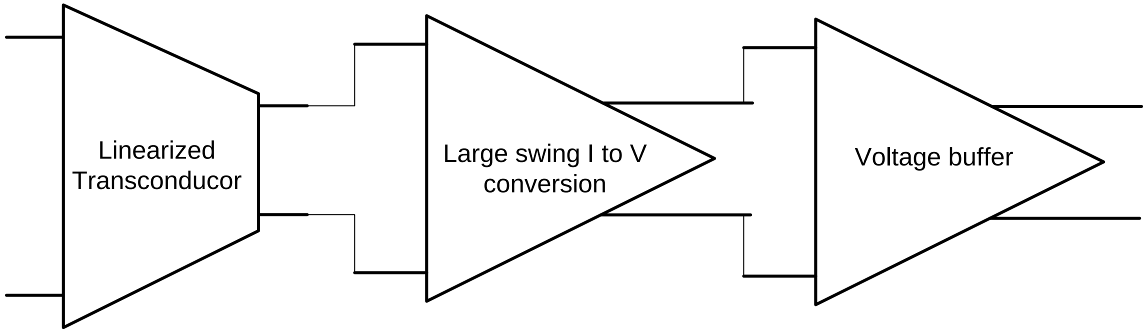
III. First prototype: ACTA

IV. Second prototype: ACTA3

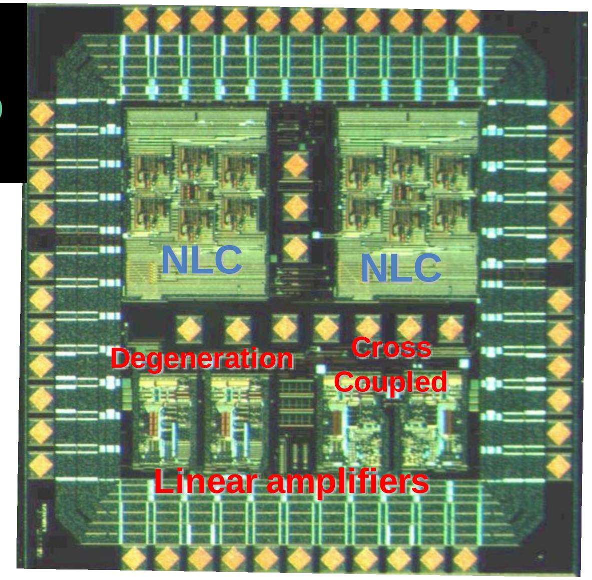
V. Summary

III. First prototype: ACTA chip

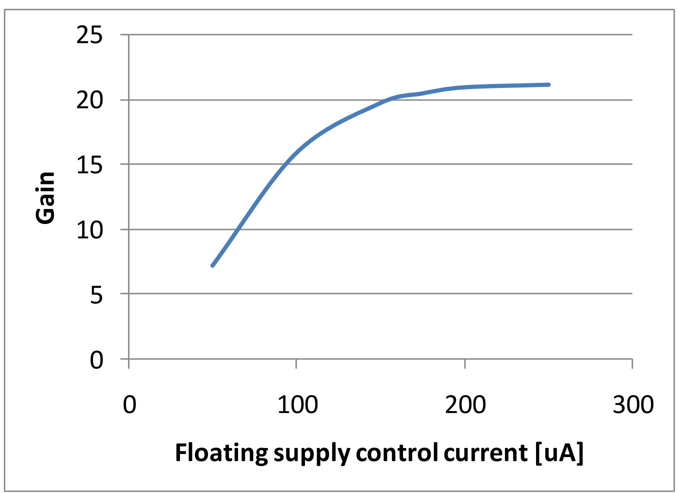
- First prototype (ACTA chip)
- Voltage buffer
  - Source follower



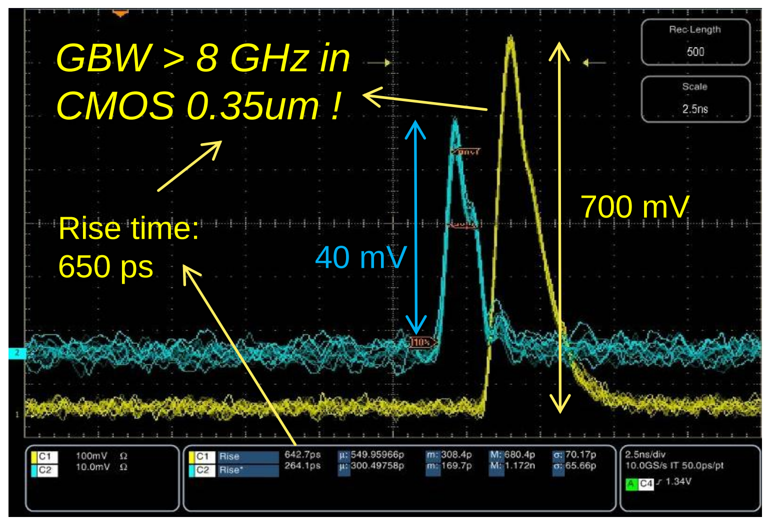
CMOS 0.35um
AMS 3 mm²
Submitted: July 20th 2009
Received: October 26th



- Gain tunable from 5 to 20

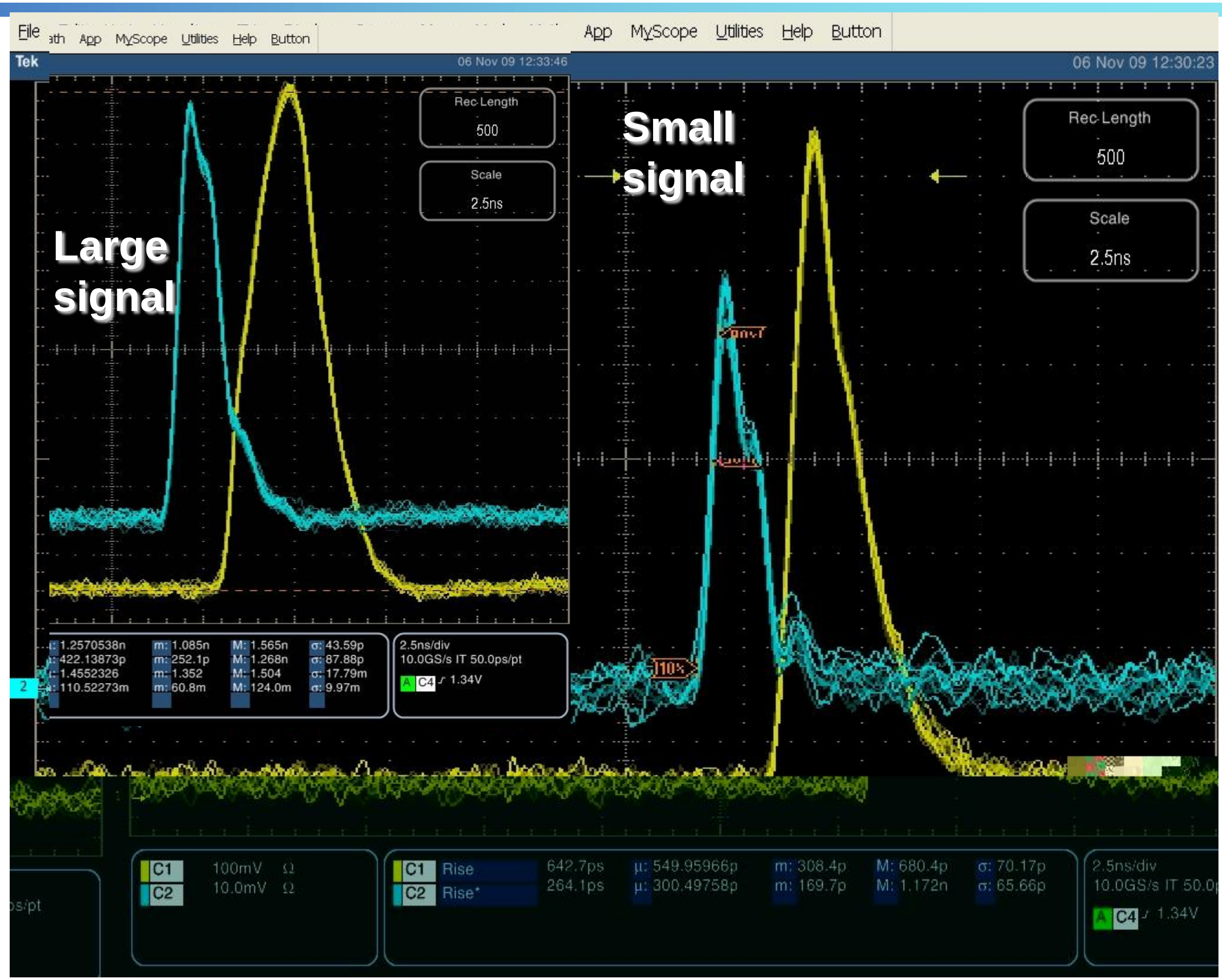


Results of the first prototype



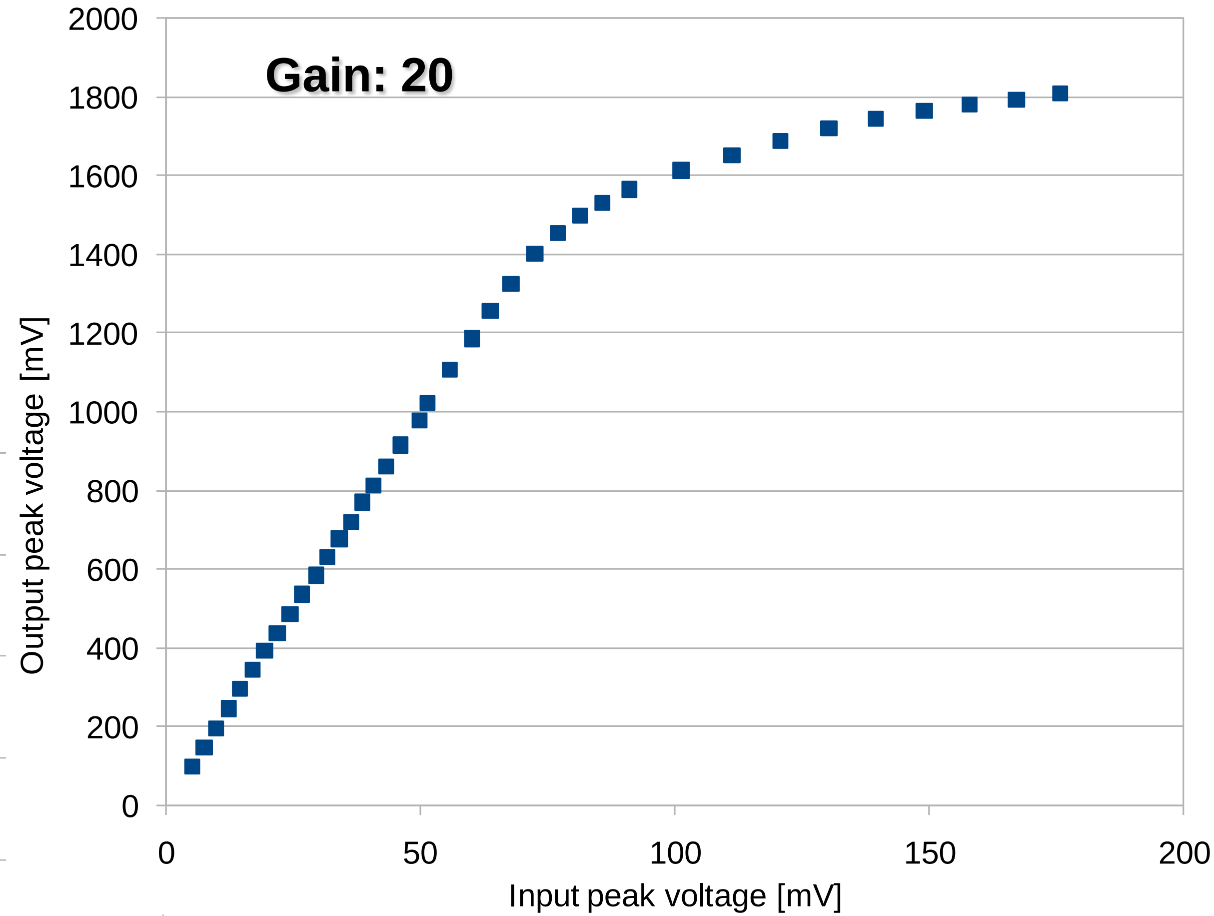
III. First prototype: ACTA chip

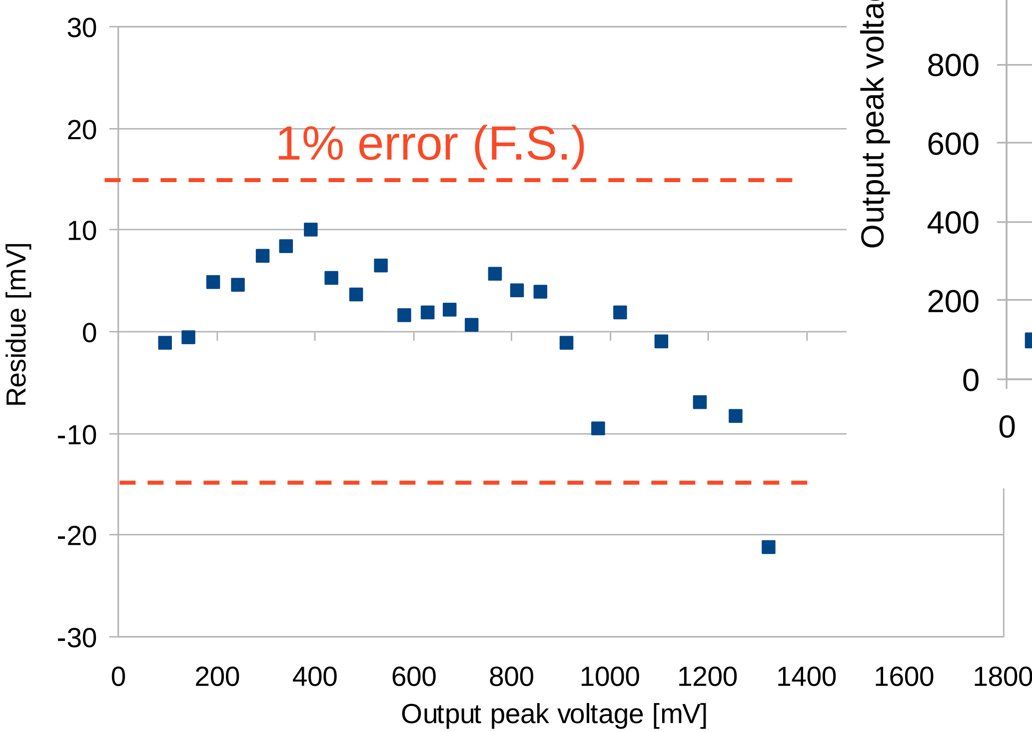
- Working
  - No ringing
  - Gain: 5 to 20
- Fast input pulse
  - Rise: 300 ps
- Output pulse
  - Rise time:
    - Small signal (< 1V)
      - 550 ps
    - High signal (> 1V)
      - 1.2 ns



III. ACTA chip: linearity

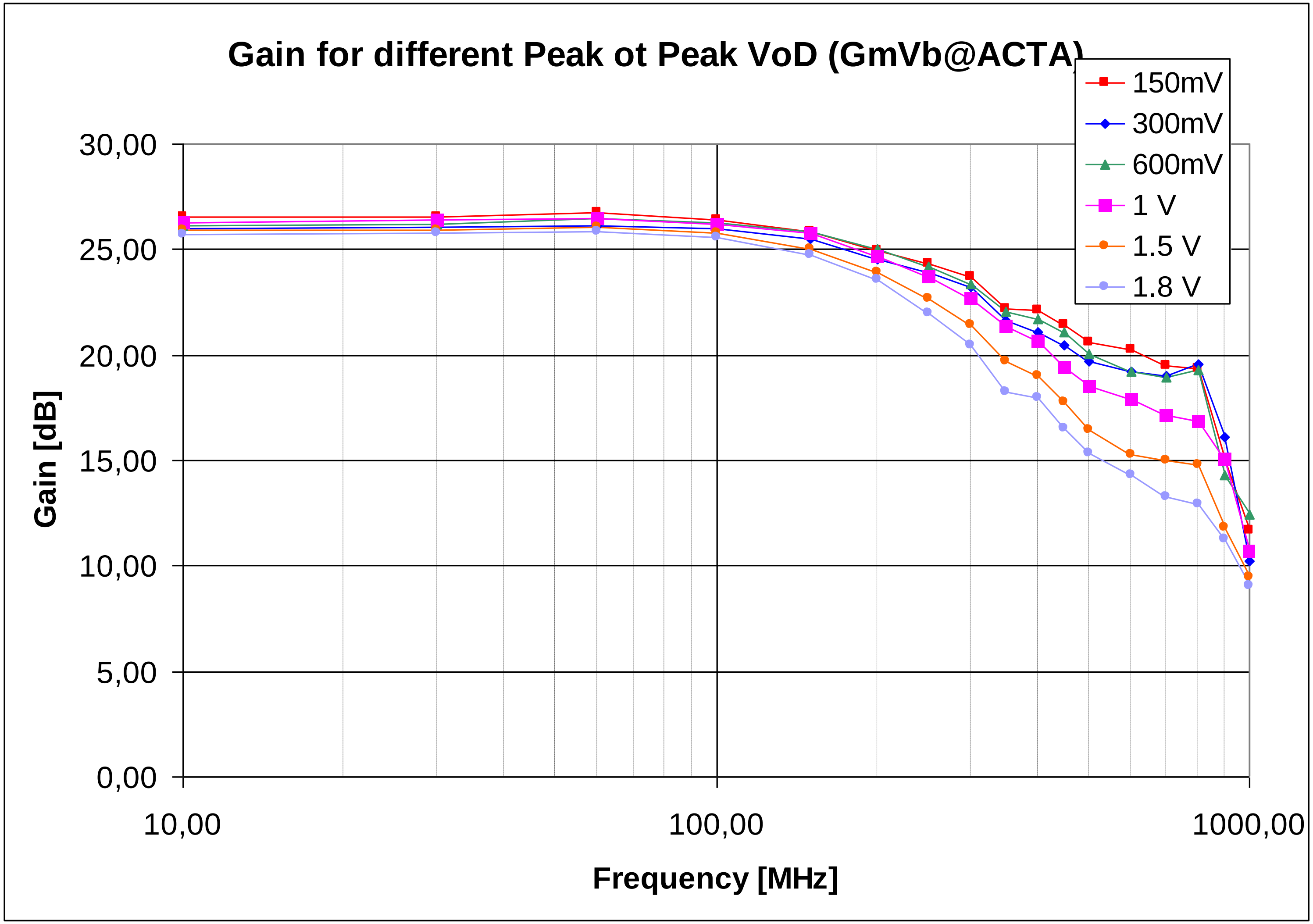
- Gain:
  - Tunnable
- Linear range
  - About 1.4 V





III. ACTA chip: frequency response

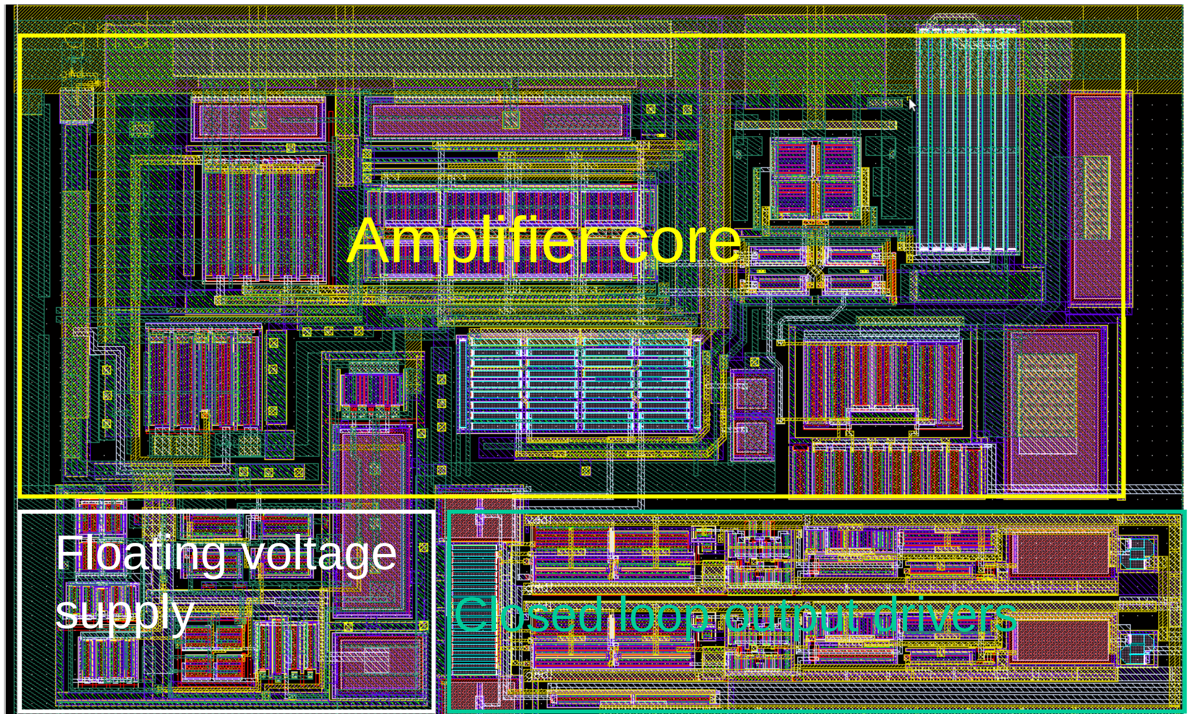
- Cut-off (3dB)
  - About 300 MHz
- Non-linearity
  - For V_{oD}>1 Vpp
- C_L aboout 5pF
  - < 1 pF when driving on-chip analogue memory input buffers



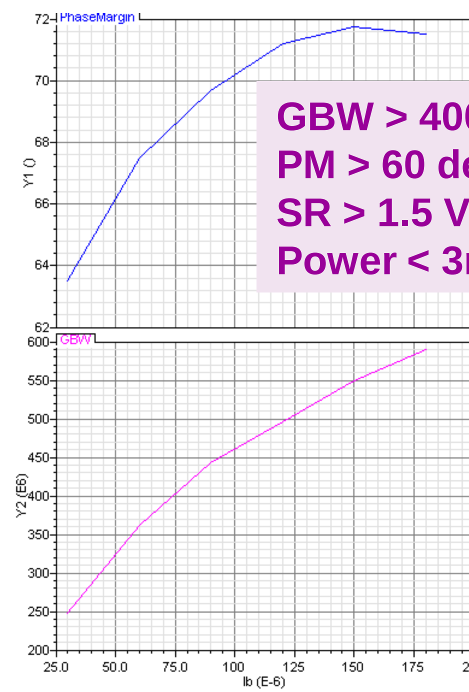
Outlook

IV. Second prototype: ACTA3

- Closed loop buffer to replace source followers
  - Better linearity & higher range
  - Lower power consumption: class AB amplifier
    - Good slew rate with low quiescent current !
  - New version of a SAM OpAmp
    - Developed in collaboration with Irfu/Saclay



- Closed loop buffer: Miller OpAmp
- Double current boost of output nMOS
  - Linear boost
  - Class B with nonlinear ctrl: off @ small signal
  - x6 boost with 750 uA (DC) total bias current
- Series resistor at the output (Rd) for C_L pole compensation
  - Limits BW



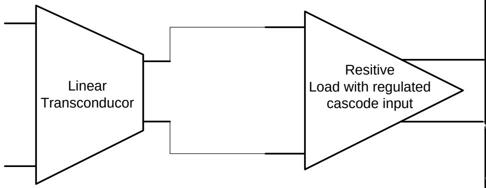
GBW > 400 MHz
PM > 60 deg
SR > 1.5 V/ns @ 5 pF
Power < 3mW

1/10 of total bias current

IV. ACTA3: 4 configurations

- Same gain block as in ACTA
- •

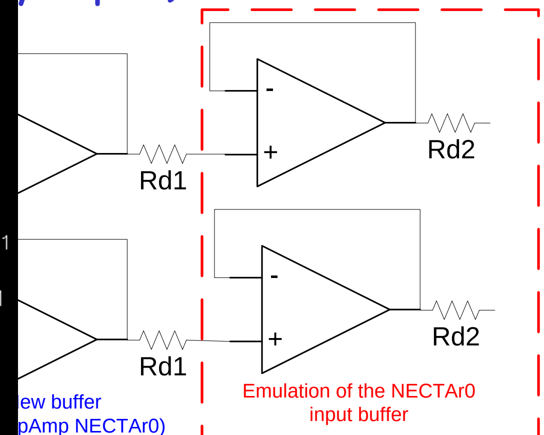
CMOS 0.35um
AMS 3 mm²
Submitted: April 2010
Received: end July 2010



Already in ACTA

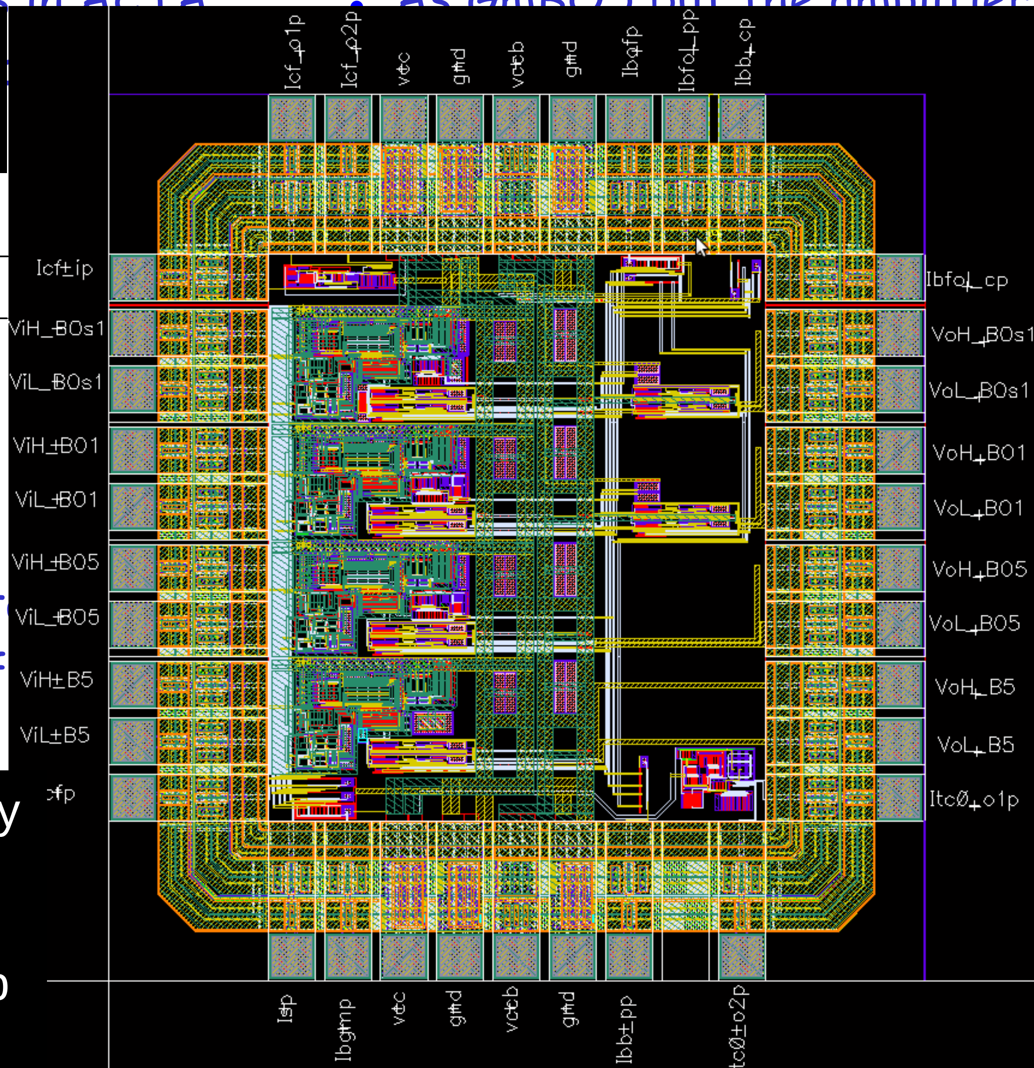
Rd for compensation
84 Ω for 4-5 pF (aprox)

- As GmBO5 but the amplifier (R_{d1}) adjusted to drive
y input)



ew buffer
pAmp NECTAr0)

Emulation of the NECTAr0 input buffer

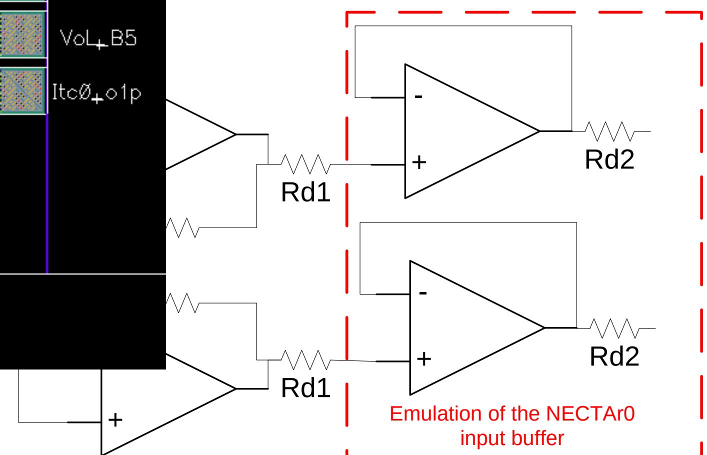


- As GmB5 but gain st
generate the DC off

replaced by diff. amp:
signals (CMRR, PSRR)

GmBO5

Produced in Irfu/Saclay engineering run with first prototype of the analogue memory chip for CTA: NETCAr0



Emulation of the NECTAr0 input buffer

Differemtial amplifier

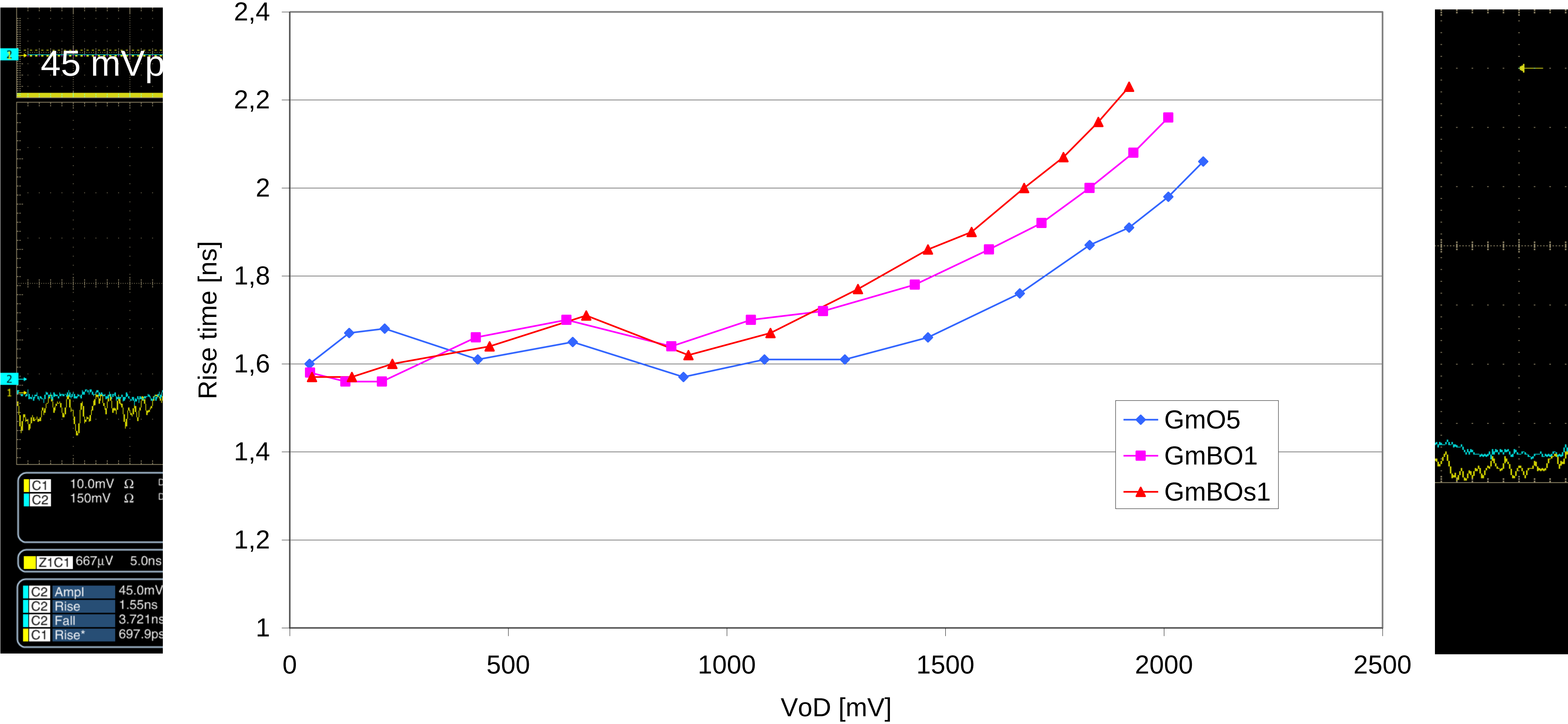
Rd for compensation
84 Ω for 4-5 pF (aprox)

New buffer
(same OpAmp NECTAr0)

Rd1 300 Ω for 1 pF (aprox)
Rd2 84 Ω for 4-5 pF (aprox)

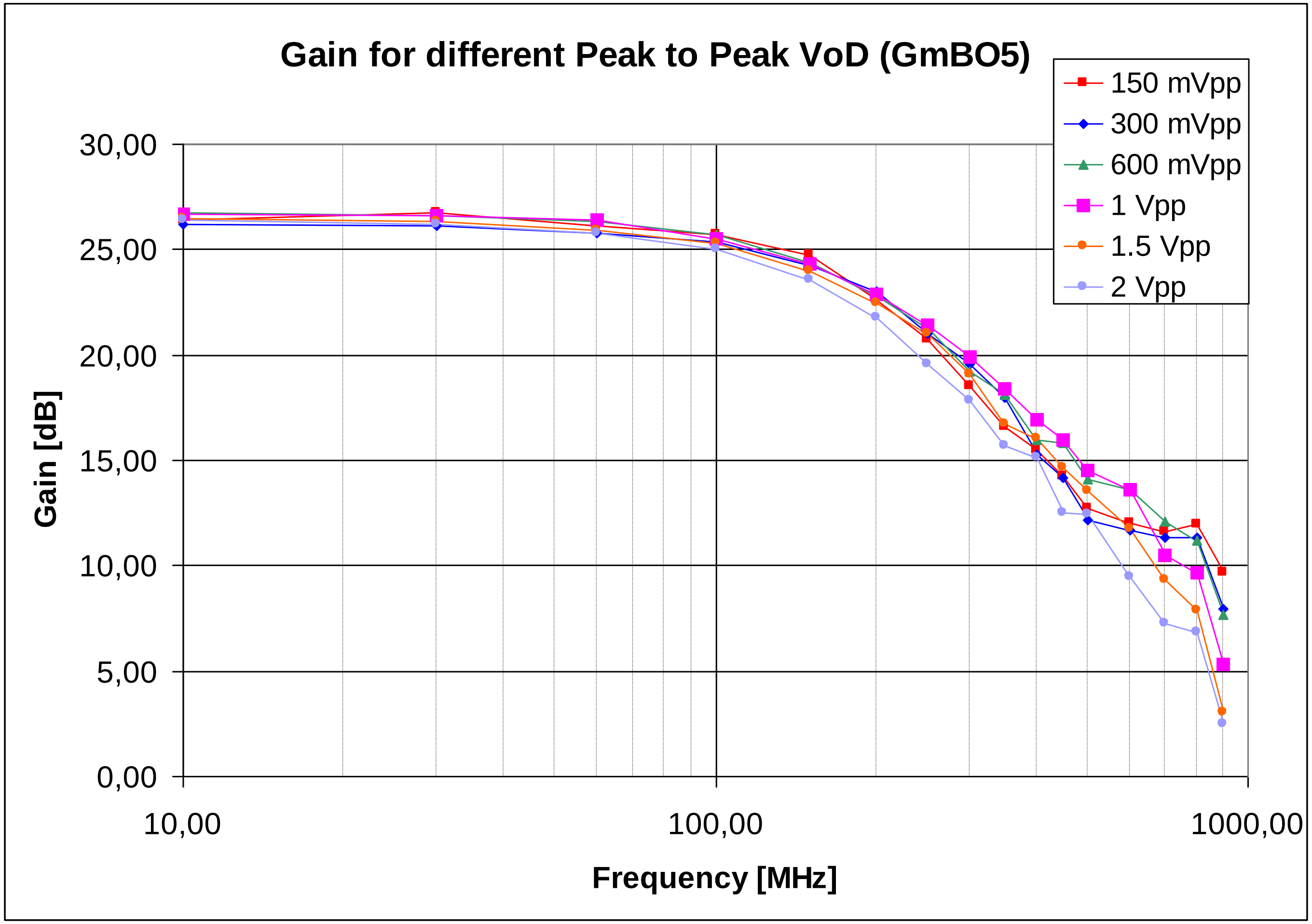
IV. ACTA3: pulse shape

- Good uniformity between small and large signal



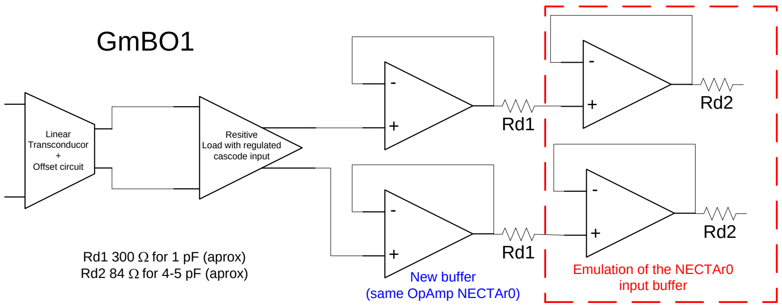
IV. ACTA3: frequency response

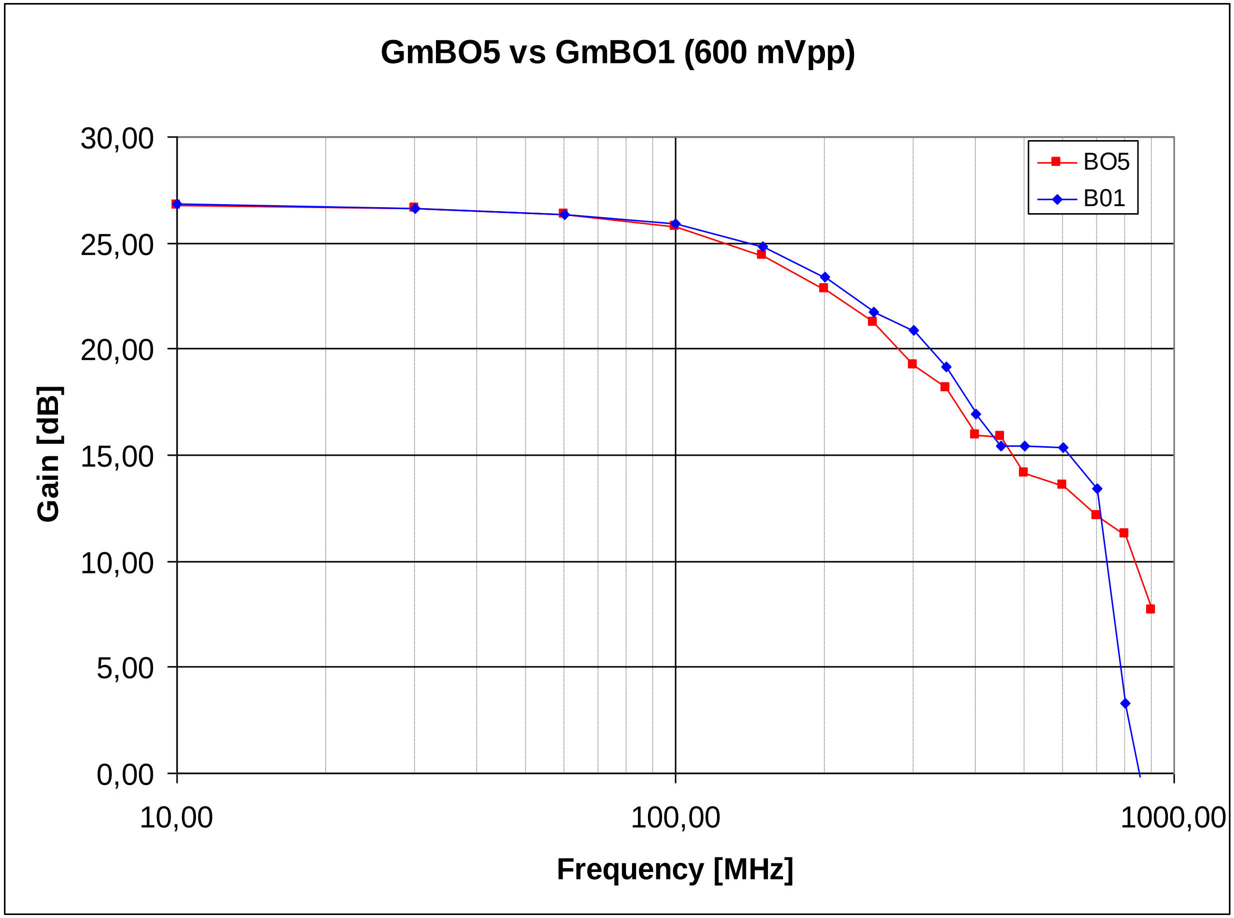
- Negligible non-linearity linearity performance for V_{oD} < 2 Vpp
- BW bit smaller than expected (300 MHz):
  - 250 MHz
  - BW given by $R_d \cdot C_L$
  - Underestimation of C_L?
  - Process variation of R_d?



IV. ACTA3: frequency response

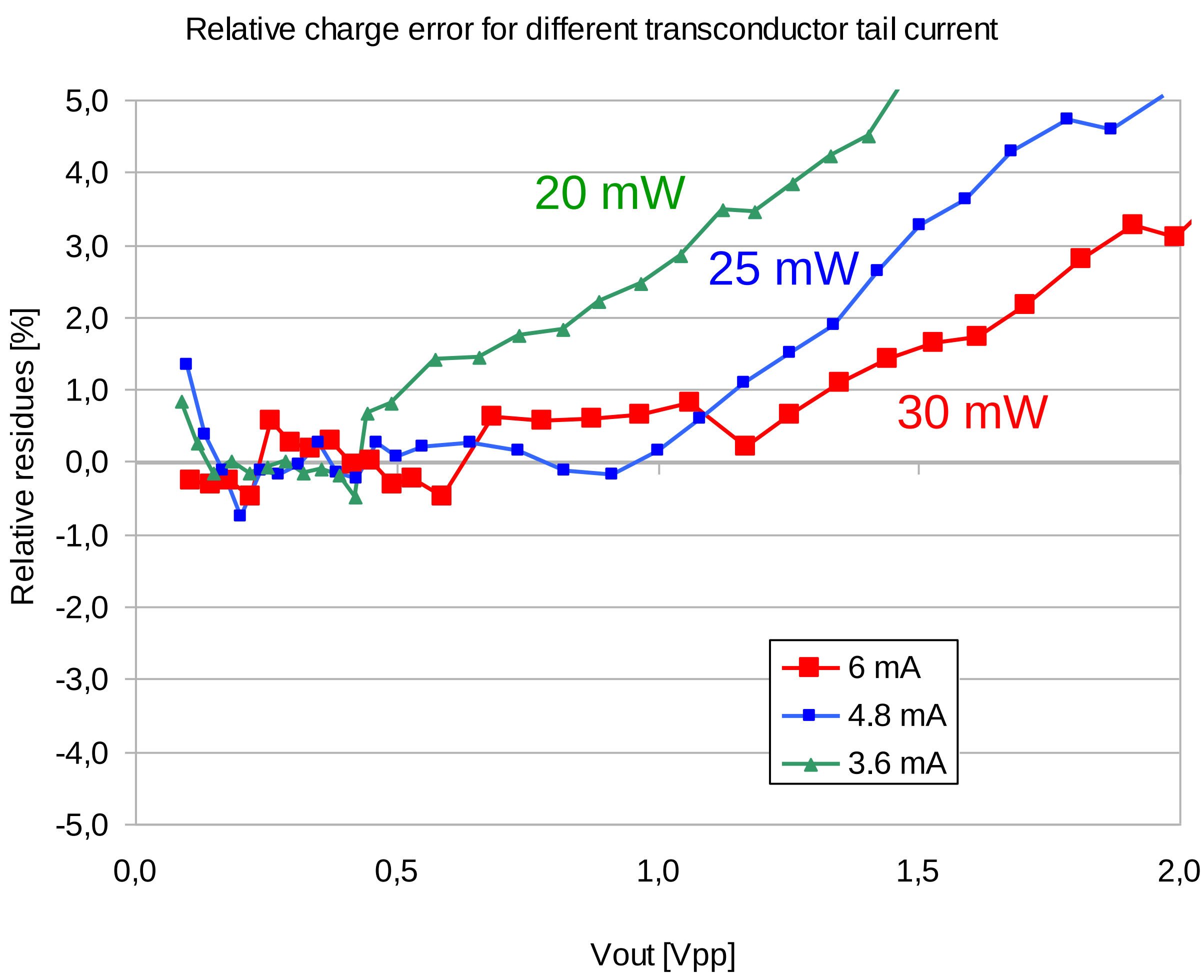
- BW of GmBO1 is even larger
  - Additional buffer !
- 300 MHz BW for ACTA3 + NECTAR0 input buffer
  - Need a very careful Rd tuning
    - BW vs stability
  - Environment more controlled
    - Same die
    - Postlayout simulation





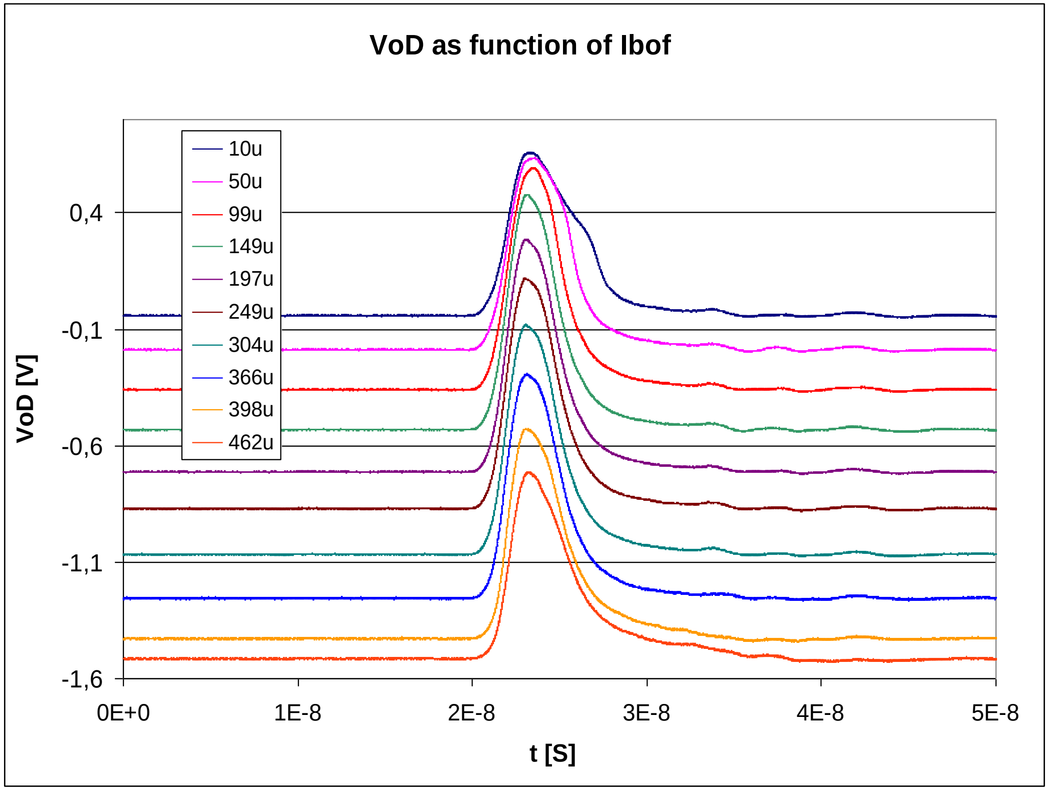
IV. ACTA3: linearity

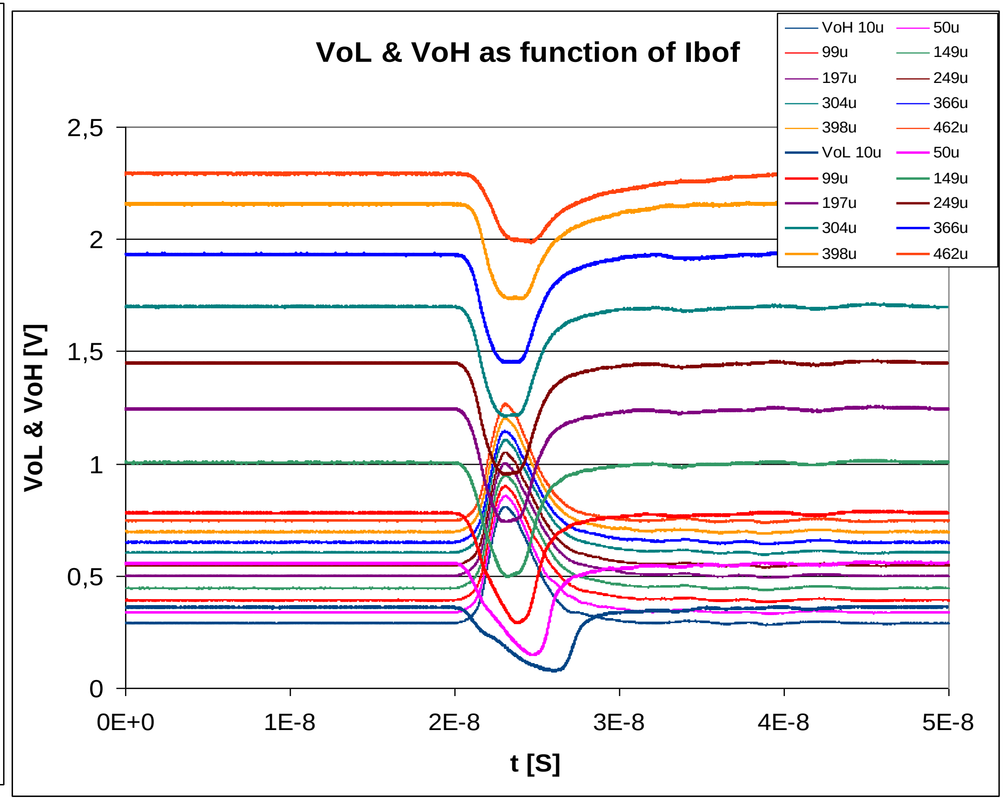
- Good linearity performance (< 1% for > 1 Vpp, < 5% up to 2 Vpp)
- Trade-off between linearity and power consumption



IV. ACTA3: Offset generation: GmBO5

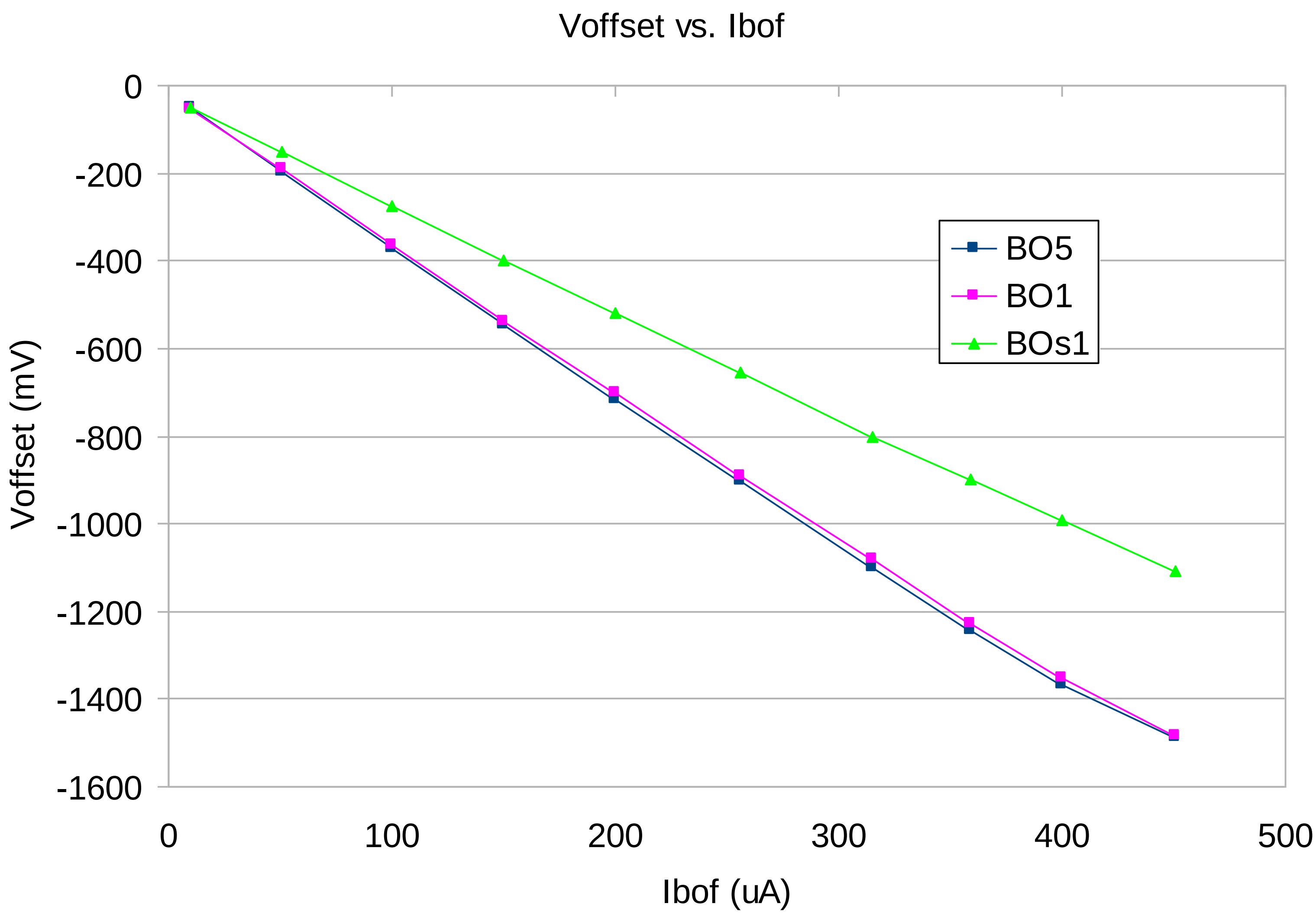
- DC offset is controlled by the current “Ibof”





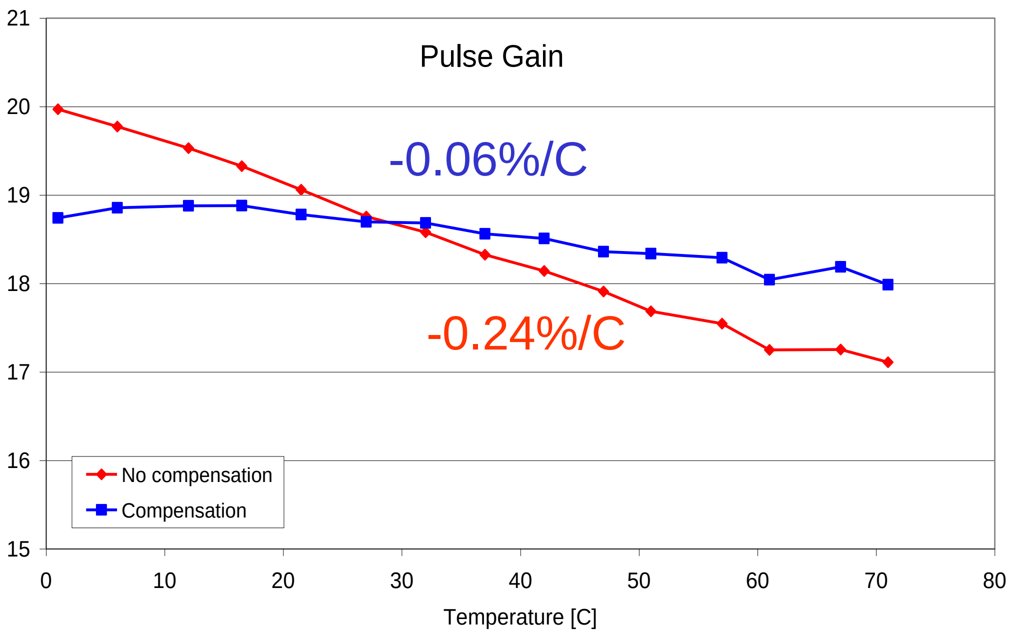
IV. ACTA3: Offset generation: transfer function

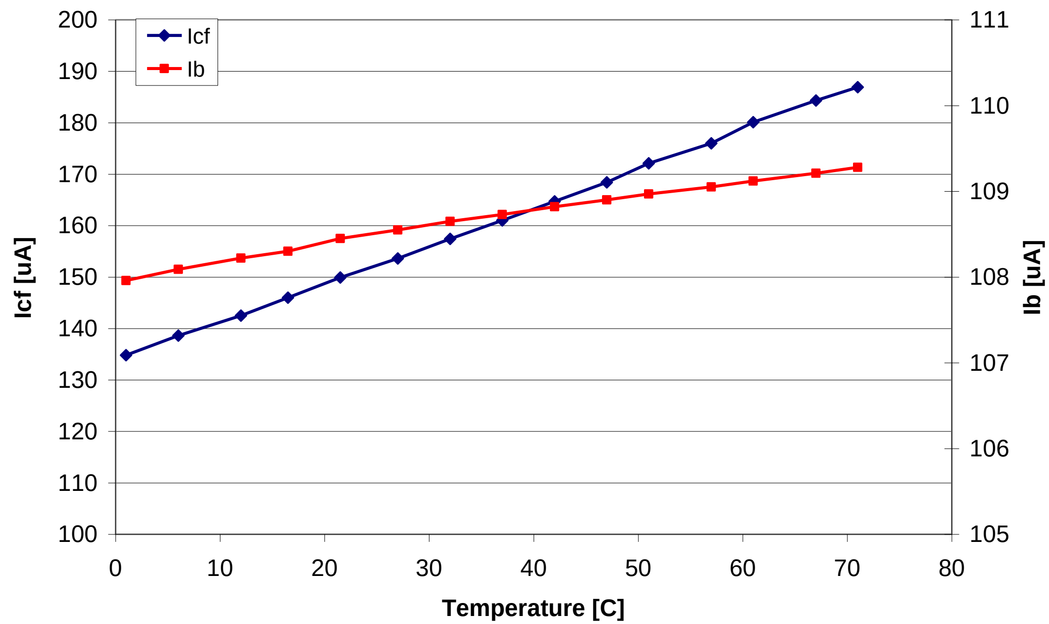
- Similar behaviour for GmBO1 and GmBOs1



IV. ACTA3: temperature compensation

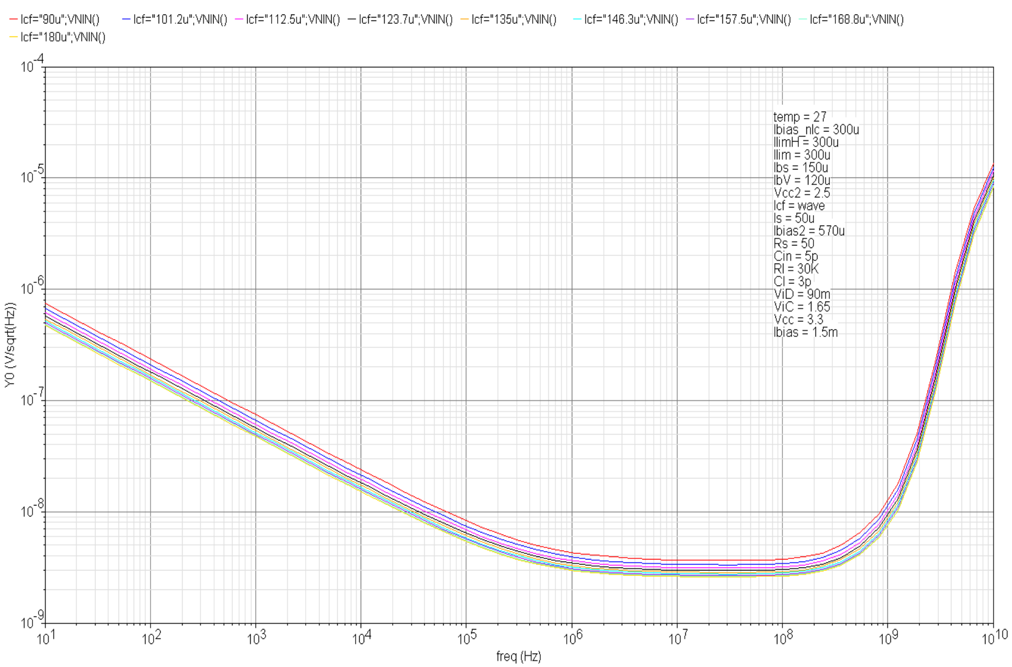
- Controlling temperature dependence of the gain
  - Transconductor TC is about -0.2%/C
  - Compensated by adjusting the TC of the current (Icf) controlling floating voltage source
  - Final TC ≈ -0.05 %/C (1% for 20 C variation in one night)
- Band gap current reference (Ib) with TC ≈ + 180 ppm/C

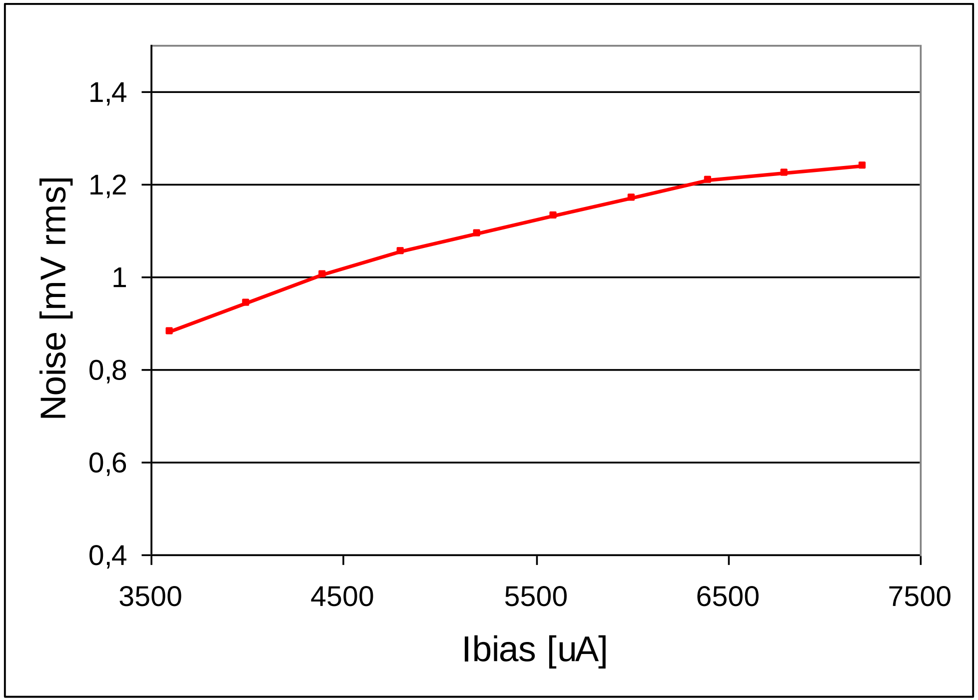




IV. ACTA3: noise

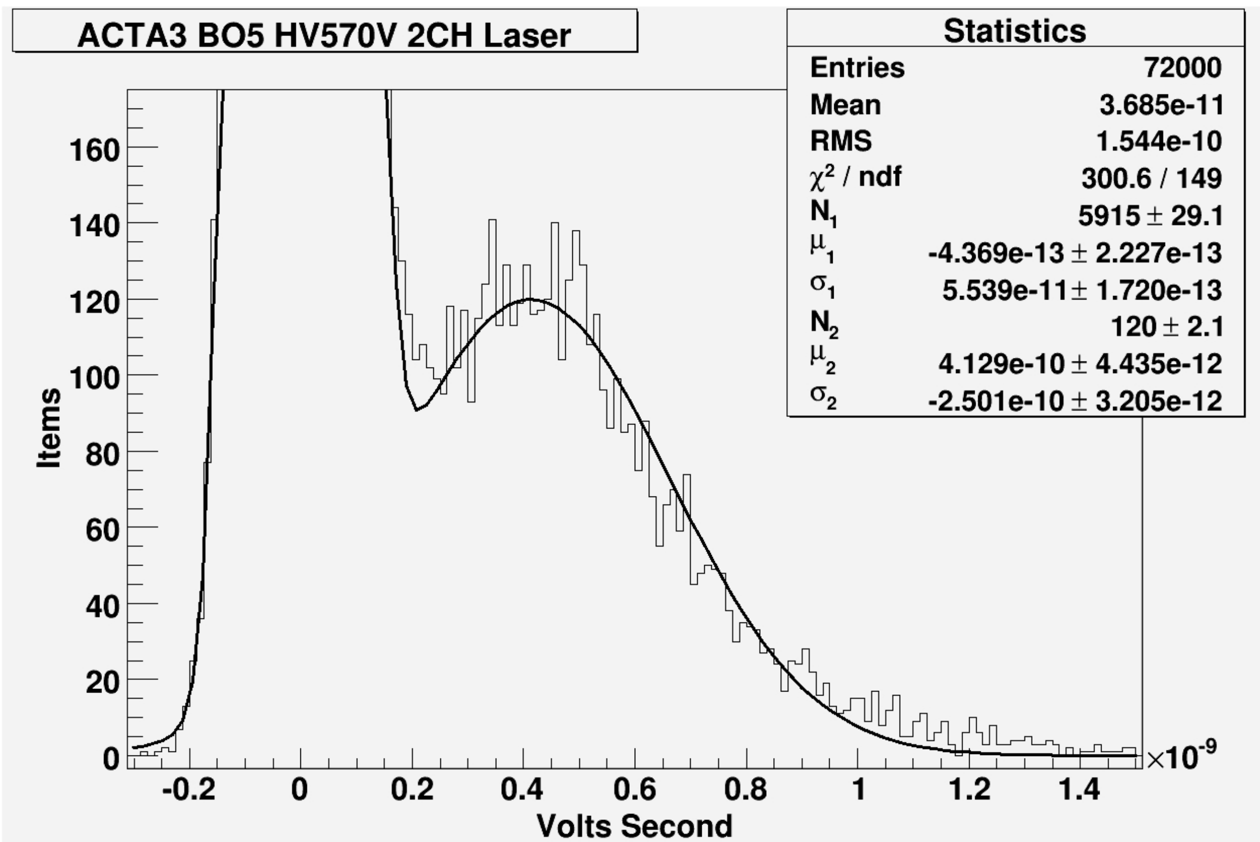
- Channel thermal noise of the input differential pair dominates
  - Wideband amplifier: 1/f noise not relevant: use NMOS
  - Cross-coupling degrades noise performance: g_m subtraction
- For input referred series noise < 3 nV/√Hz
  - Gm > 5 mS : large K (W) and/or bias offset Vb
  - Tradeoff between noise and large signal handling
- Noise increases with differential pair bias current

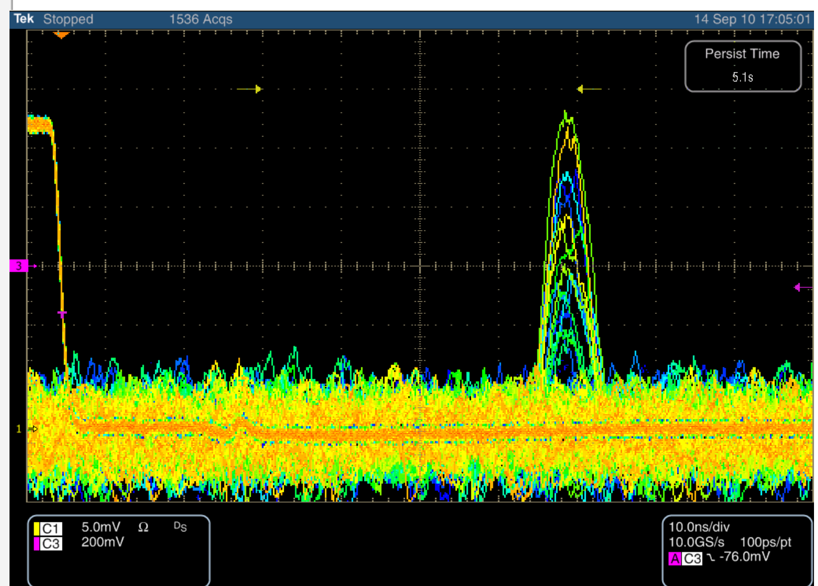




IV. ACTA3: single photoelectron response

- Single photoelectron response at PM nominal gain ($2 \cdot 10^5$)
  - With R5900 PM, not optimal for SPE resolution
  - To be done with PM developed for CTA





Outlook

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V. Summary

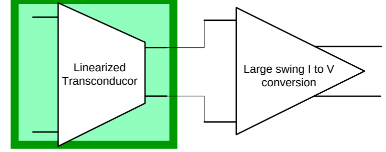
- Alternative solution for wideband pulse amplifiers
  - Gain: 20
  - Bandwidth
    - > 400 MHz for C_L < 1 pF
    - > 300 MHz for C_L < 5 pF

GBW > 6 GHz in 0.35 um CMOS technology

  - Linearity < 1% for 1Vpp and < 3% for 2 Vpp
    - For fast "closed loop" amplifiers, linearity is usually limited by slew rate
- Intrinsic BW of the core amplifier (without buffer) > 600 MHz
  - BW > 1 GHz in 130 nm technology ?
- Tuneable:
  - Gain
  - DC offset : ADC interface
  - Linearity vs power conssumption

Thank you !

II. The circuit: HF transconductors

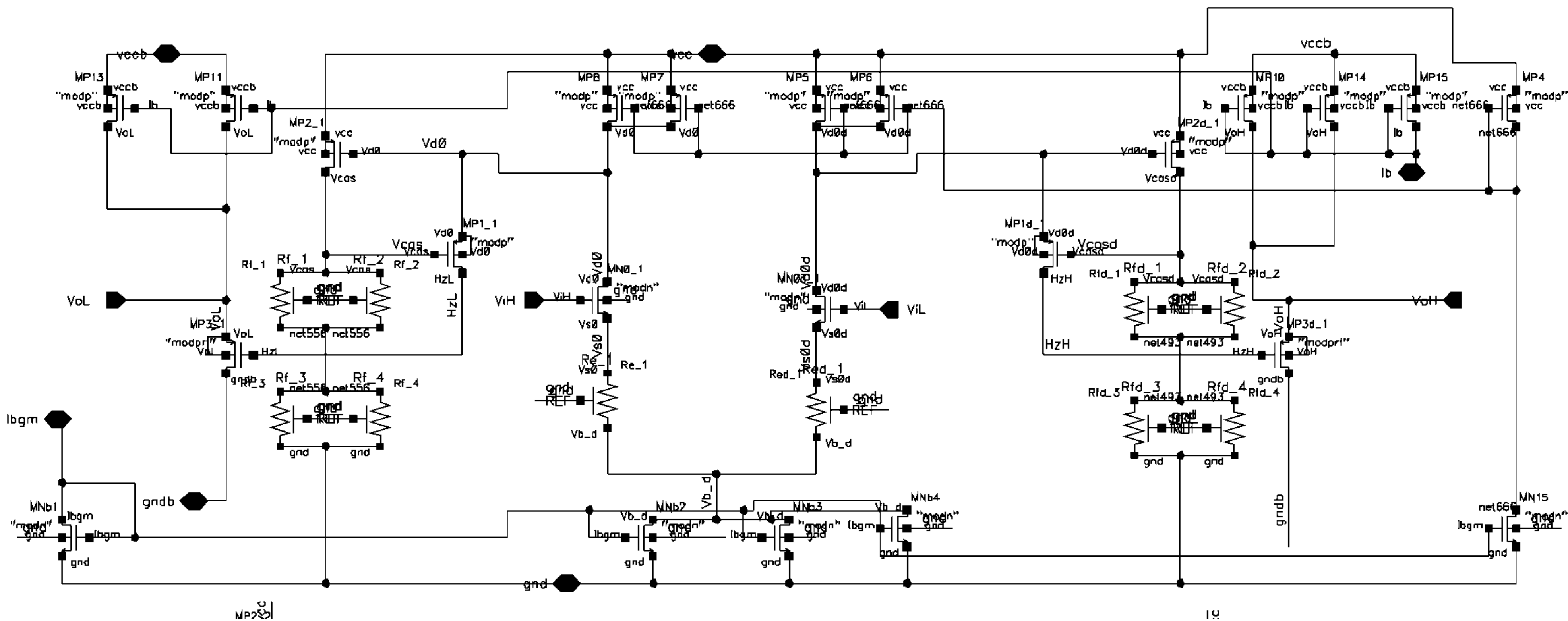


- HF transconductors with linearisation by local feedback

	Lin. Err. [%]	BW [MHz]	Noise [nV /√Hz]	Bias current [mA]	Comments
Simple dif. Pair	2	1000	2.2	4.5	W/L limited by linearity
Dif. Pair with degeneration	1	1000	2.7	4.5	Limited range
Cross coupled (XC) mismatched	3	2000	5.7	4.5	Low Gm/Ibias
XC with offset Wang-Guggenbuhl	0.5	850	3.2	8	High consumption
XC with bias offset Szczepanski	0.5	1000	2.5	4.5	Accurate control of Gm with bias offset voltage
Adaptative Nedungadi-Viswanathan	Small range	1000	2.5	7.5	Small linear range even for high bias current

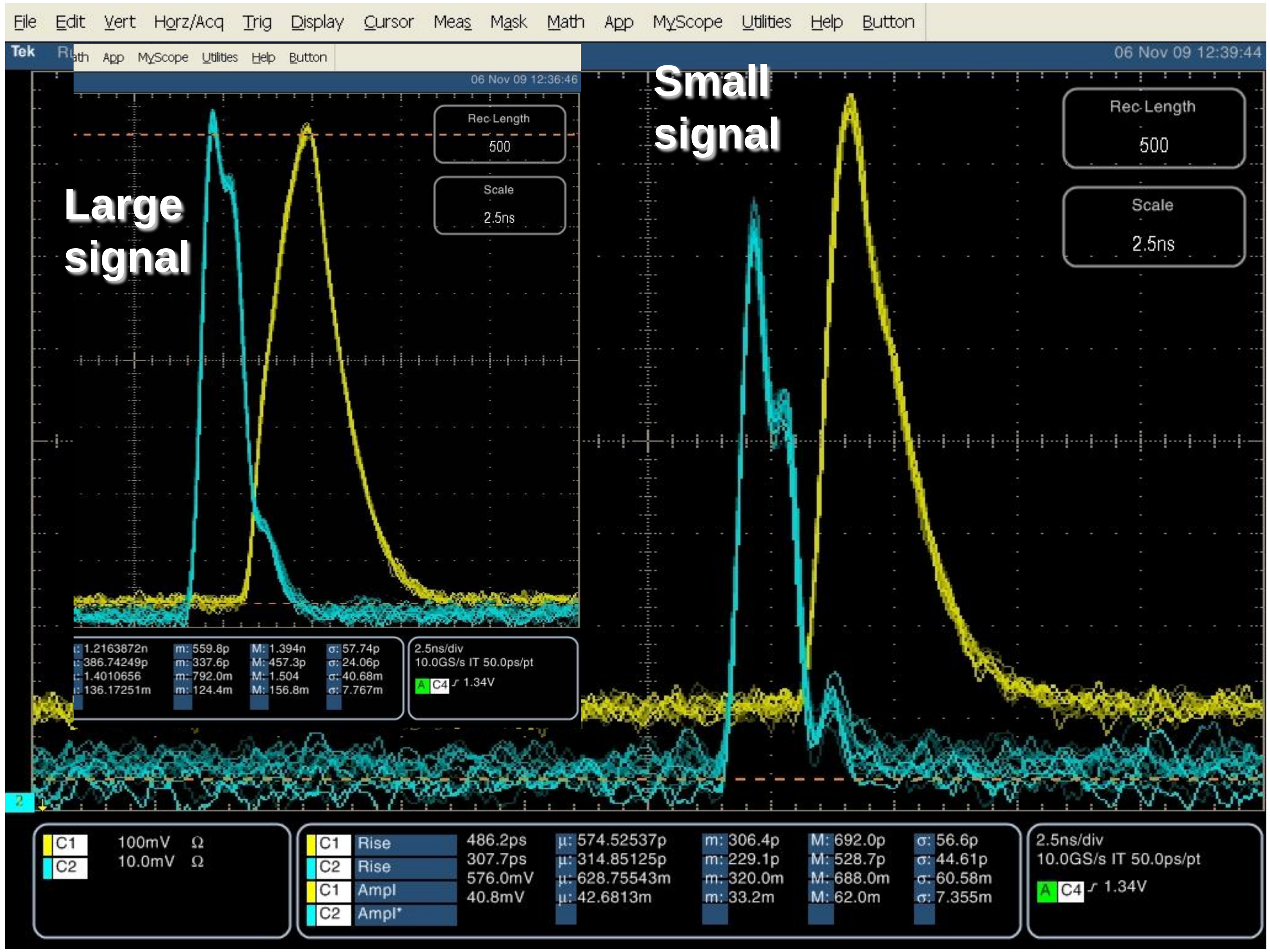
Linear amplifier: diff. pair with degeneration

- Three stages:
  - HF transconductor: source degenerated MOS diff. pair: V to I
  - Cascoded common gate amplifier: I to V
  - Source follower: low impedance driver (up to 3pF cap. load)
- Post-layout simulation: 5 GHz GBW and 3% lin error (VoD 1.7 V)



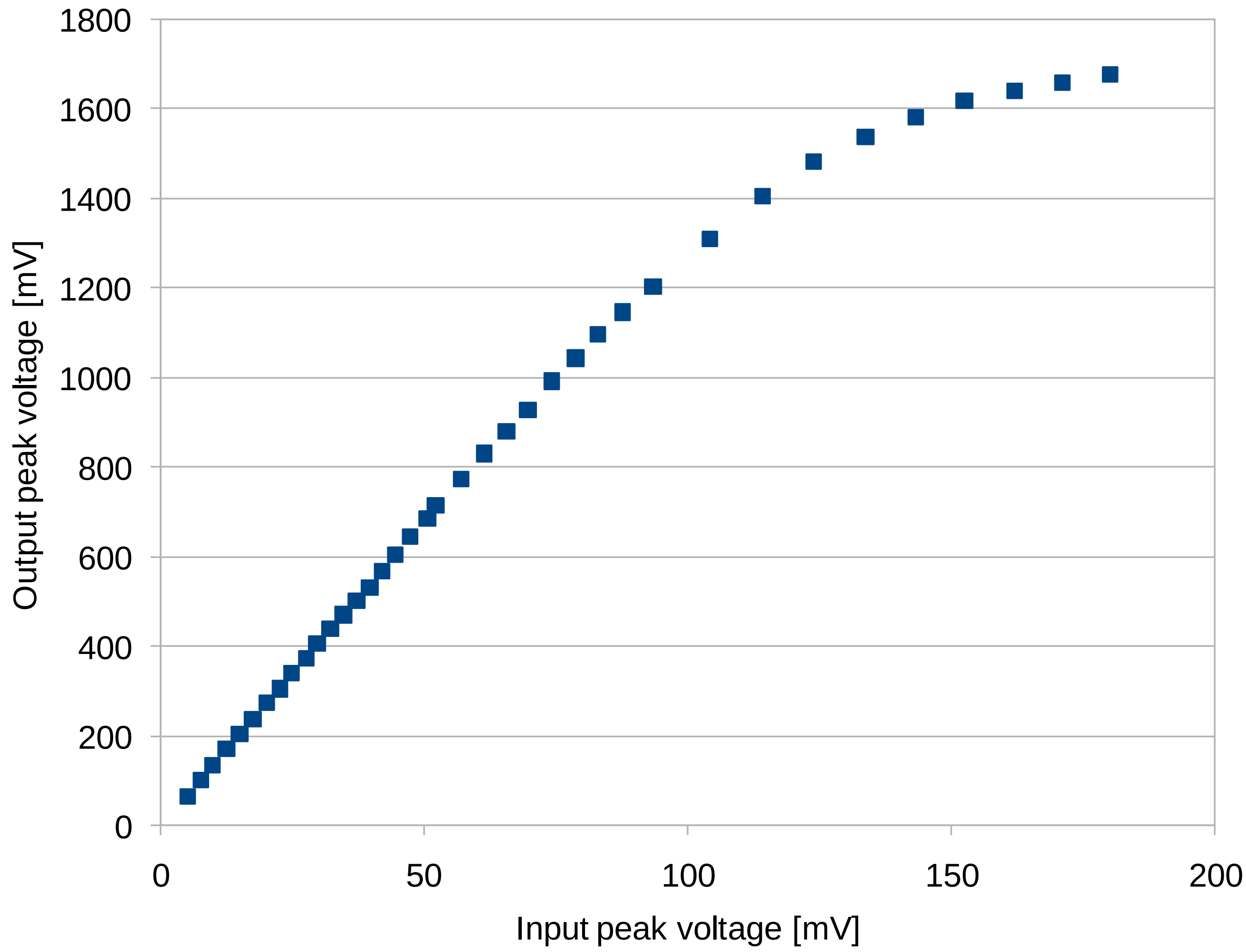
Results: linear amplifier: degenerated transconductor

- Working
  - Blue: input
  - Yellow: output
  - No ringing
- Fast input pulse
  - Rise: 300 ps
- Output pulse
  - Rise time:
    - Small signal (< 1V)
      - 574 ps
    - High signal (> 1V)
      - 1.2 ns



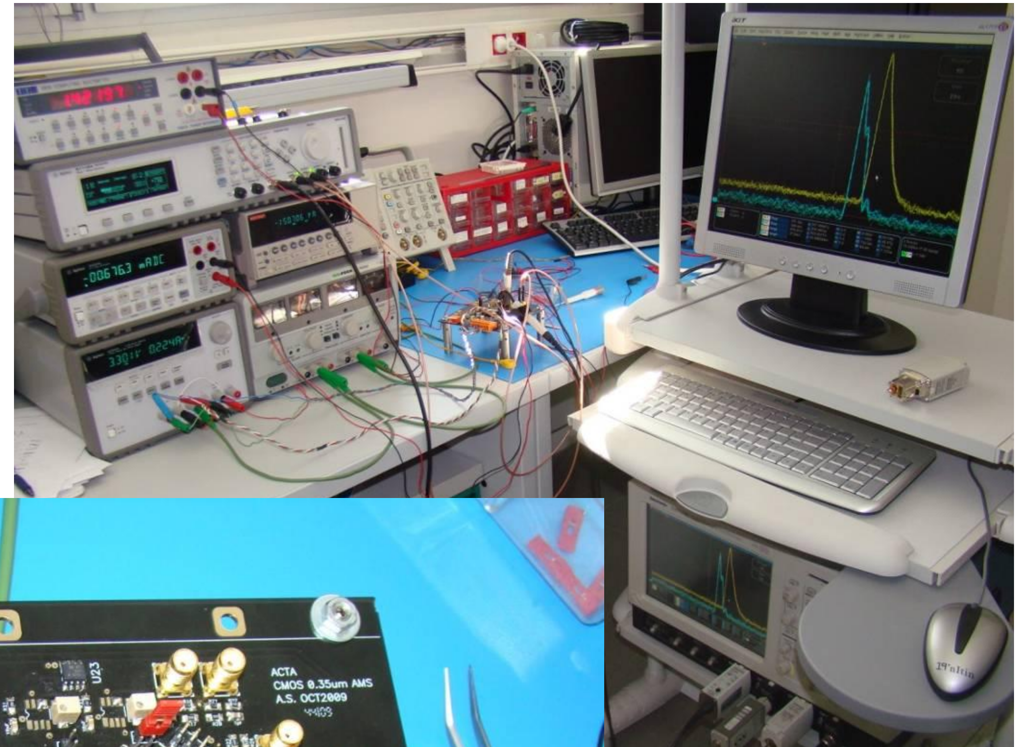
Preliminary results: linear amplifier: degenerated transconductor

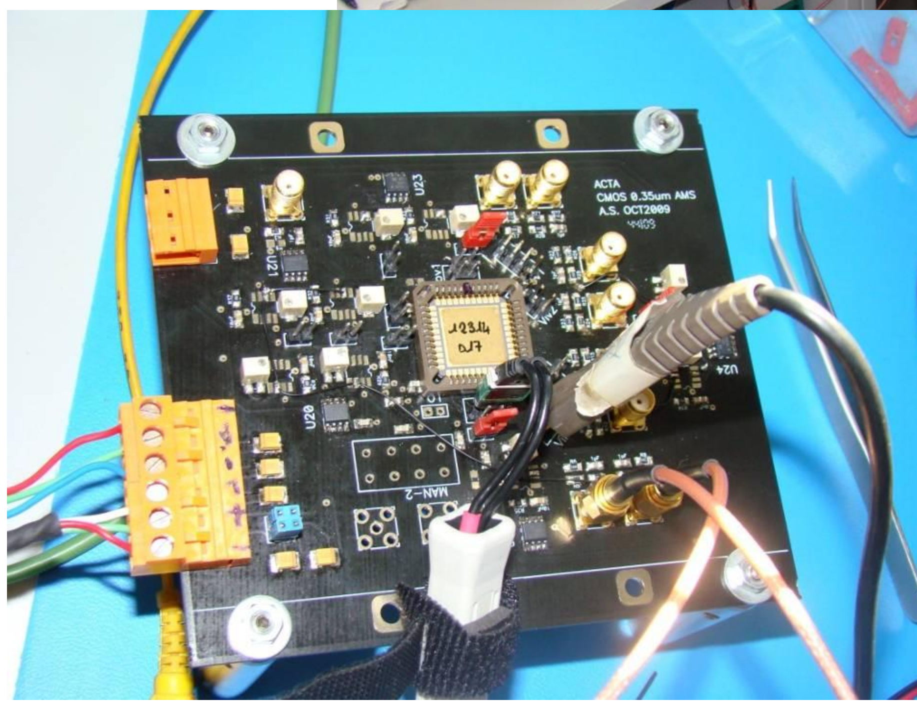
- Gain
  - About 13,5
  - Slightly tunnable
- Linear range
  - About 1.5 V



III. First prototype: test set-up

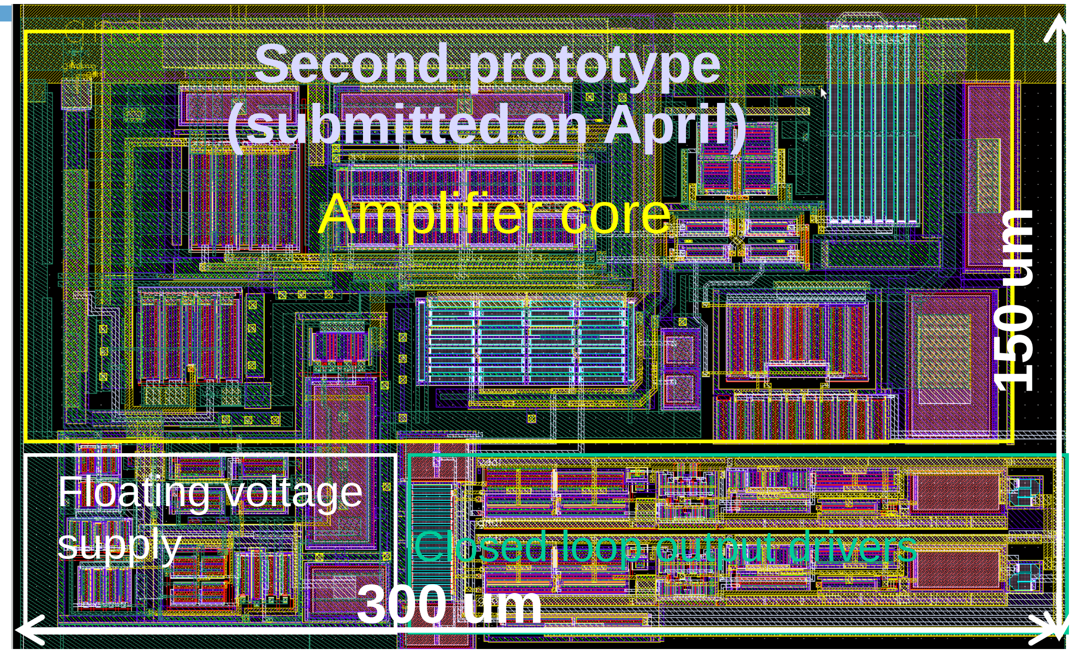
- Two test cards
  - General charact
    - Fast pulse generation
    - Bias current though stable ref
  - S-parameter
    - Minimal components
- Acquisition
  - Scope:
    - 1.7 GHz
    - 20 GS/s
  - Probe: diff. 4 GHz
- Test just started
  - < 1 week



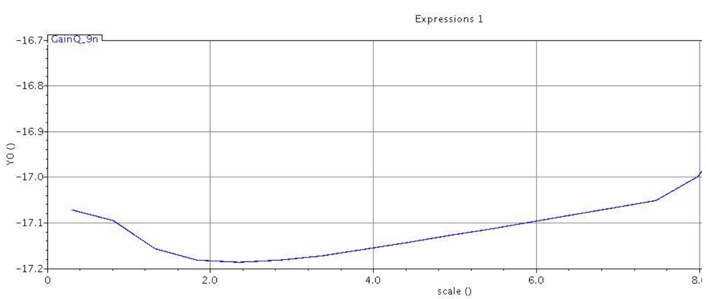


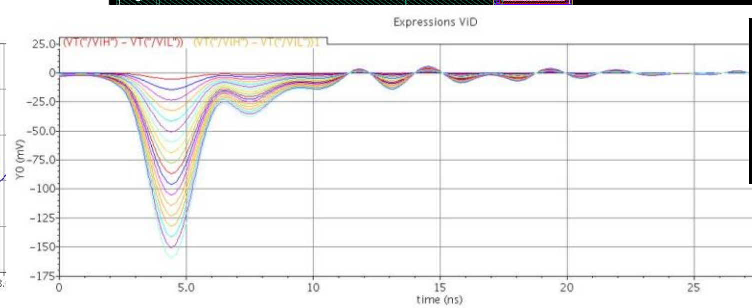
I. Introduction: ACTA3

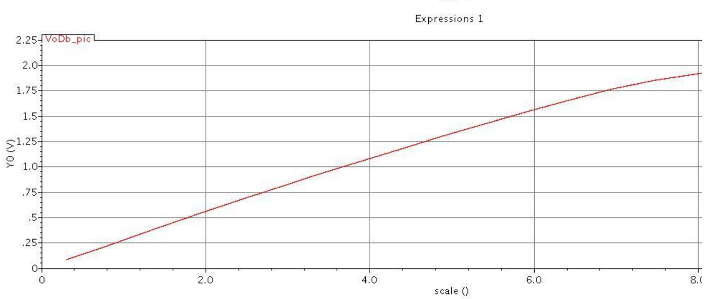
- Second prototype (ACTA3)
  - Better linearity
  - Low power output driver:
    - Class AB amplifier
      - New version of a SAM OpAmp
      - Collaboration with Eric
  - Temperature compensation
  - Control of DC offset as needed for ADC

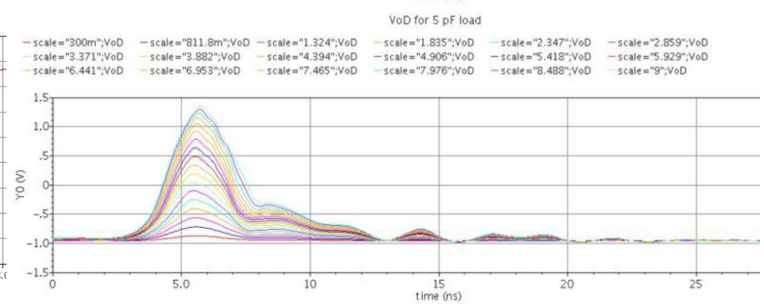


CMOS 0.35um
AMS 3 mm²
Submitted: April 2010
Received: end July 2010



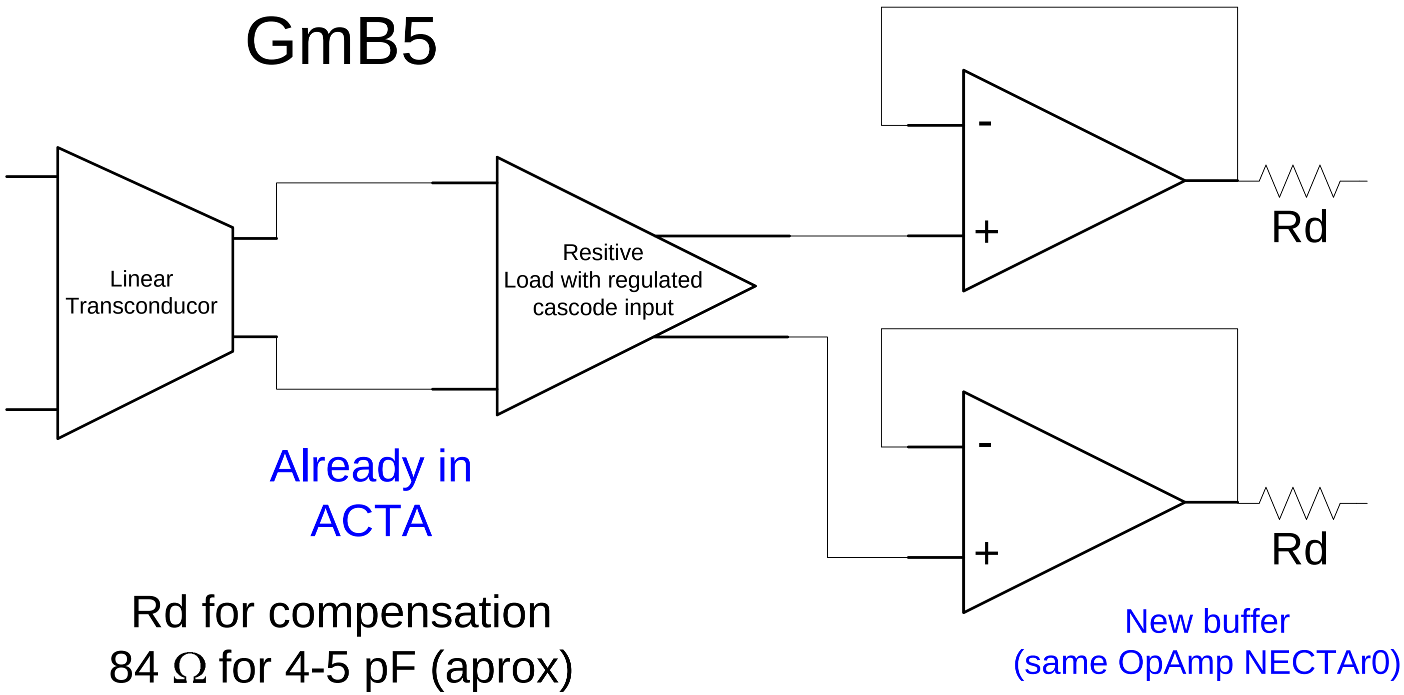






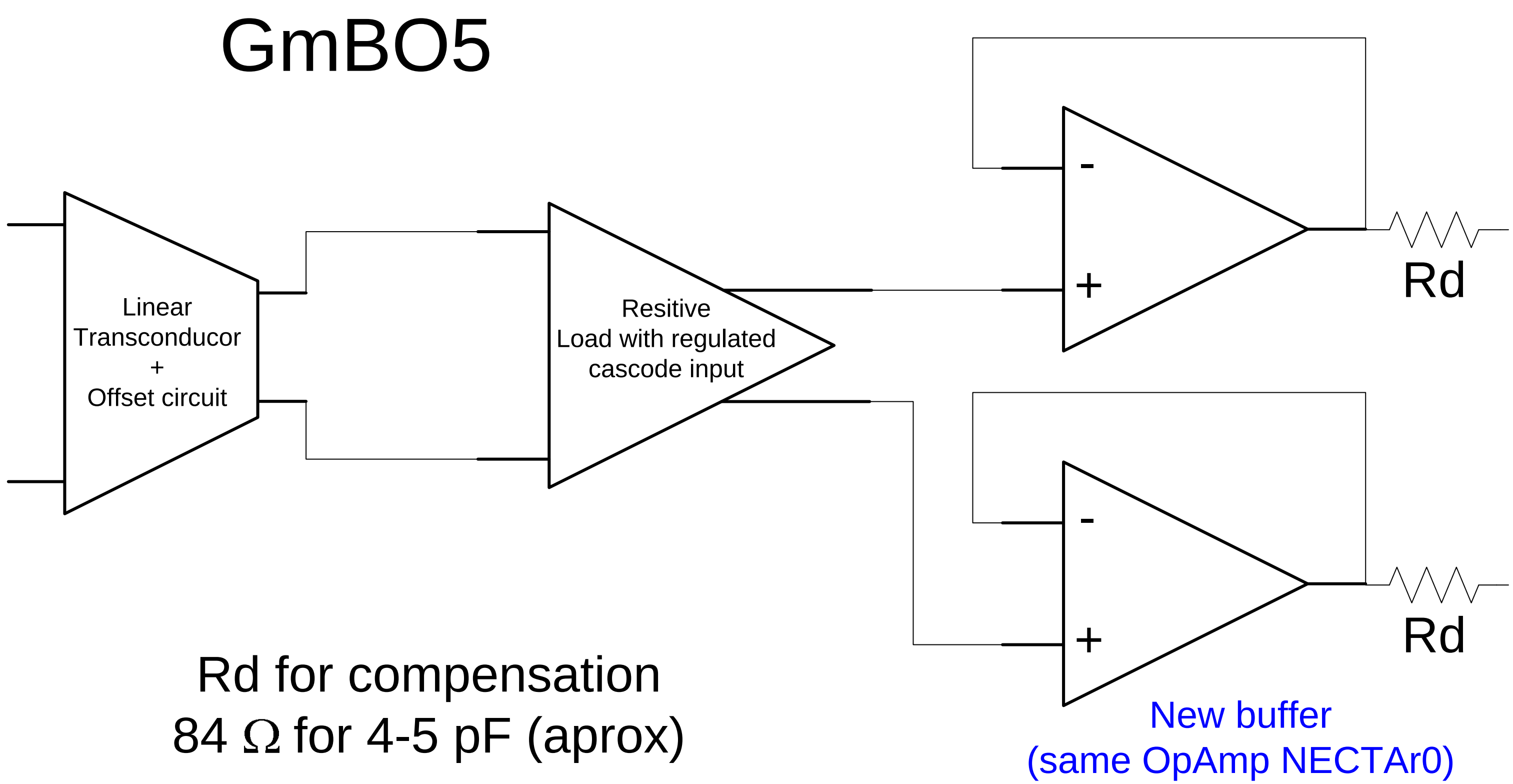
II. Blocks in ACTA3: GmB5

- Same gain block as in ACTA
- New buffer
  - Based on the same OpAmp used for NECTAR0 input buffers
    - Colaboration with Saclay
- Compensation resistor sized to drive outptut pads (4-5 pF load)
- Not tested for the moment, only to "debug"



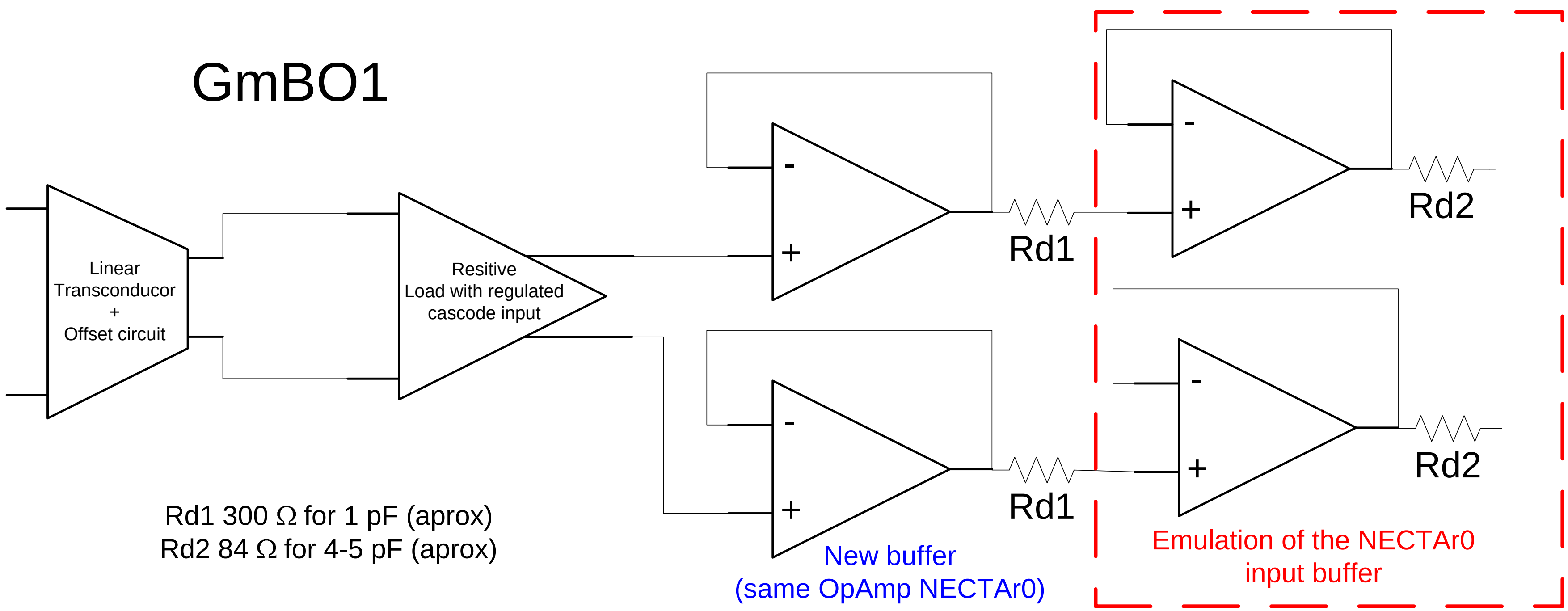
II. Blocks in ACTA3: GmBO5

- As GmB5 but gain stage is modified to generate the DC offset required by ADC
- Compensation resistor sized to drive outptut pads (4-5 pF load)



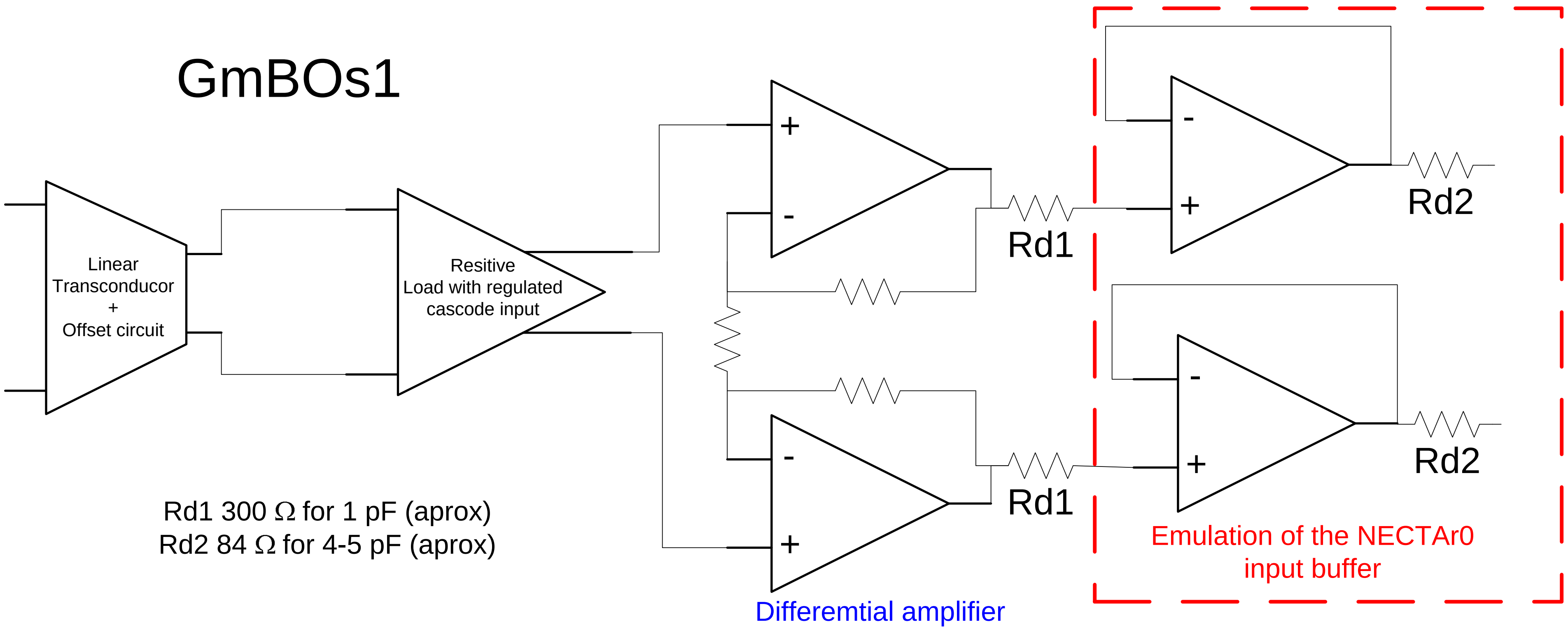
II. Blocks in ACTA3: GmBO1

- As GmBO5 but the amplifier (Rd1) is adjusted to drive a smaller capacitance:
  - It should be the case if it is integrated in the analogue memory chip
  - An additional buffer is added to emulate the NECTAr0 input stage and test the chain



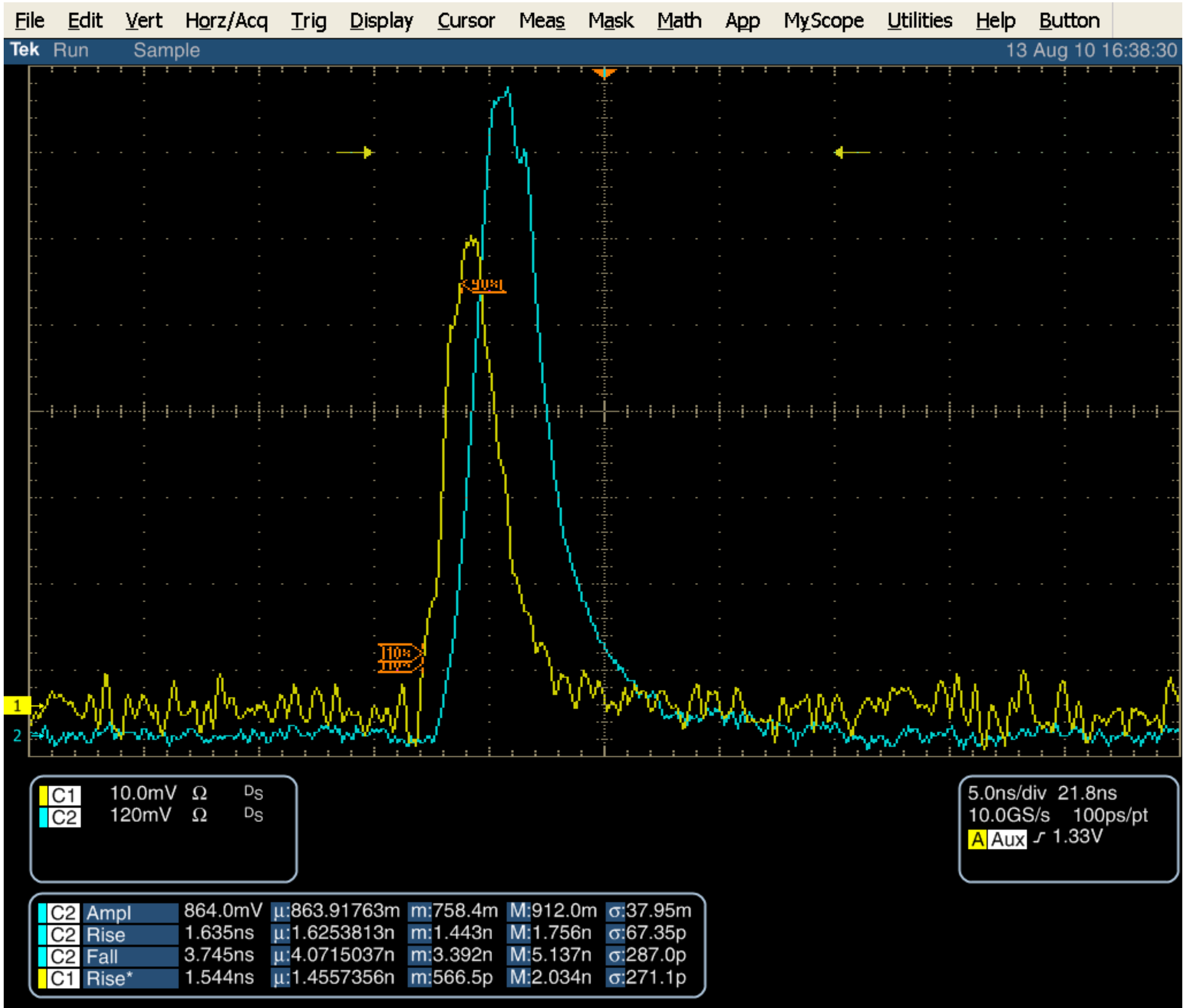
II. Blocks in ACTA3: GmBOs1

- As GmBO1 but the buffer is replaced by a fully differential amplifier:
  - Subtract common mode signals as soon as possible (CMRR, PSRR)



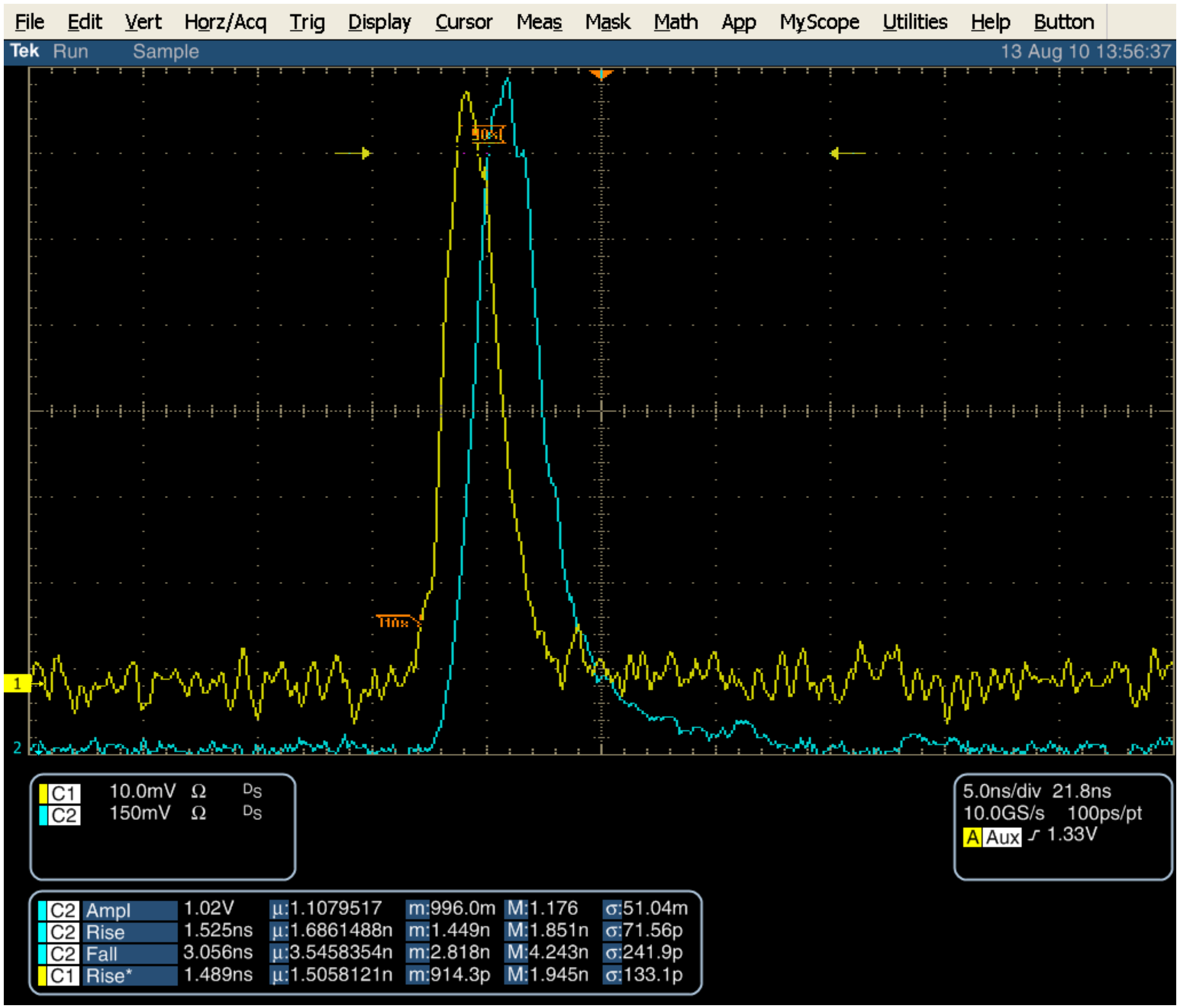
III. Pulse shape: GmBO1

- Second order response effects in the shape? (small…)

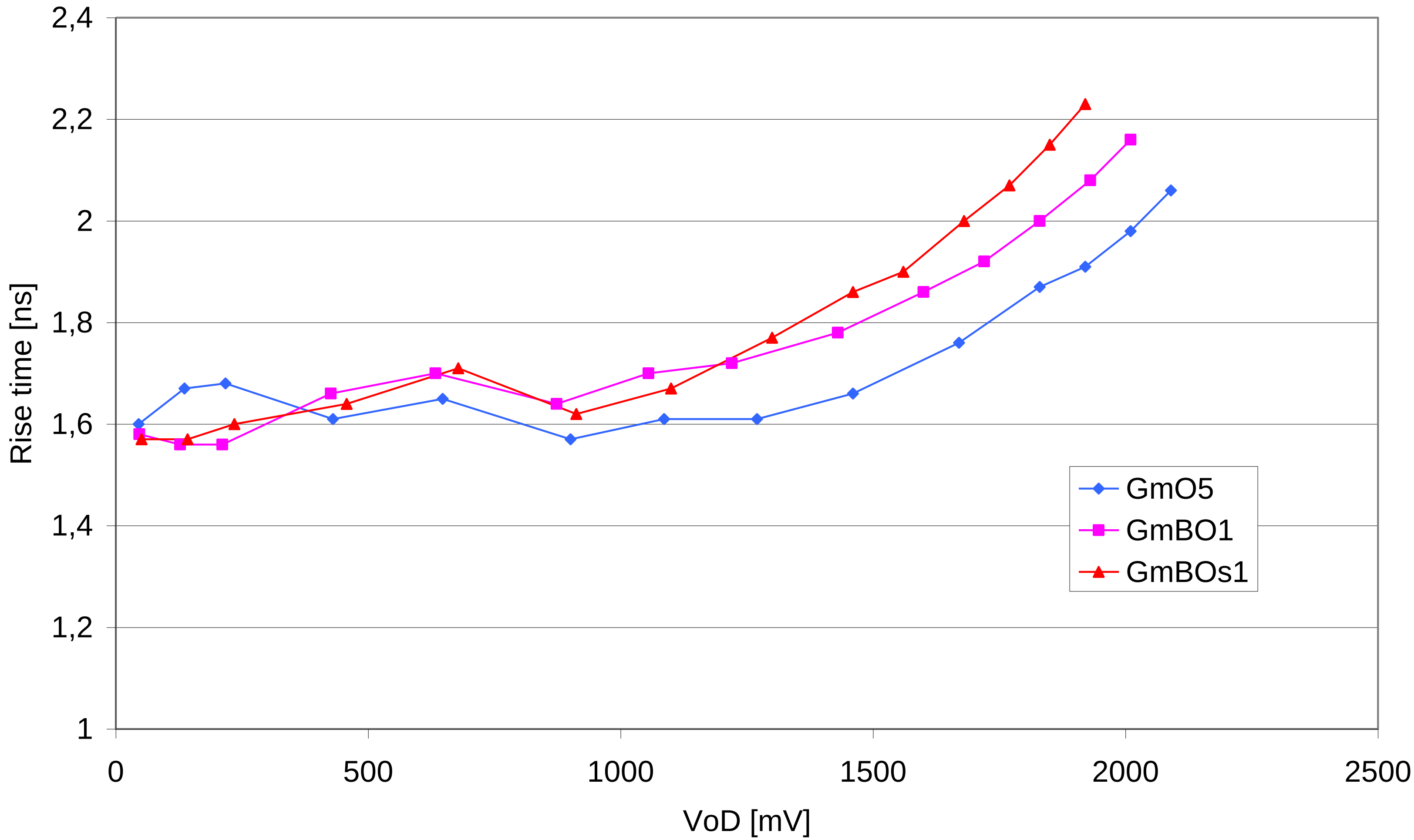


III. Pulse shape: GmBOs1

- Second order response effects in the shape? (small...)

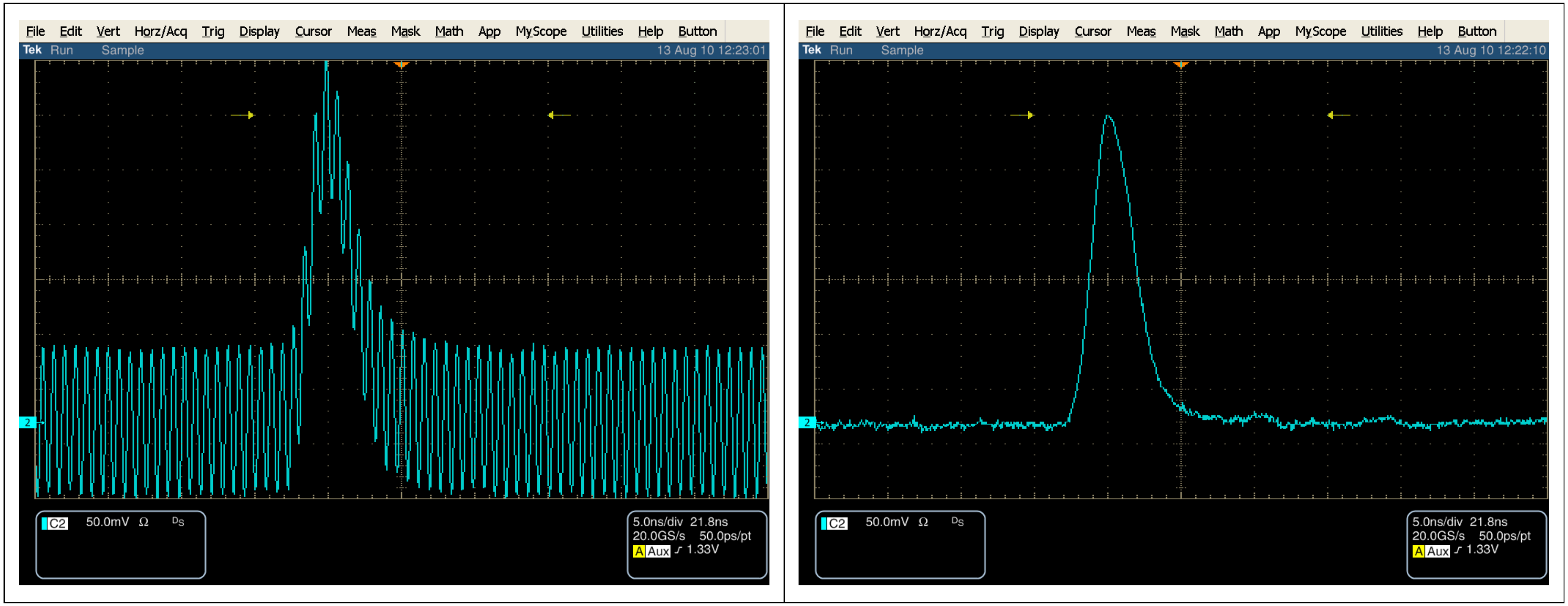


III. Pulse shape: rise time vs amplitude



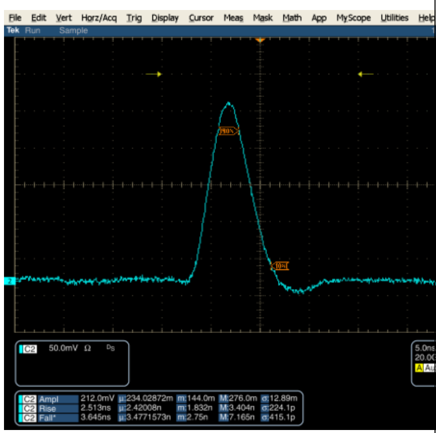
IV. Behaviour of the new buffer: class B boost control

- A current control Ibfol has to be set to > 30 uA to be sure that the class B current boost is off at the quiescent state

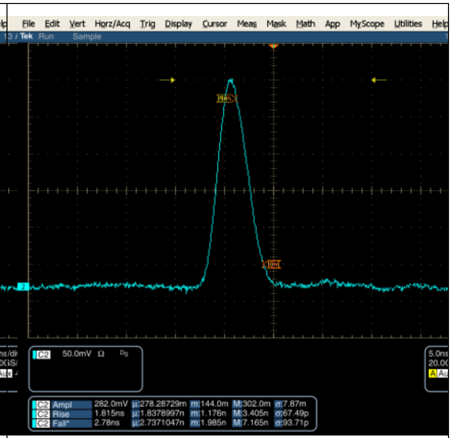


IV. Behaviour of the new buffer: bias current (buffer driving 5 pF)

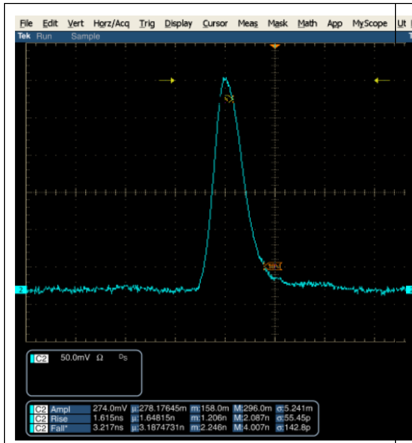
- Bias current (4*Ibbpp):
  - If too low (< 75uA for 5pF, <45uA for 1 pF) GBW is too low
  - If too high (>200uA) phase margin too low



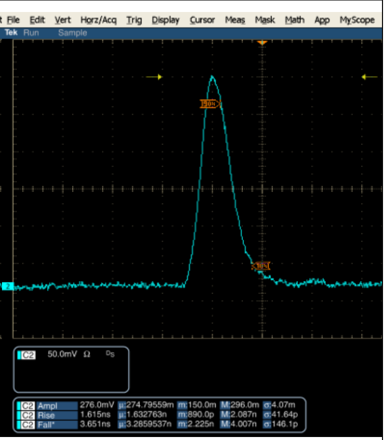
Ibb=10uA



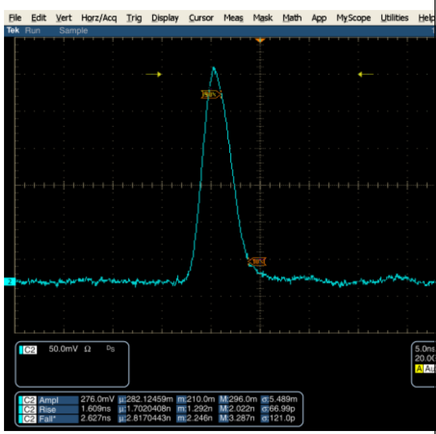
Ibb=33 uA



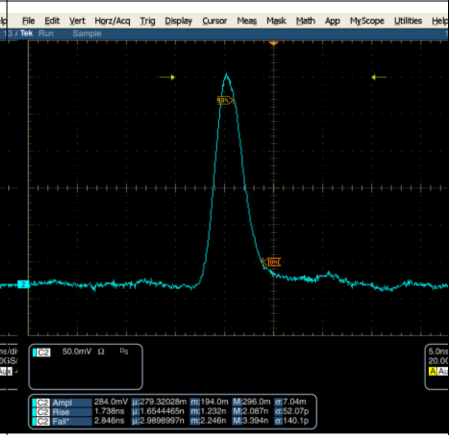
Ibb=152uA



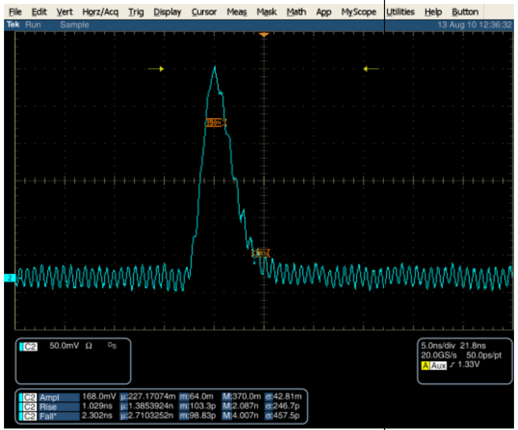
Ibb=195uA



Ibb=66uA



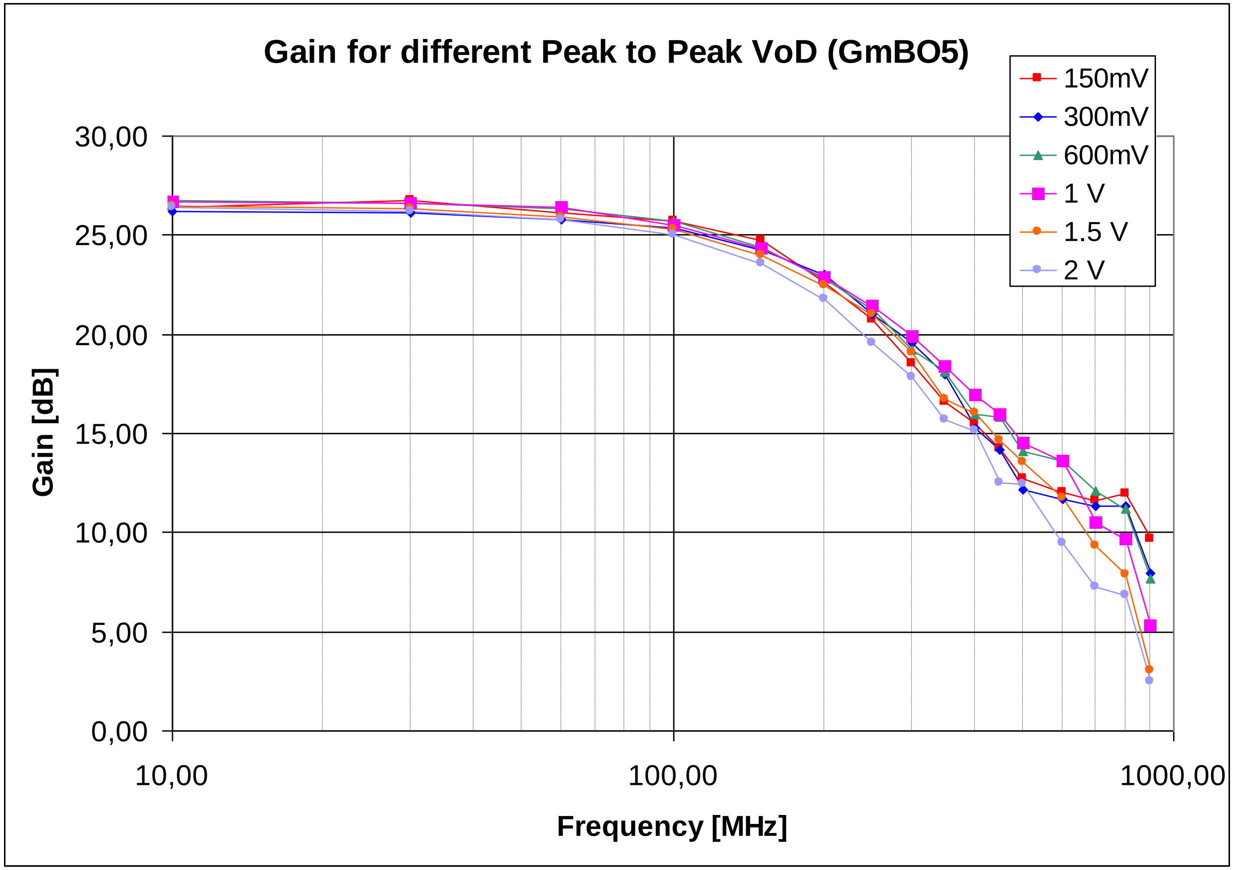
Ibb=104uA



Ibb=264uA

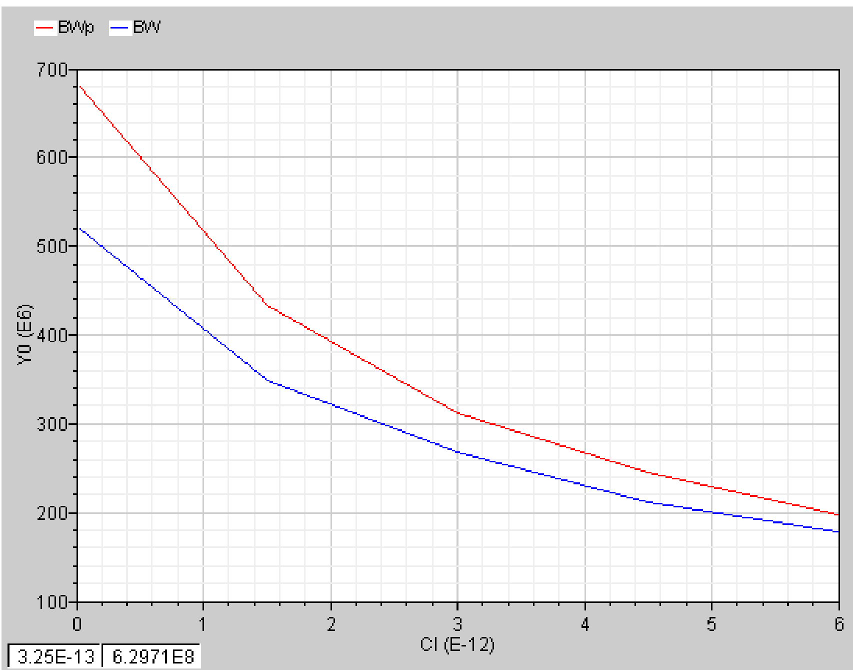
V. Bandwidth: GmBO5

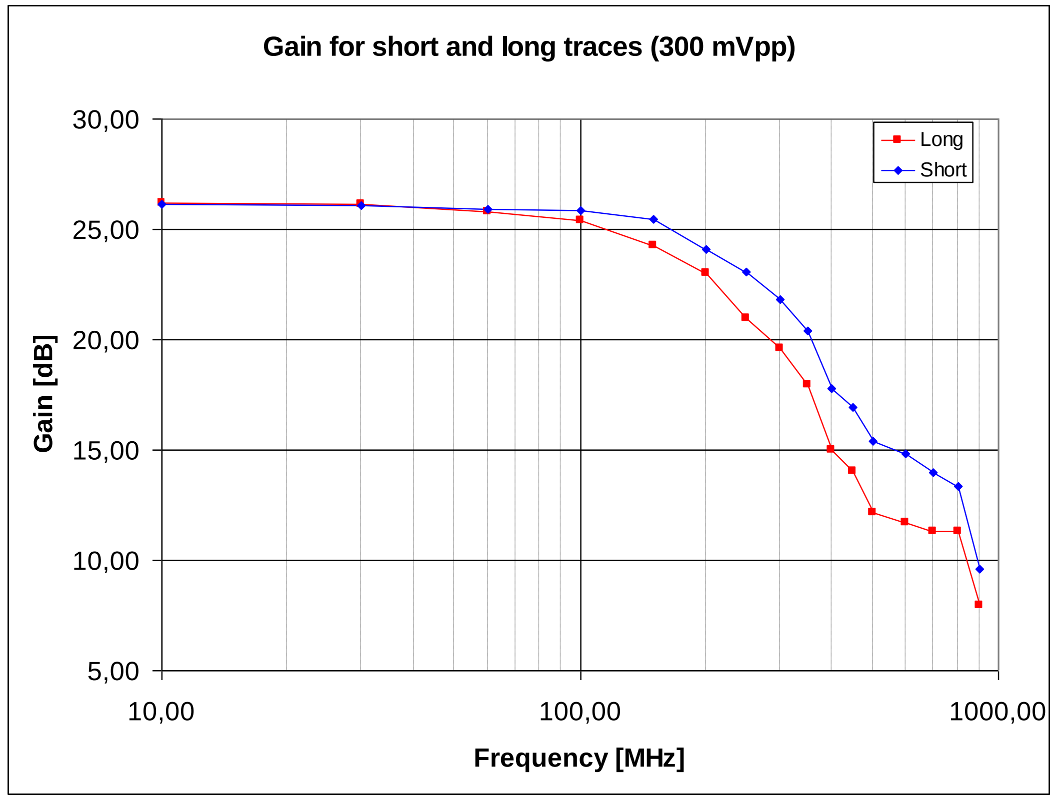
- Nice first order response with little non-linearity up to 2 V, but…
- However BW is only 200 MHZ
  - Rd was adjusted to have 300 MHz !!!
    - With an external Cload of 3 pF + extracted capacitances including pads



V. Bandwidth: GmBO5

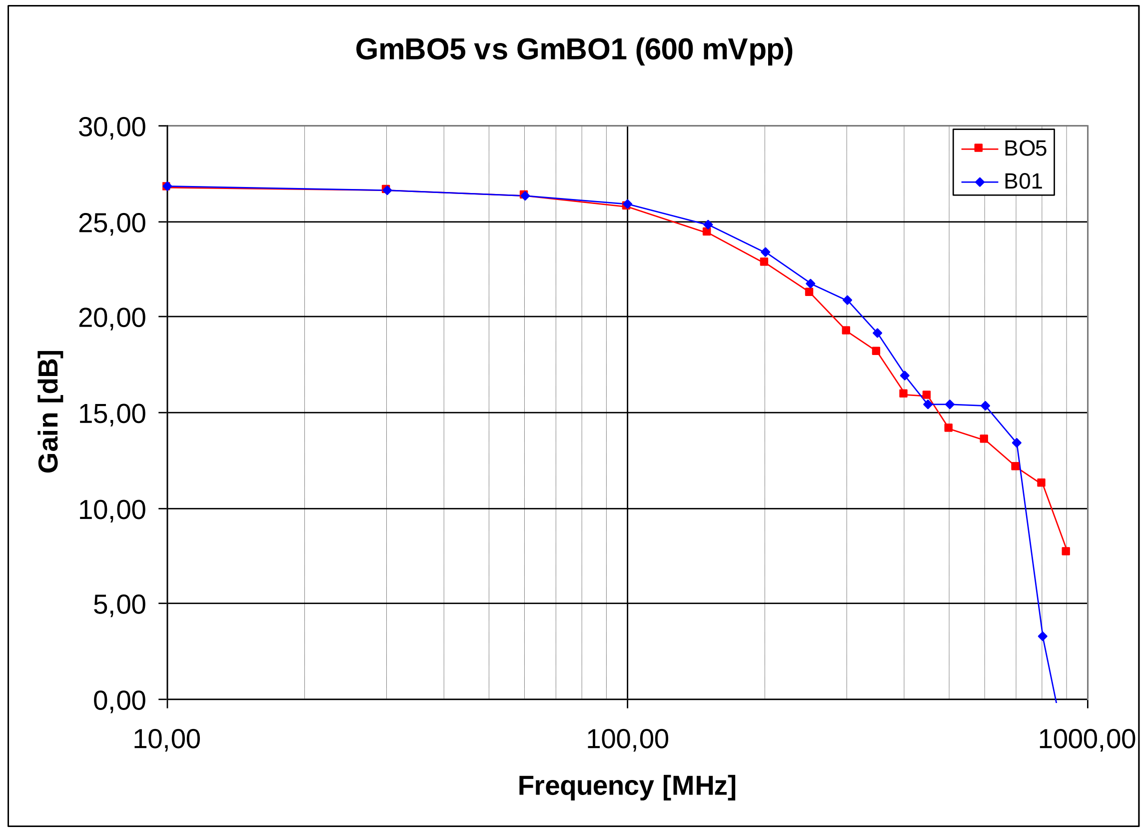
- It seems that the BW is dominated by the pole Rd*Cload
    - After some surgery it was possible to measure the BW with shorter PCB traces: increases to 250 MHz
    - The response looks like a first order response (up to 500 MHz)
- Possible explanation
    - External Cload is larger than expected
    - Process variation effects in R and C





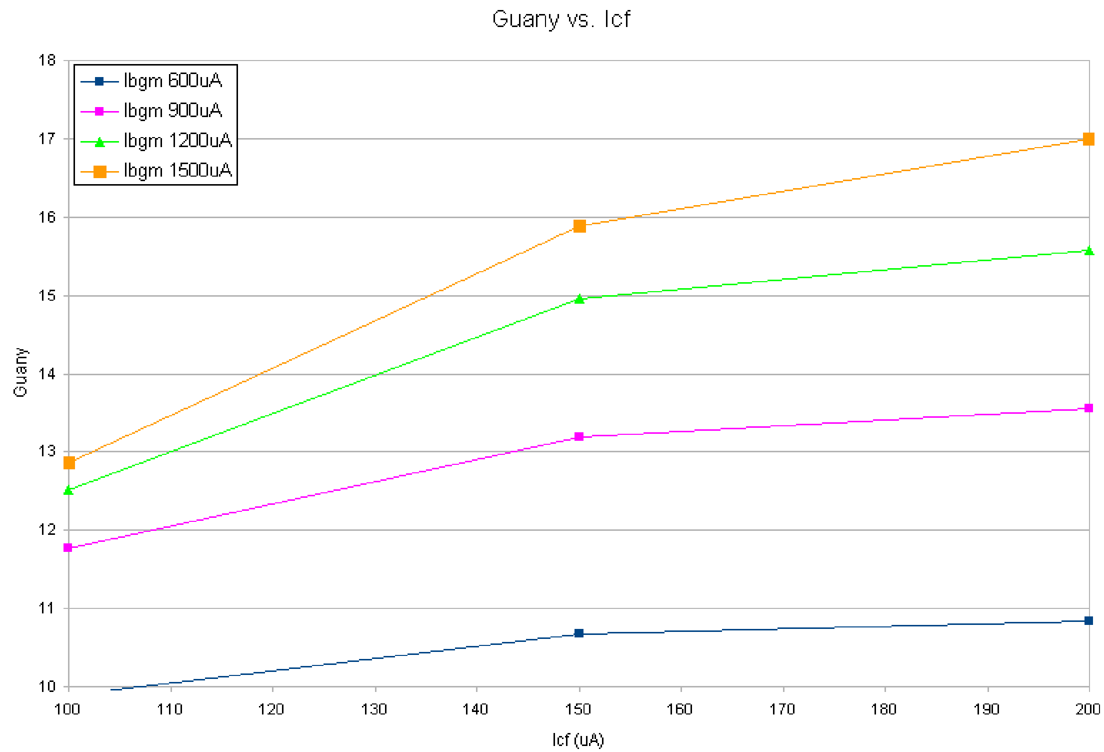
V. Bandwidth: GmBO5 vs GmB01

- Additional confirmation that the BW is limited by the Rd*Cload
  - The BW of GmBO1 is even larger
    - It has an additional buffer !
- Should be possible to achieve > 300 MHz BW for the full amplification
  - ACTA3 + NECTAR0 input buffer
  - Need a very careful tuning of Rd
    - BW vs stability
  - Environment more controlled
    - ACTA3 in NECTAR silicon
    - Postlayout simulation with Eric
- Side effect:
  - Underestimation of lin error ?
  - Seems to be enough margin…



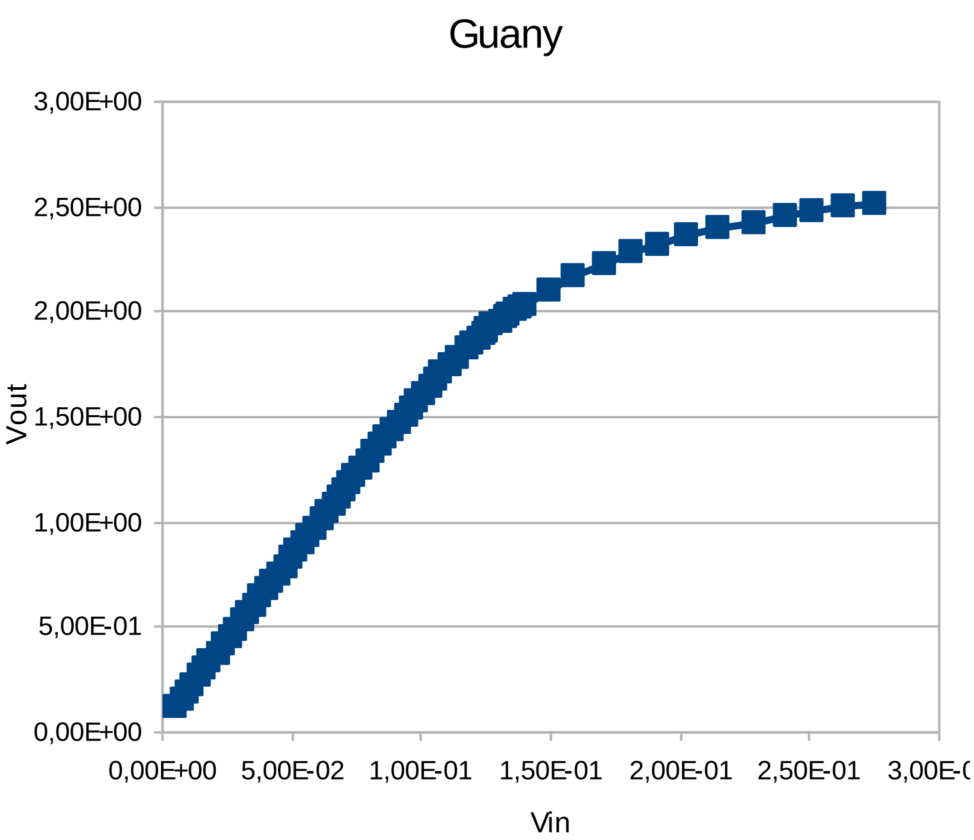
VI. Linearity

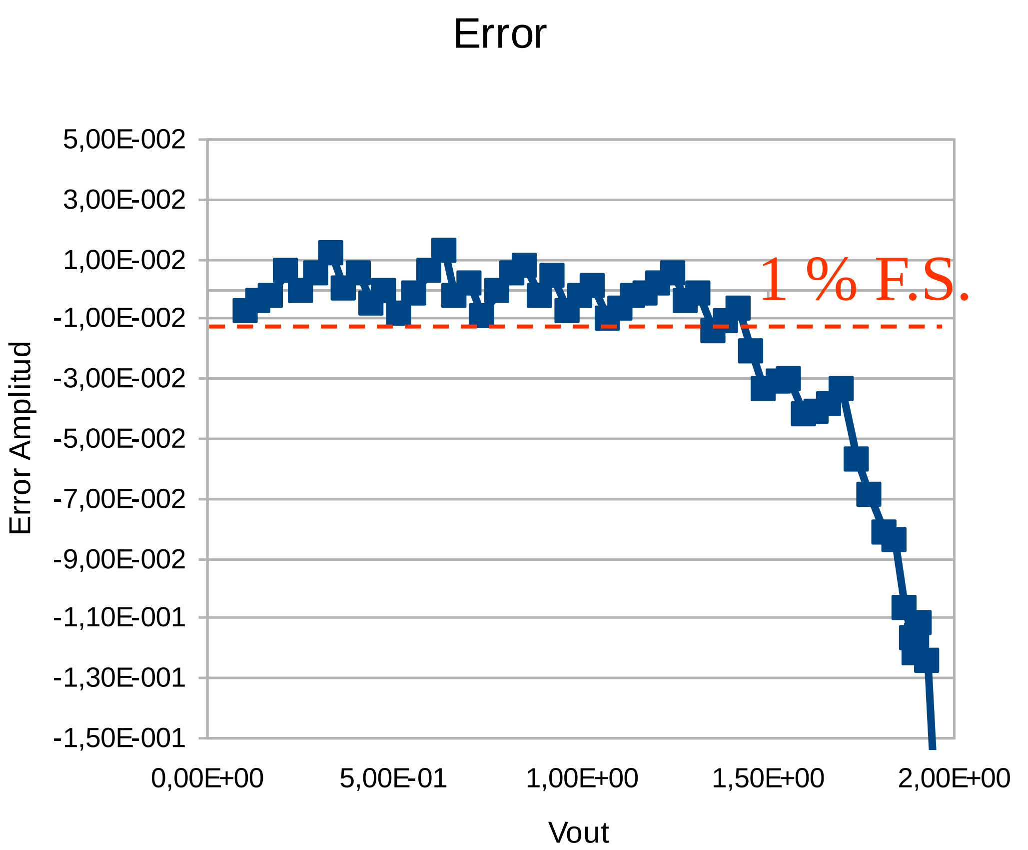
- Remember that gain depends on two bias current:
  - Ibgm: linearized transconducor differential pair tail current
  - Icf: current controlling floating voltage supply current
- "Nominal" condition is Ibgm=1500 uA and Icf=150uA (pulse gain = 16, DC gain = 20)
- Results will be shown for this condition
- Tested for other conditions, results available for other conditions:
  - Trade-off conssumption / linearty
    - Nominal conssumption is 10 mA



VI. Linearity: GmB05

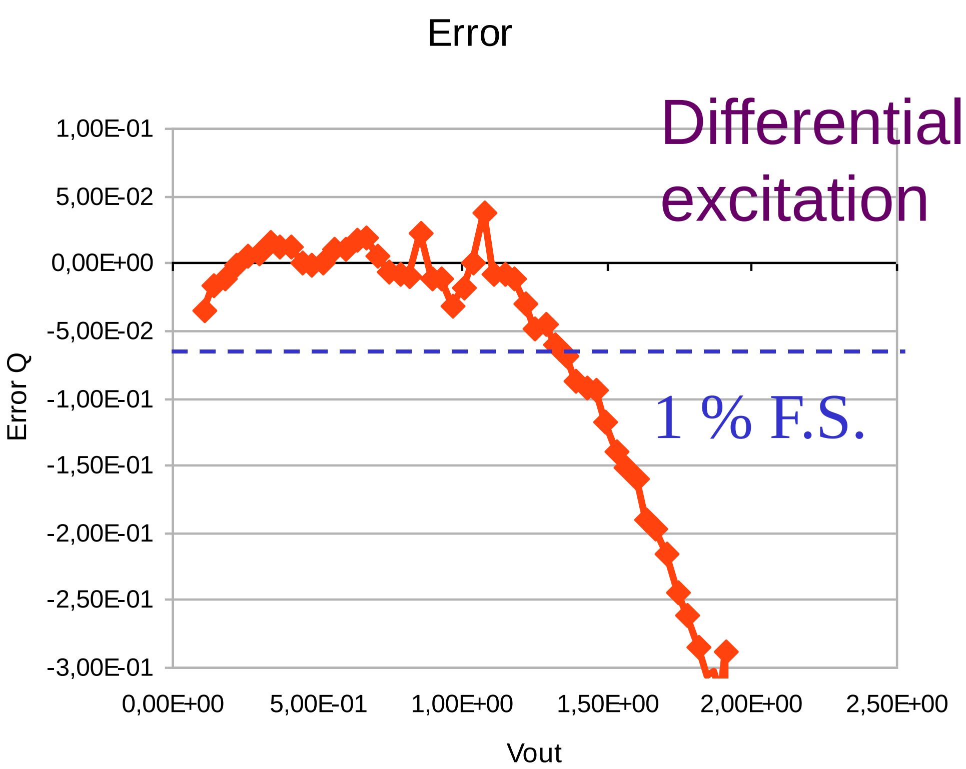
- *Amplitude measurement*
- *Linearity residue:*
  - < 1 % of the Full Scale (F.S.) for outputs < 1.3 Vpp
  - < 3 % F.S. for output < 1.6 Vpp

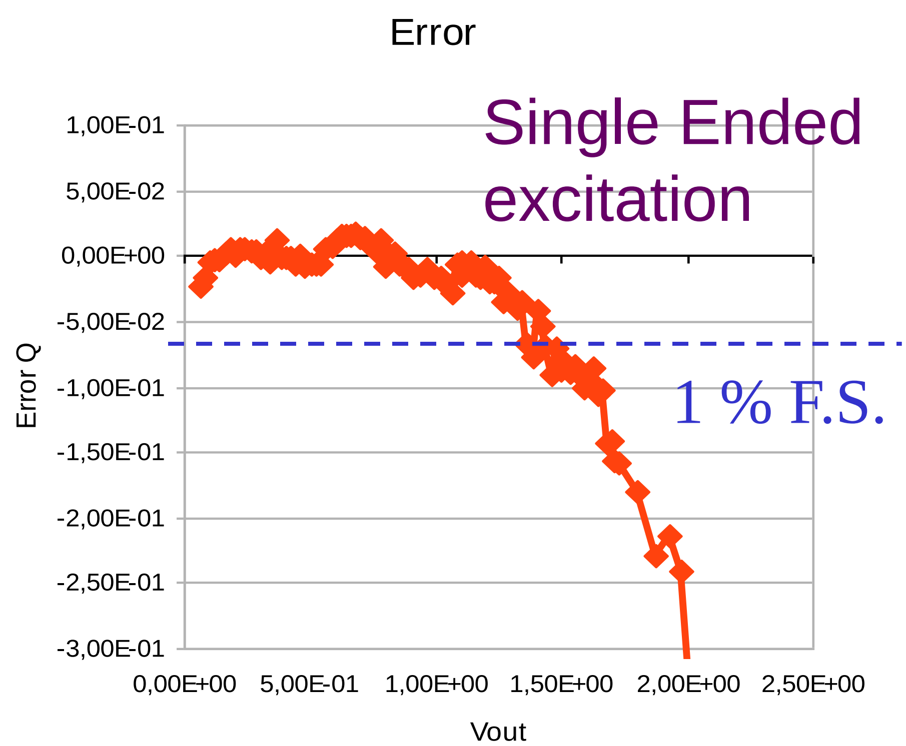




VI. Linearity: GmB05

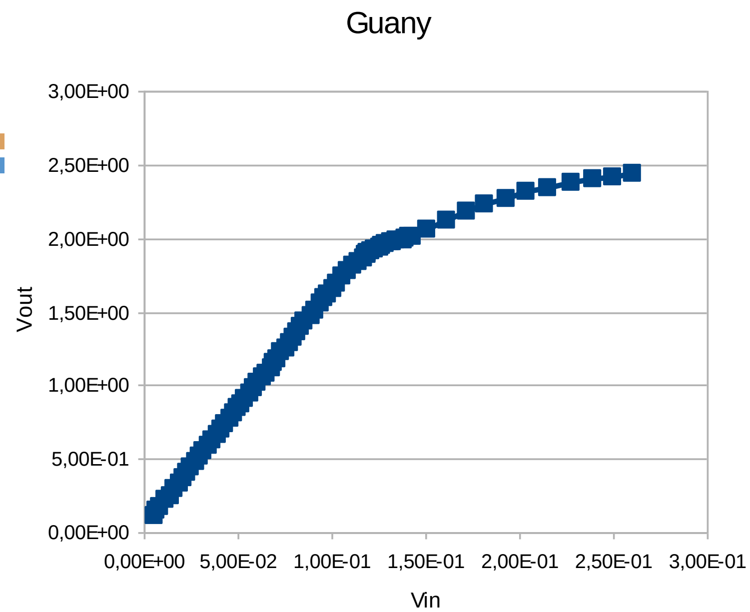
- Charge (area) measurement
- Linearity residue:
  - < 1 % of the Full Scale (F.S.) for outputs < 1.3 Vpp
  - < 3 % F.S. for output < 1.6 Vpp

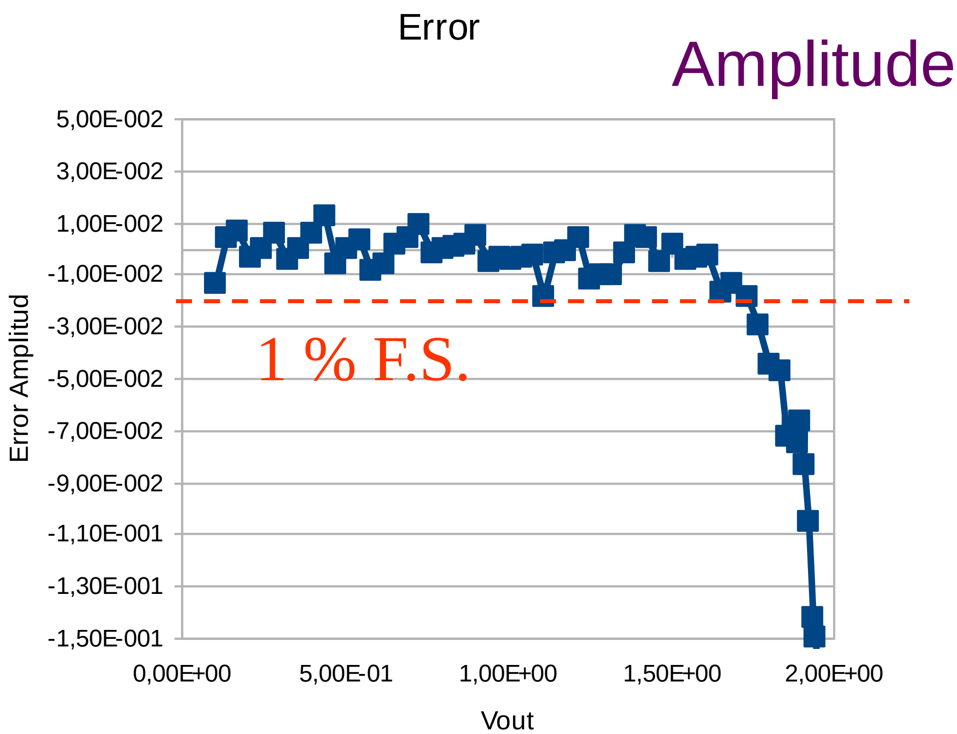


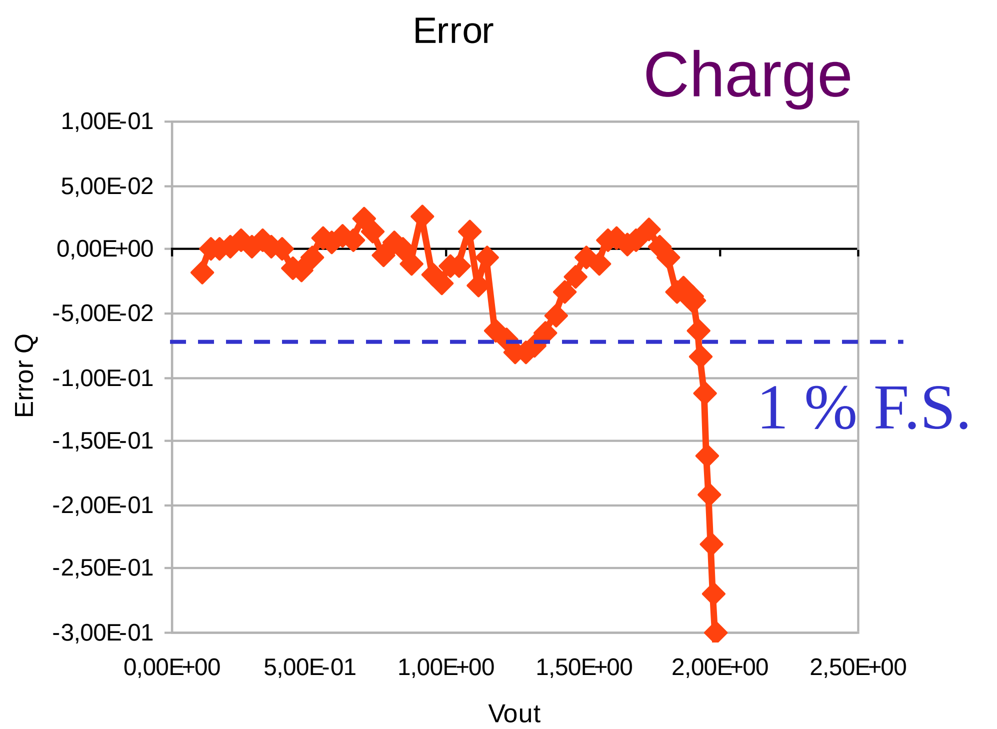


VI. Linearity: GmB01

- Similar to GmBO5

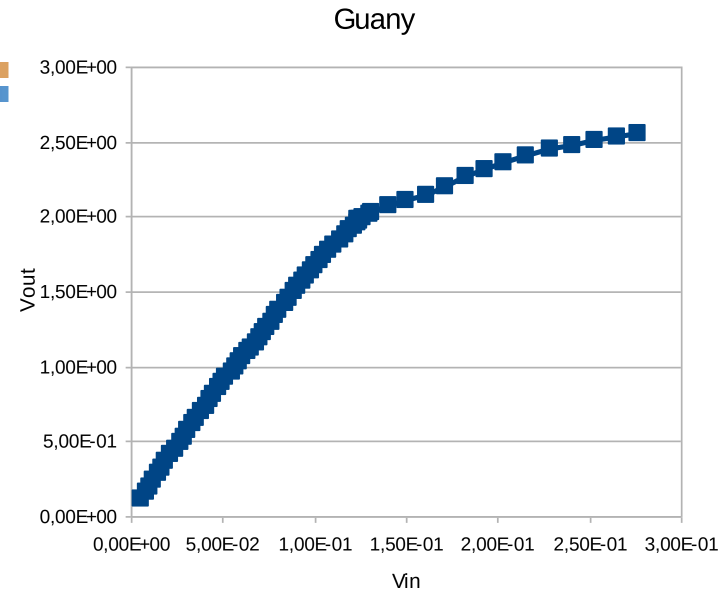


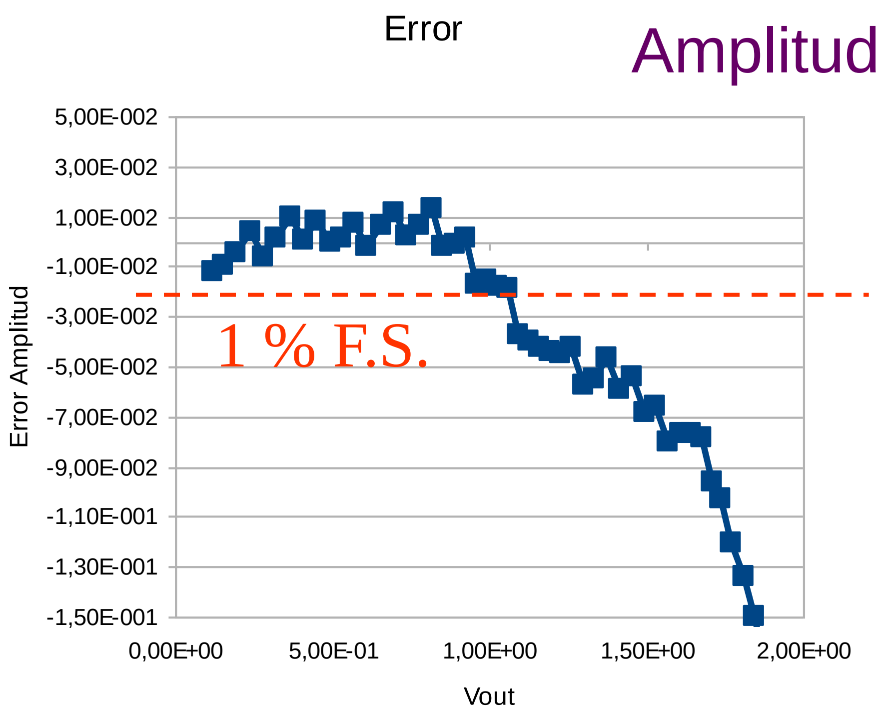


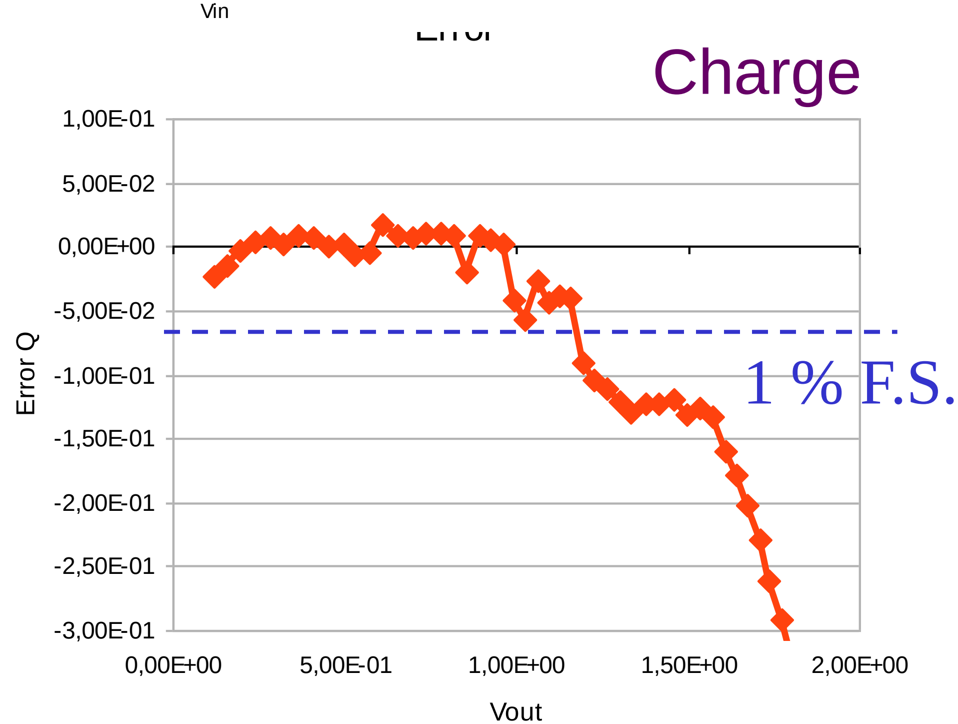


VI. Linearity: GmB0s1

- *Slightly worst*
- *Gain is 10 % higher*







IV. ACTA3: Offset generation: effect on linearity and gain

- Linearity is ok at the gain plateau
- Optimal region around Ibof 300 uA