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# UPGRADE OF THE CSC ENDCAP MUON PORT CARD AT CMS

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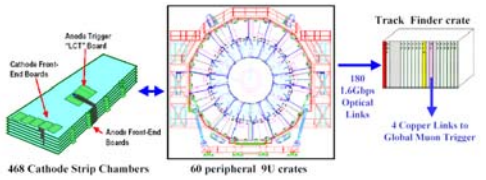
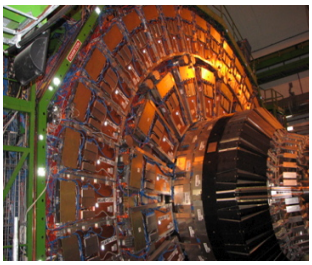
## ENDCAP MUON (EMU) CATHODE STRIP CHAMBERS AND TRIGGER ELECTRONICS




468 Cathode Strip Chambers  60 peripheral 9U crates

### Chambers and On-chamber Electronics

- 468 trapezoidal 6-layer multi-wire proportional chambers
- Located in the endcap regions of CMS and arranged in four stations ME1/2/3/4
- Intended for muon identification, triggering and momentum measurement
- Each chamber is equipped with:
  - 4 or 5 Cathode Front-End Boards (CFEB)
  - 12..42 Anode Front-End Boards (AFEB)
  - One Anode Local Charge Track (ALCT) Card



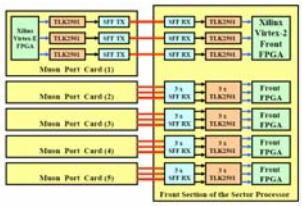
Endcap Cathode Strip Chambers (CSC) at CMS

### EMU Trigger Electronics

- Anode and Cathode track segments called Local Charged Tracks (LCT) are found independently using pattern recognition firmware
- ALCT and CLCT are combined in the Trigger Motherboard (TMB). Each chamber is served by one TMB.
- 60 9Ux400 mm VME crates are located on the periphery of the return yokes of CMS. Each crate houses:
  - Up to 9 Trigger Motherboards (TMB)
  - Up to 9 Data Acquisition Motherboards (DMB)
  - One Muon Port Card (MPC)
  - One Clock and Control Board (CCB)
  - One custom VME Crate Controller (VCC)
- Up to two combined LCTs are sent from each TMB to the MPC over point-to-point backplane lines in the peripheral crates.
- MPC performs sorting (based on 4-bit "Quality" value of the LCT), selects the three "best" LCTs and transmits them to the Sector Processor in the Track Finder crate in the underground counting room.
- The Track Finder crate comprises:
  - 12 Sector Processors (SP)
  - One Muon Sorter Board (MS)
  - One Clock and Control Board (CCB)
  - One Detector Dependent Unit (DDU) Card
  - One CAEN V2718 VME Crate Controller
- On top of the CSC Trigger chain, the Muon Sorter selects 4 "best" muon patterns and transmits them to the Global Muon Trigger receiver board via dedicated copper links at 40MHz

## PRESENT TRIGGER OPTICAL LINK AND MOTIVATION FOR THE MUON PORT CARD UPGRADE

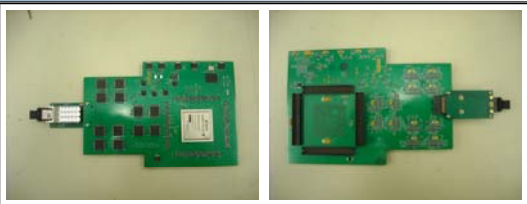
Muon Port Card with old Virtex-E mezzanine (left) and Sector Processor (right)




Present optical link to the CSC Track Finder

- Preliminary results of simulation at the top SLHC luminosity of $10^{35}cm^{-2}s^{-1}$ suggest that the occupancies of the CSC system will increase due to prompt pile-up, higher neutron background and larger average number of LCTs from the most critical inner ME1/1 chambers
- The probability to see more than two LCTs in the ME1/1 is still quite low (0.6%), so the present TMB-to-MPC interface, peripheral backplane, TMB and MPC main boards may remain unchanged
- MPC should be able to send up to 12 pre-sorted LCTs/BX to the upgraded Track Finder. Need to increase the bandwidth of optical links and enhance sorting capabilities
- Ultimate solution: transmit all 18 LCTs to the Track Finder every bunch crossing with or without sorting

## NEW VIRTEX-5 MEZZANINE BOARD



Top and bottom views with the SNAP12 transmitter attached

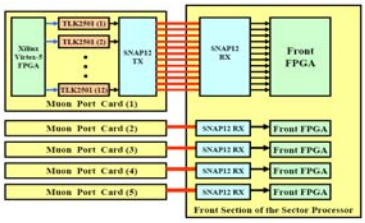
- Xilinx XC5VLX110-1FF1153C FPGA with XCF128X PROM
- Virtex-5 inputs/outputs are compatible with the 3.3V logic levels on the main Muon Port Card board
- 12 Texas Instruments TLK2501 transmitters
- 12 LCTs @ 80MHz or all 18 LCTs @ 120MHz to Track Finder
- Two CERN-designed QPLL2 ASIC to obtain low jitter 80MHz or 120MHz clock for the TLK2501 serializers
- 12-channel parallel SNAP12 optical transmitter is mounted on a small plug-in board that is attached to the mezzanine from the back

Pluggable 12-channel optical transmitter

## UPGRADED MUON PORT CARD AND OPTICAL TRANSNISSION SYSTEM

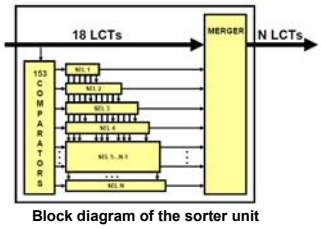
Muon Port Card with the new Virtex-5 FPGA mezzanine

- Upgraded Muon Port Card supports 3 "old" 1.6Gbps links and 12 "new" links (1.6Gbps @ 80MHz or 2.4Gbps @ 120MHz)
- Main MPC board remains unchanged
- Minor modification of the front panel for an additional optical cable
- One 12-fiber optical cable from the MPC to the upgraded Sector Processor
- Use embedded FPGA deserializers in the front FPGA of the SP
- Front section of the future SP would be greatly simplified




Upgraded CSC Trigger optical link system

## FIRMWARE DEVELOPMENT AND HARDWARE TESTS




Block diagram of the sorter unit

### Sorter Unit

- Upgraded from "3 best LCTs out of 18" to "12 best LCTs out of 18"
- Sorting process in three steps:
  - 153 comparisons between all patterns
  - quick sequential sorting to define the addresses of the "best" patterns
  - merging of input patterns
- Extra latency = two bunch crossings (50 ns)
- Supports both 3 "old" and 12 "new" links
- Additional output FIFO buffers for debugging and testing purposes

Test Crate

### Current Status and Initial Tests

- Two prototypes of the FPGA mezzanine and three SNAP12 plug-in boards have been assembled and tested in summer 2010
- Initial tests were performed at 80MHz
- Successfully ran the data transmission test in the fully loaded peripheral crate from 9 TMBs to the MPC. "Safe window" of data latching into the Virtex-5 was measured and found to be the same as for older Virtex-E, as expected.
- 12 channels of SNAP12 transmitter were checked using one of our custom evaluation boards with the TLK2501 receiver. Channel-by-channel test with the PRBS and limited number of test patterns.

## CONCLUSION, FUTURE PLANS, REFERENCES

### Conclusion

- The idea of using a mezzanine FPGA on a host motherboard was adopted by the CSC electronic designers approximately 10 years ago and has proven to be very useful. Some of the boards have already been updated (SP) and the others, like TMB and MPC, will be updated within few years. This is a straightforward evolutional approach which allows to keep the infrastructure and expensive electronic components intact for many years while upgrading the most critical processing and data transmission units such as the FPGA and optical links.
- Using of compact parallel 12-channel optical modules allows us to operate at modest rates of 1.6Gbps or 2.4Gbps synchronously with the LHC bunch crossing frequency while increasing the overall throughput several times to be able to transmit all the trigger primitives from each chamber to the CSC Track Finder.
- More sophisticated sorters with minimal additional latency are easily implemented in the Virtex-5 FPGA
- Seamless integration into the present trigger system. Interfaces to "old" and "new" Track Finders are available on the same Muon Port Card.

### Future Plans

- Optical tests with the fully functional SNAP12 receiver board with an embedded FPGA deserializers, when it becomes available as a part of the CSC Track Finder upgrade project (late 2010-early 2011)
- Irradiation tests of the Virtex-5 FPGA and other new components
- Modify the project for 120MHz operation

### References

[1] Virtex-5 FPGA Mezzanine Draft Specification:
http://bonner-ntserver.rice.edu/cms/projects.html#mpcmez
[2] Muon Port Card Specification: http://bonner-ntserver.rice.edu/cms/MPC2004_100808.pdf
[3] TLK2501 Gigabit Transceiver Specification: http://focus.ti.com/lit/symlink/tlk2501.pdf
[4] SNAP12 Specification: http://bonner-ntserver.rice.edu/cms/snap12msa_051202.pdf
[5] Custom evaluation optoboards designed at Rice University:
http://bonner-ntserver.rice.edu/cms/projects.html#opto