The Gigabit Link interface Board (GLIB), a flexible system for the evaluation and use of GBT-based optical links

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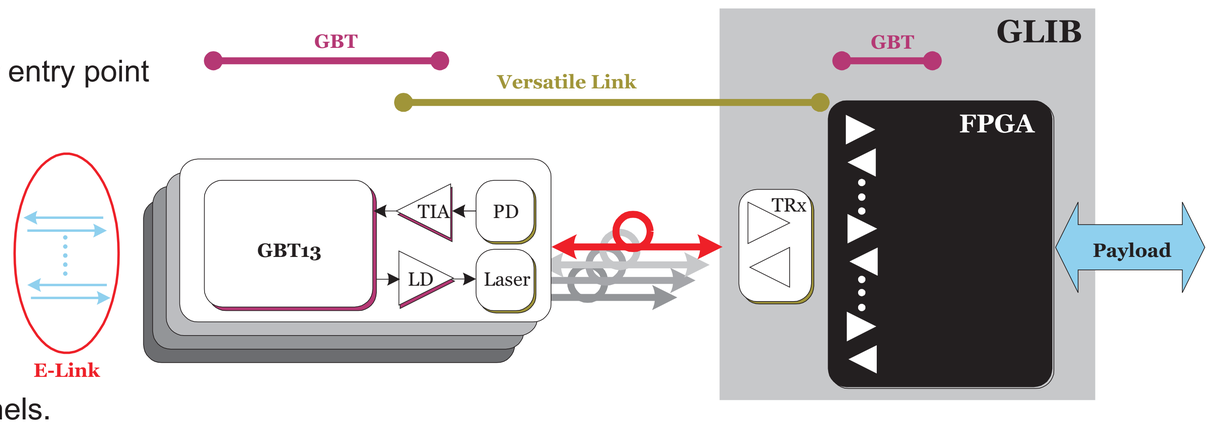
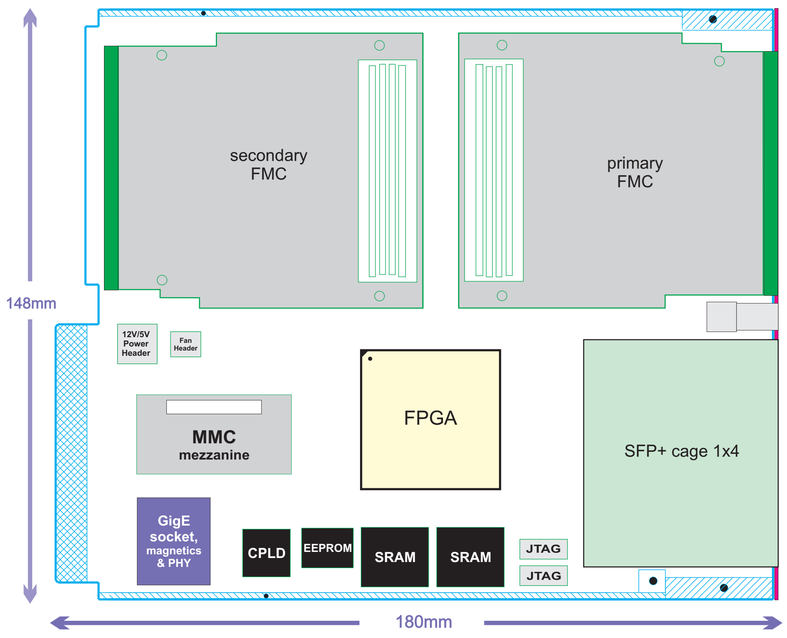
THE CONCEPT

The Gigabit Link Interface Board (GLIB) is an evaluation platform and an easy entry point for users of high speed optical links in high energy physics experiments.
Its intended use ranges from optical link evaluation in the laboratory to control, triggering and data acquisition from remote modules in beam or irradiation tests.
Each GLIB card can process data to/from four SFP+ transceiver modules, each operating at bi-directional data rates of up to 6.5 Gbps. This performance matches comfortably the specifications of the GBT/Versatile Link project [1][2] with its targeted data rate of 4.8 Gbps.
In its simplest form, one GLIB board thus interfaces with up to four GBT channels.



THE IMPLEMENTATION

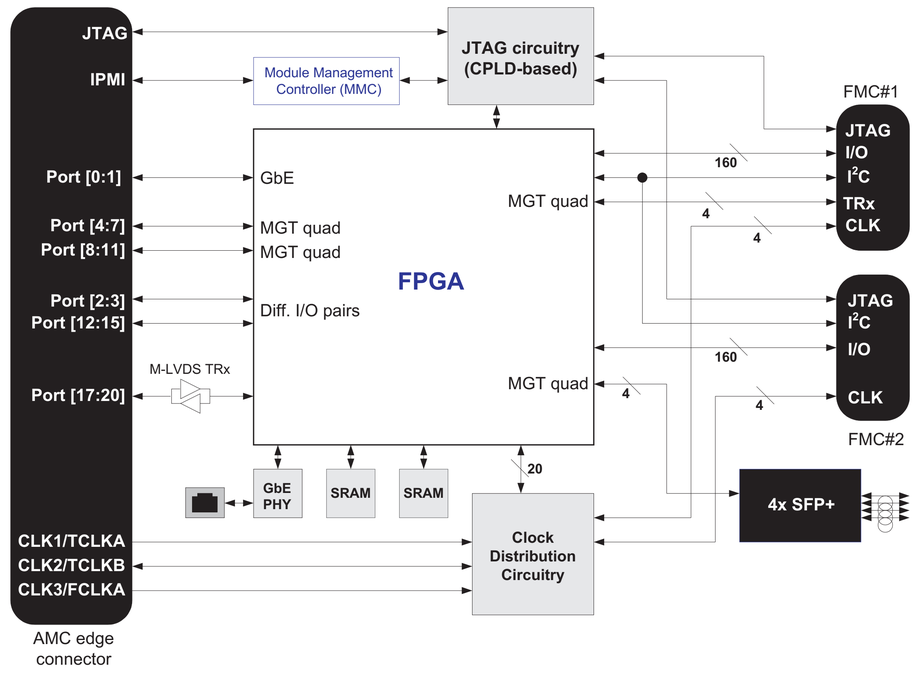
The GLIB is a double width Advanced Mezzanine Card (AMC) conceived to serve a small and simple system residing either inside a µTCA crate or on a bench with an optional link to a PC.



The GLIB I/O capability can be further enhanced with two FPGA Mezzanine Cards (FMC). This gives users the flexibility to adapt the GLIB interface to their system, by for instance adding connectivity to the TTC network at the backend, or connecting to e-links at the frontend.

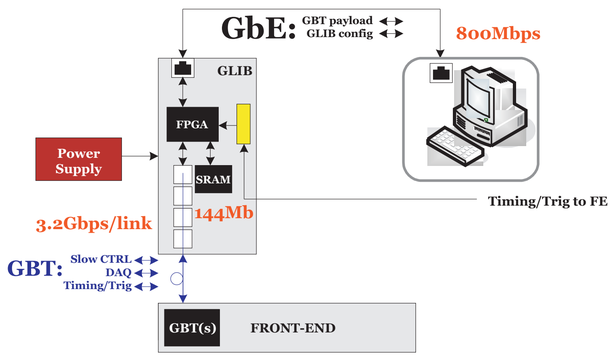
The GLIB is based on the XC6VLX130T FPGA of the Virtex-6 family by Xilinx Inc.
It provides GbE as well as PCIe links to the AMC edge connector. There is possibility to implement other protocols instead of PCIe. The board management when in a µTCA environment is performed by an Module Management Controller (MMC) mezzanine card [3].

When in bench-top mode, it can interface to a PC either through a standard Ethernet cable and/or a PCIe adapter card. Its sophisticated clock distribution circuitry offers user flexibility. On-board SRAM is also available.

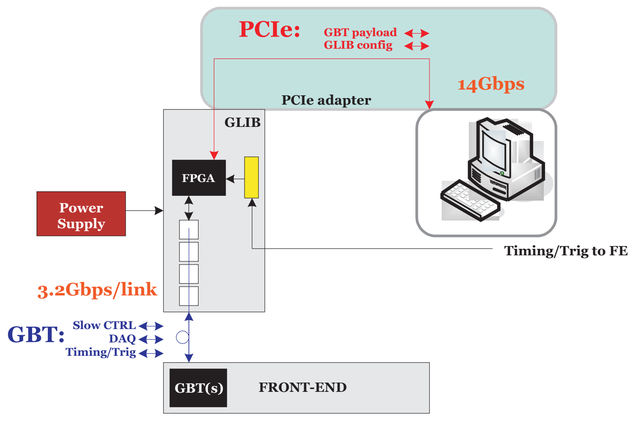


TYPICAL USE CASES

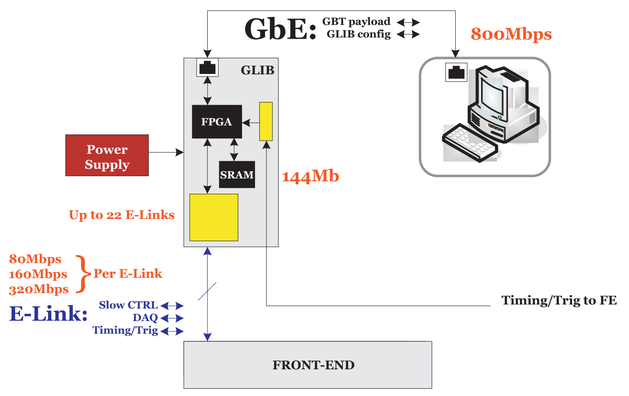
Bench-top test beam setup



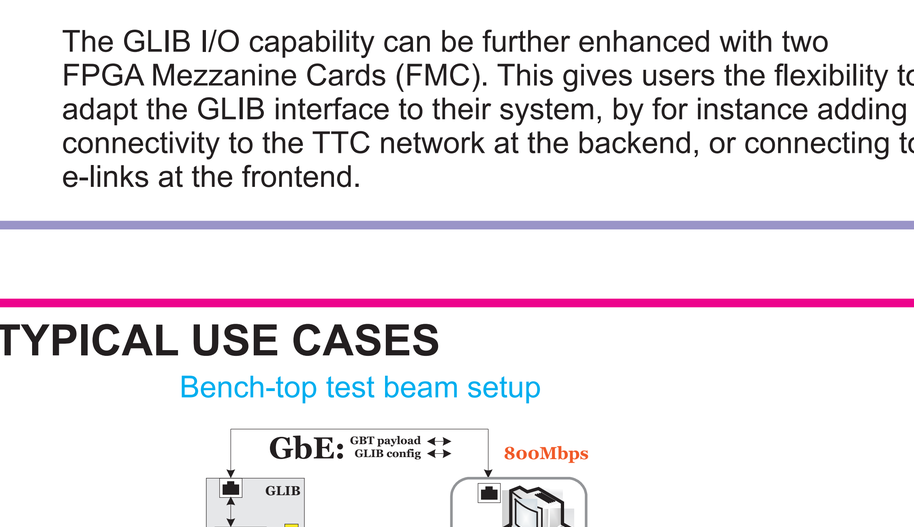
Bench-top front-end module test setup



Bench-top system test setup



Crate system test setup



=TTC FMC =E-LINK FMC =SFP+

STATUS

SPECIFICATIONS: version 1.8 available.
SCHEMATIC: Ready to be submitted for layout design.
LAYOUT: Scheduled to start on October 4, expect to be ready end of 2010.
µTCA ENVIRONMENT: Under preparation. System components ordered:
- Schroff 11850-019 6 slot uTCA for physics crate. Expected beginning of October 2010.
- Kontron AM4904 MCH. Expected end of September 2010.
- Kontron AM5030 CPU. Expected end of September 2010.

TEST ENVIRONMENT: Development in early 2011.
FIRST PROTOTYPE: Expected in spring 2011.

For more information
GLIB project homepage: https://espace.cern.ch/project-GBLIB/public
Contact: Paschalis.Vichoudis@cern.ch

REFERENCES

[1] P. Moreira et al “The GBT, a proposed architecture for multi-Gb/s data transmission in high energy physics”, proceedings of the Topical Workshop on Electronics for Particle Physics TWEPP-07, CERN-2007-07 (2007) pg. 332–336
[2] L. Amaral et al “The versatile link, a common project for super-LHC”, 2009 JINST 4 P12003
[3] E. Aslanides et al "MMC mezzanine board specifications v2.0”, LHCb Technical Note