Development of custom radiation-tolerant DCDC converter ASICs

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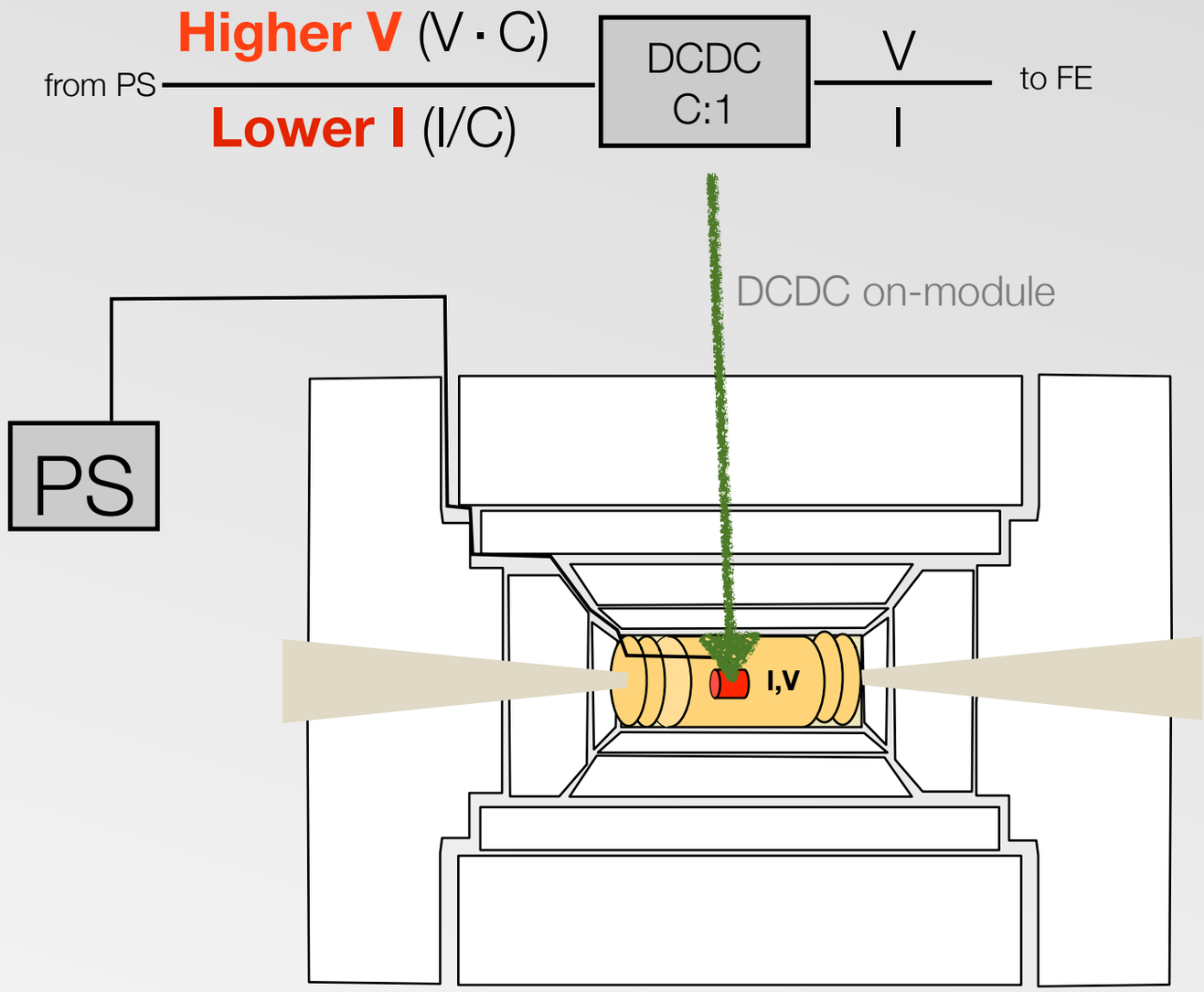
Outline

- Introduction
- Chronology of ASIC DCDC prototypes
- Characteristics and electrical performance of the ASICs
- A bad surprise
- Radiation tolerance
- Conclusion

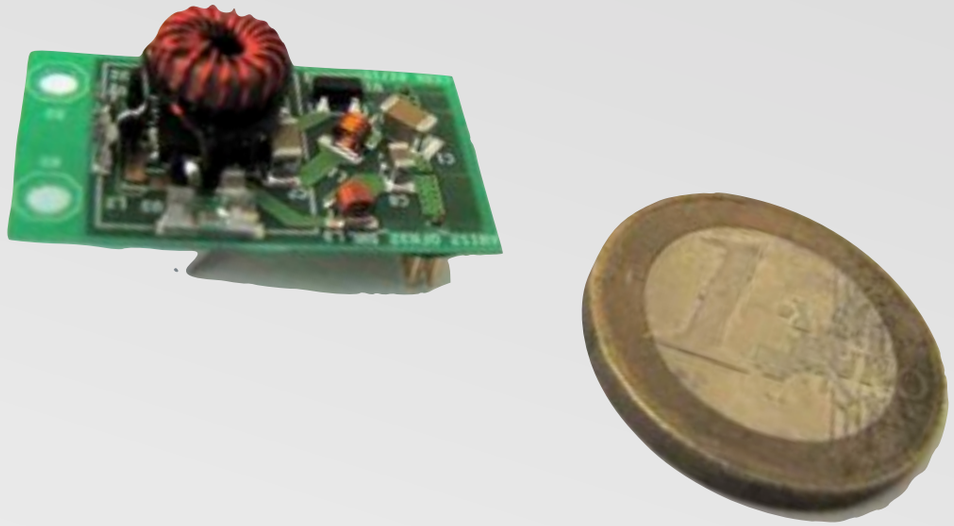
Introduction

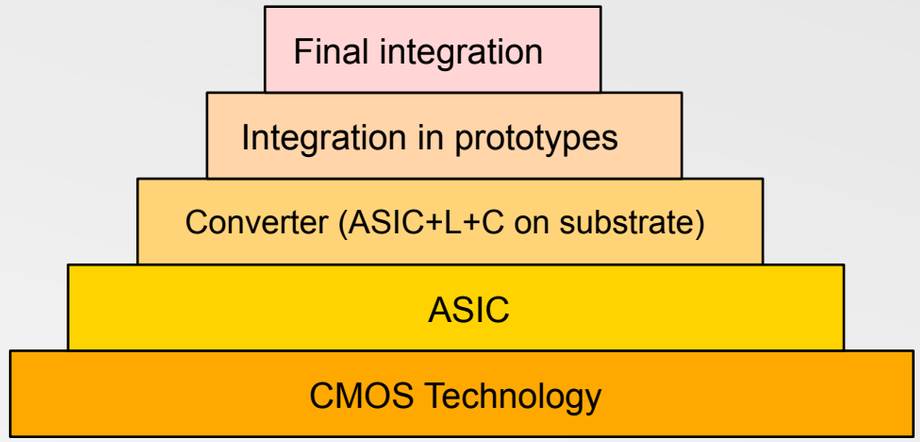
- Work in preparation of LHC detectors' upgrades
- Local on-detector V conversion allows distributing power at higher voltage
  - Lower mass
  - Less heat to be removed
  - Smaller volume of cables to bring power inside the experiment
- DCDC converter for on-module integration has to be radiation and magnetic field tolerant



Target of DCDC development

- Development of a low-volume, low-mass, radiation and magnetic field tolerant DCDC converter
  - Choice of ‘buck’ architecture presented at TWEPP08 after a detailed study of a set of possible solutions
- Building blocks for a successful development have been listed at TWEPP09
- One of the fundamental blocks is a DCDC ASIC embedding the control circuitry and the power switches
  - This requires a CMOS technology with radiation-tolerant power MOS





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Chronology of ASIC prototypes

	Tech.	When	LDMOS used
TID and p test of '0.35 technology' completed			
DCDC35B	0.35µm	Tape-out: 10/08	Lateral NMOS 14V
TID and p test of 5 candidate technologies completed: choice of 0.25µm			
DCDC25A	0.25µm	Tape-out: 5/09	Lateral NMOS (22V) and PMOS (16V) Generation 2A
TID and p test of 0.25µm LDMOS Generation 2A and 2B completed : same results **BUT** foundry moved to Generation 3 for all MPWs			
DCDC25B	0.25µm	Tape-out: 1/10	Lateral NMOS (22V) and PMOS (19V) Generation 3 + Isolated Lateral NMOS (13V)
SEBchip	0.25µm	Tape-out: 11/09	Test Generation 3 LDMOS for full radiation tests

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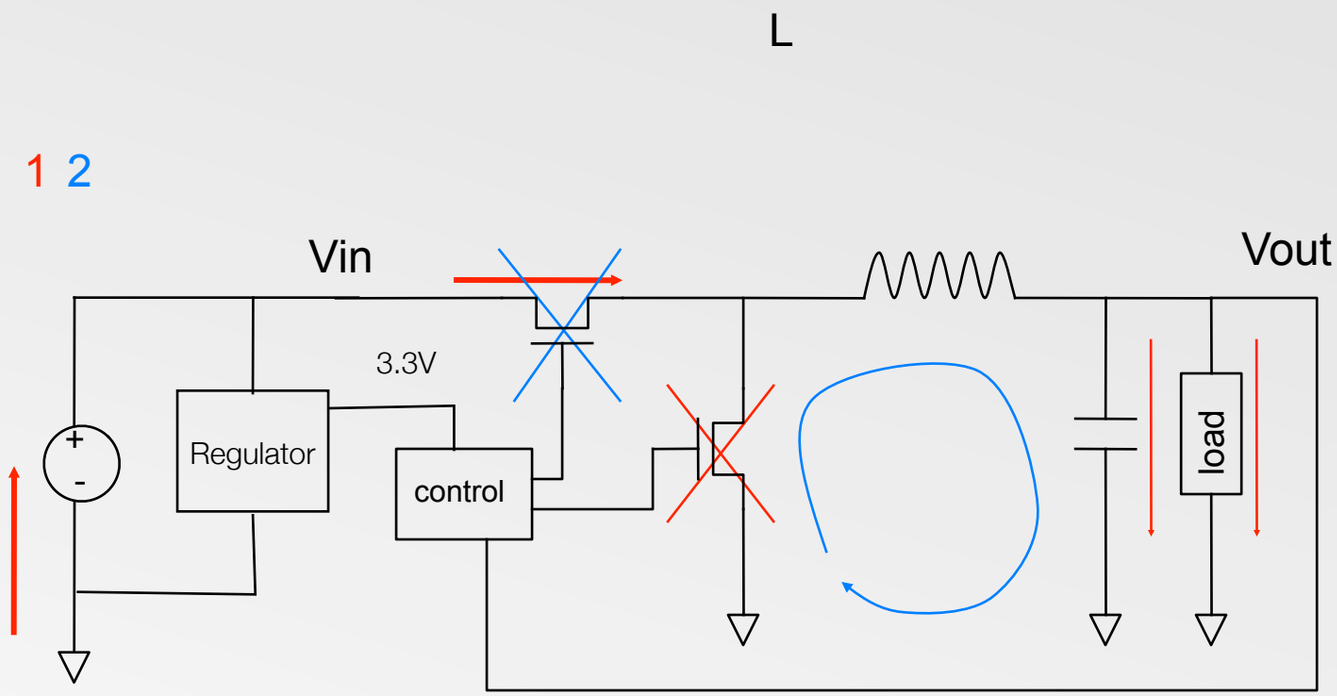
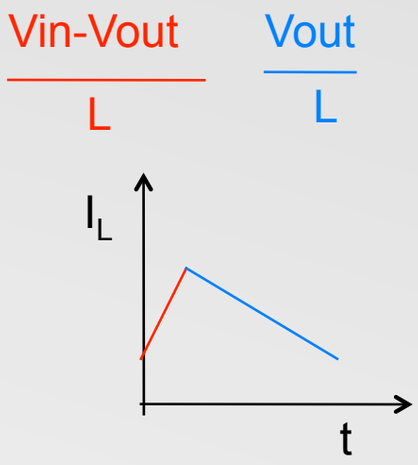
How a synchronous ‘buck’ DCDC works





$$\frac{Vout}{Vin} = \text{Duty cycle}$$

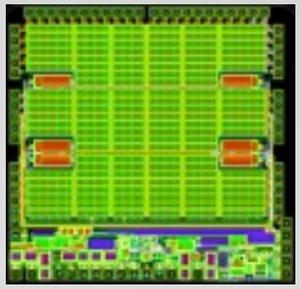
L determines peak-peak => implication on switching frequency (air-core = low L = high f of 1-4MHz)

Embedded functionalities of different prototypes

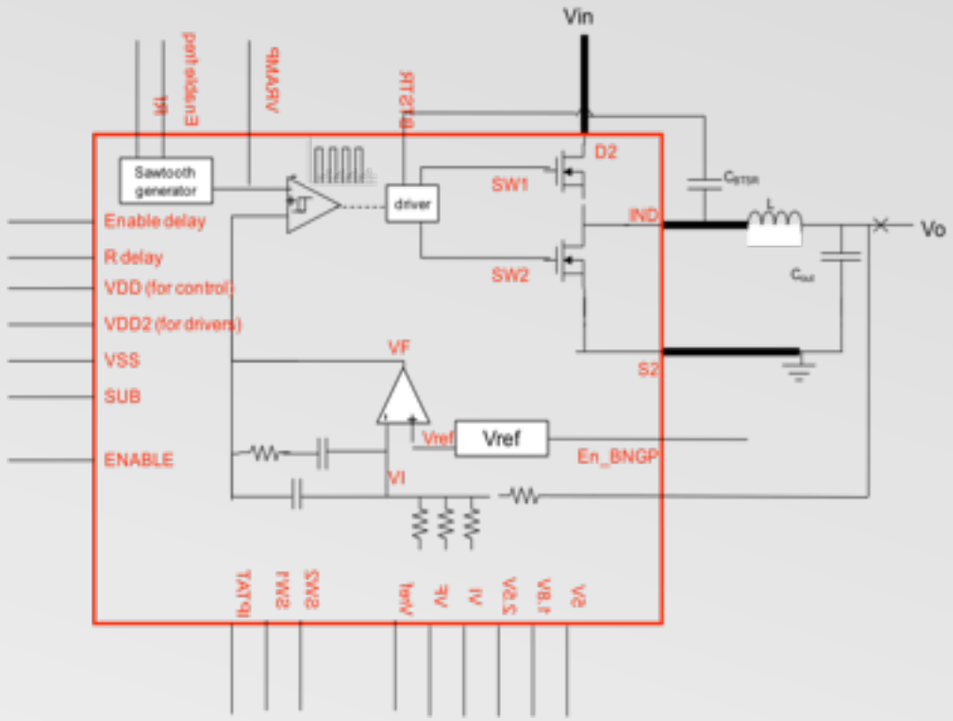
	DCDC35B	DCDC25A	DCDC25B	Next*
Full control loop	✓	✓	✓	✓
Dead times' handling	Fixed	Adaptive (QSW)	Adaptive (QSW and CCM, sharp transition)	Adaptive (QSW and CCM, smooth transition)
On-chip regulator(s)	No	No	✓	✓
Soft Start	Simple RC	Simple RC with comparators	Full sequence with comparators	State machine
Over-I protection	No	No	✓	✓
Over-T protection	No	No	No	✓
Under-V disable	No	No	No	✓

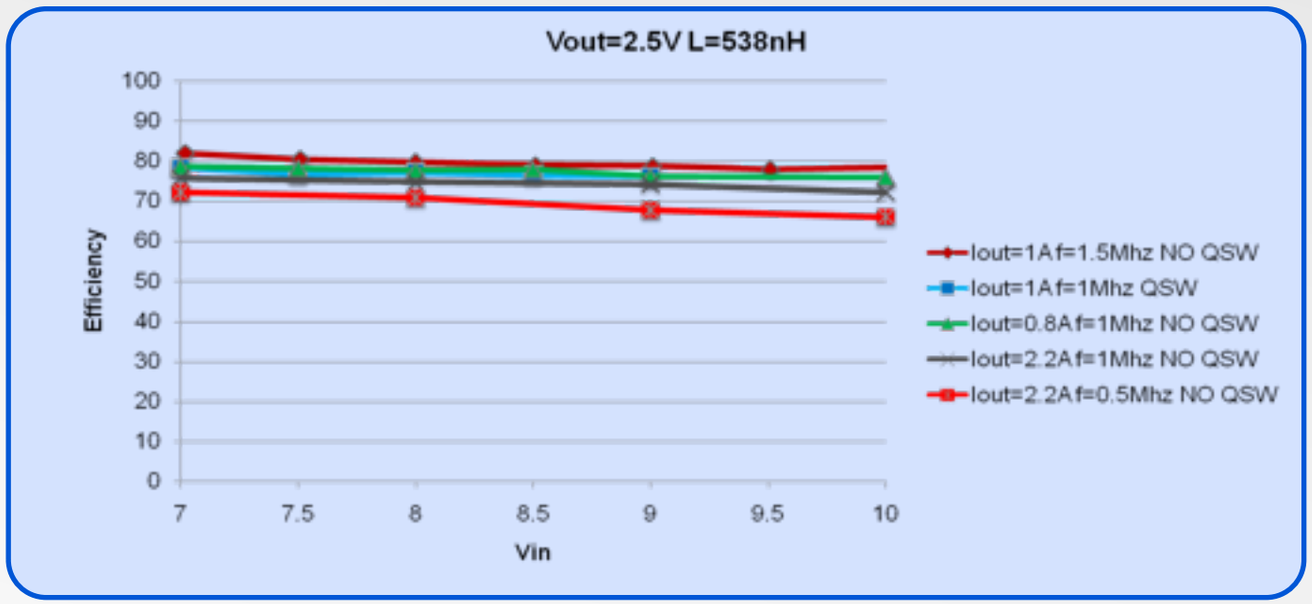
*Full design complete at schematic level (including start-up and protection features simulated with a behavioral model for the converter)

DCDC35B

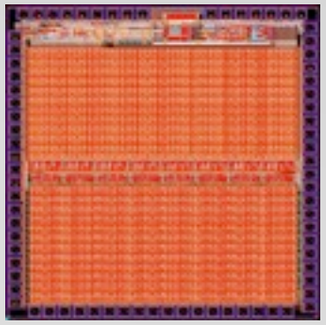


- Lateral HV NMOS transistors are used as power switches
- VIN and Power Rail Operation from +3.3V to +12V
- Internal oscillator fixed at 1Mhz, programmable up to ~4MHz with external resistor
- Internal voltage reference
- Programmable delay between gate signals
- Integrated feedback loop with bandwidth of 20Khz
- Different Vout can be set: 1.2V, 1.8V, 2.5V, 3V, 5V
- Size: ~2.7 x 2.7 mm
- Widely used in system tests

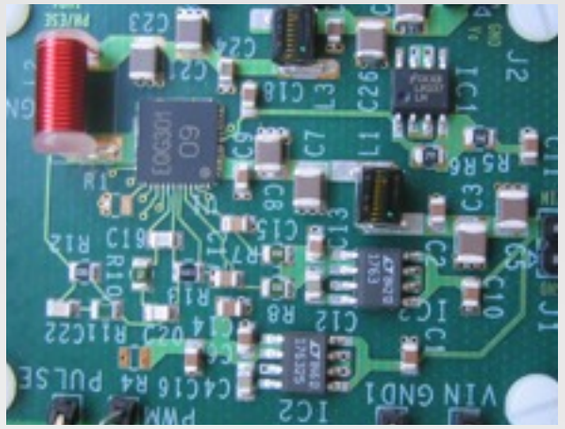




DCDC25A

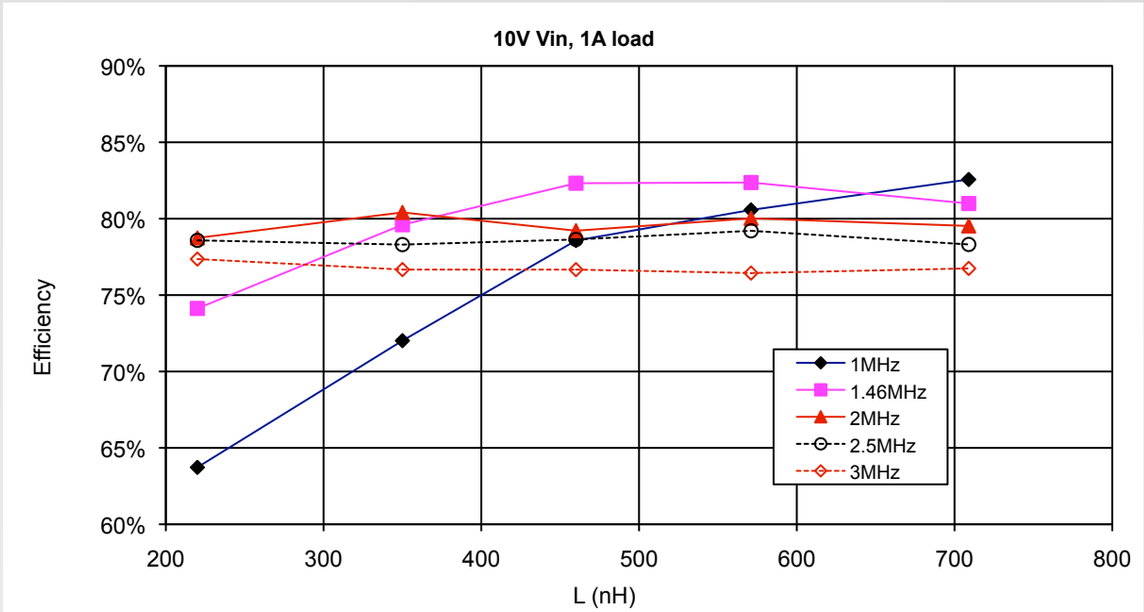


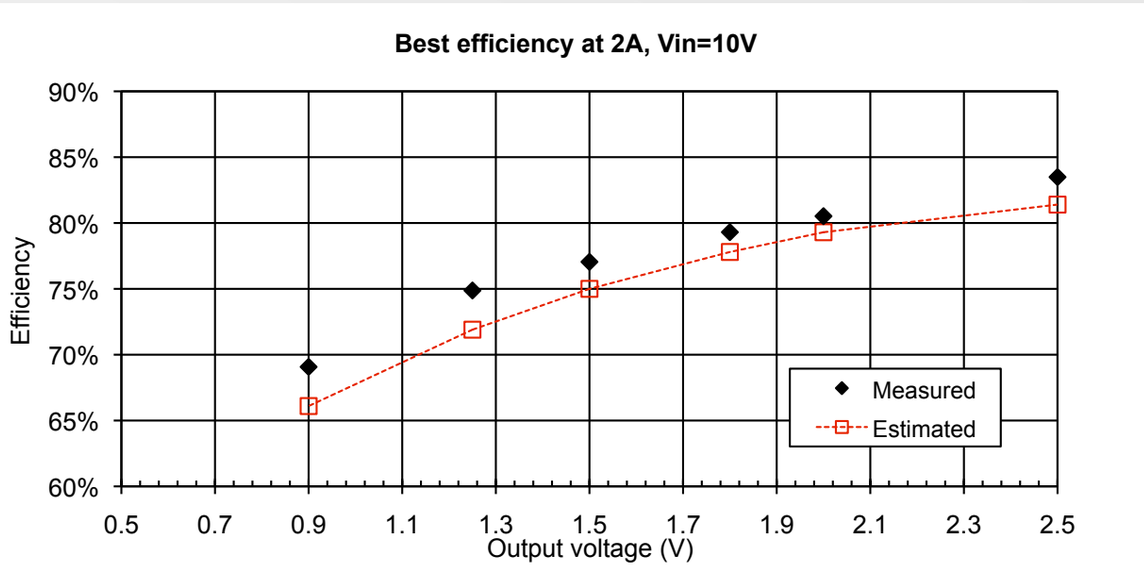
- First prototype in the 0.25µm technology
- Lateral HV NMOS (low-side) and PMOS (high-side) transistors are used as power switches - Generation 2A devices
- Internal oscillator fixed at 2MHz, but programmable with external resistor
- Voltage reference and regulated voltages (2.5V, Vin-2.5V) to be provided from outside
- Delay between gate signals automatically set (adaptive), but fixed for 1 transition in CCM
- Compensation network off-chip
- Programmable Vout (from reference)
- Size: 2.8x2.5mm^2



DCDC25A - efficiency

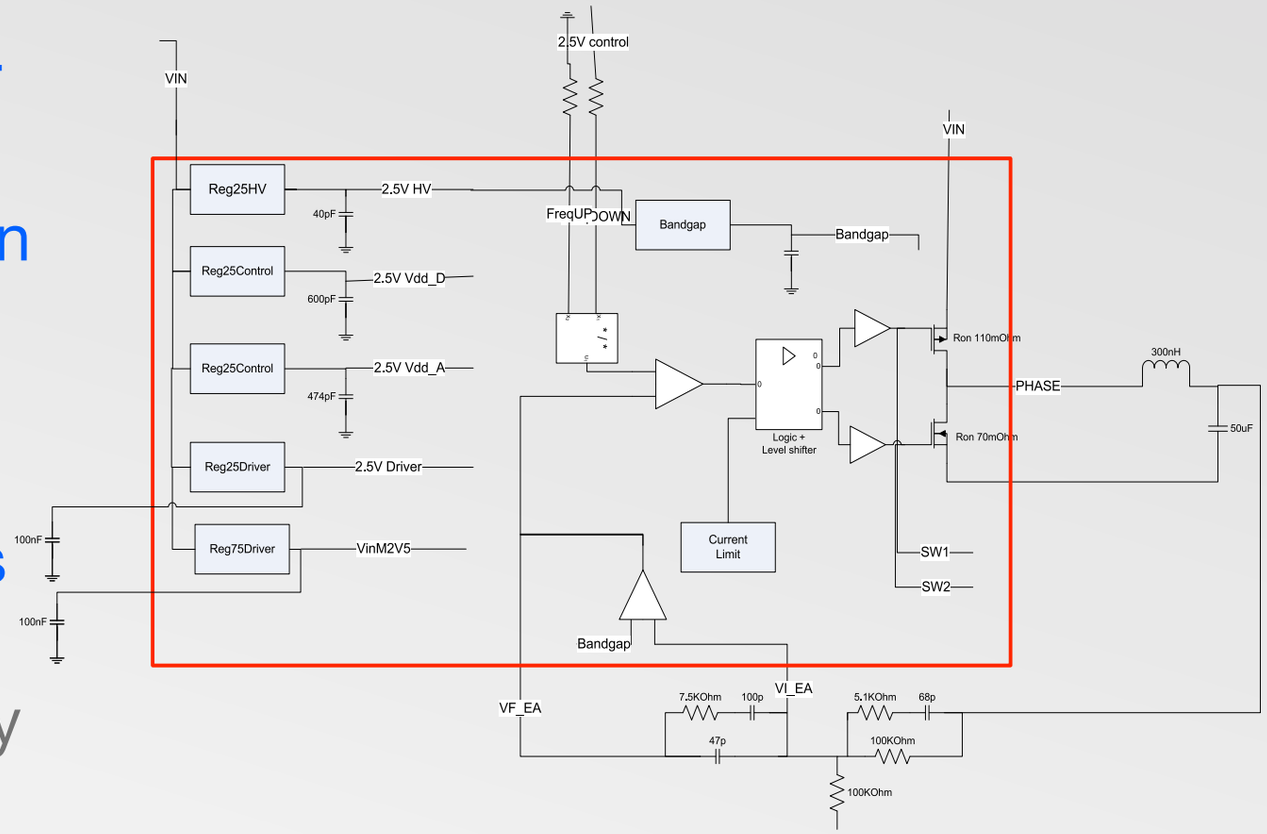
- Measurements taken at constant Vin (10V), Vout (2.5V), Iout (1A)
- Large change of efficiency with L and switching frequency - this changes the peak-peak current and hence the relative losses of conduction, switching and driving
- Peak efficiency at Vout=2.5V and Iout=2A is about 84%
  - impact of packaging technology is not negligible





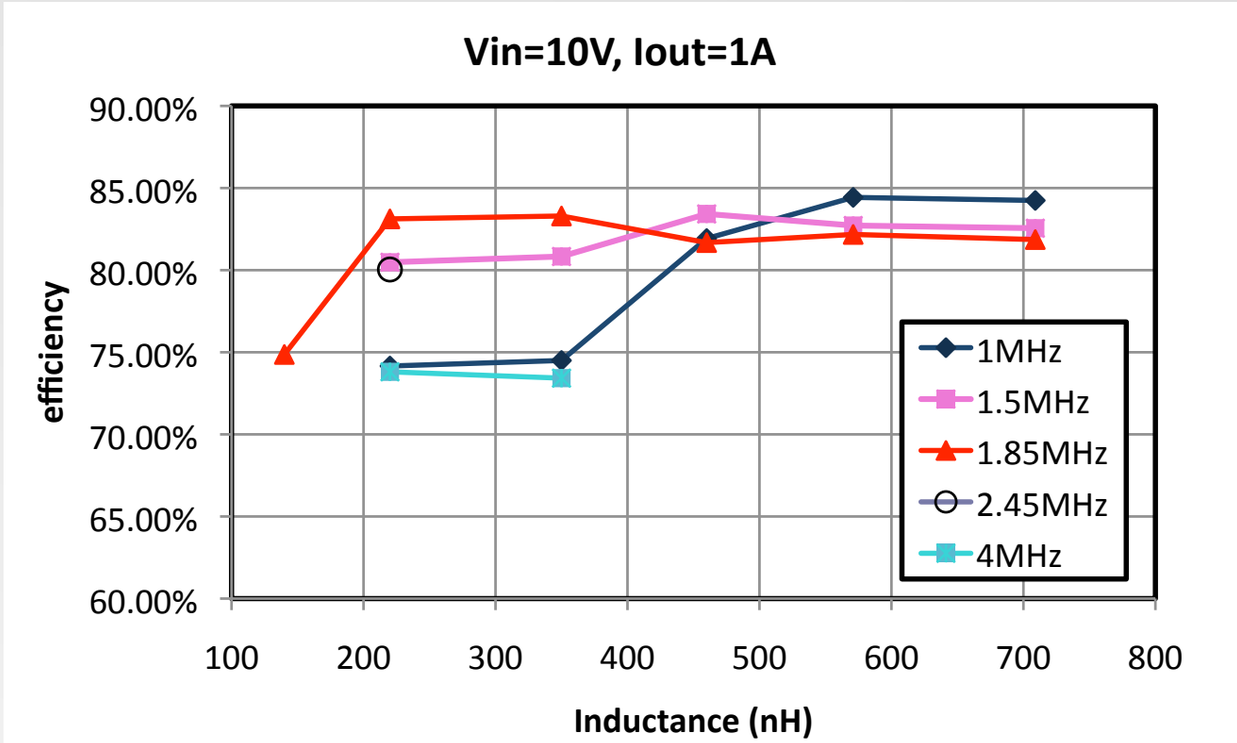
DCDC25B

- 2nd prototype in the 0.25µm technology
- Lateral HV NMOS (low-side) and PMOS (high-side) transistors are used as power switches - Generation 3 transistors
- Isolated Lateral HV NMOS used as well in the circuit
- Internal oscillator fixed at 2MHz, but programmable with external resistor
- Voltage reference and regulated voltages (2.5V, Vin-2.5V) generated on-chip
- Delay between gate signals automatically set (adaptive) in all conditions
- Compensation network off-chip
- Programmable Vout (from R_{bridge})
- Size: 2.8x2.5mm^2



DCDC25B efficiency

- Efficiency measured in the same conditions as for DCDC25A for comparison
  - Efficiency generally higher, notable increase at small values of inductance (in QSW)
  - This improvement is due to higher performance LDMOS, faster switching, and shorter dead times



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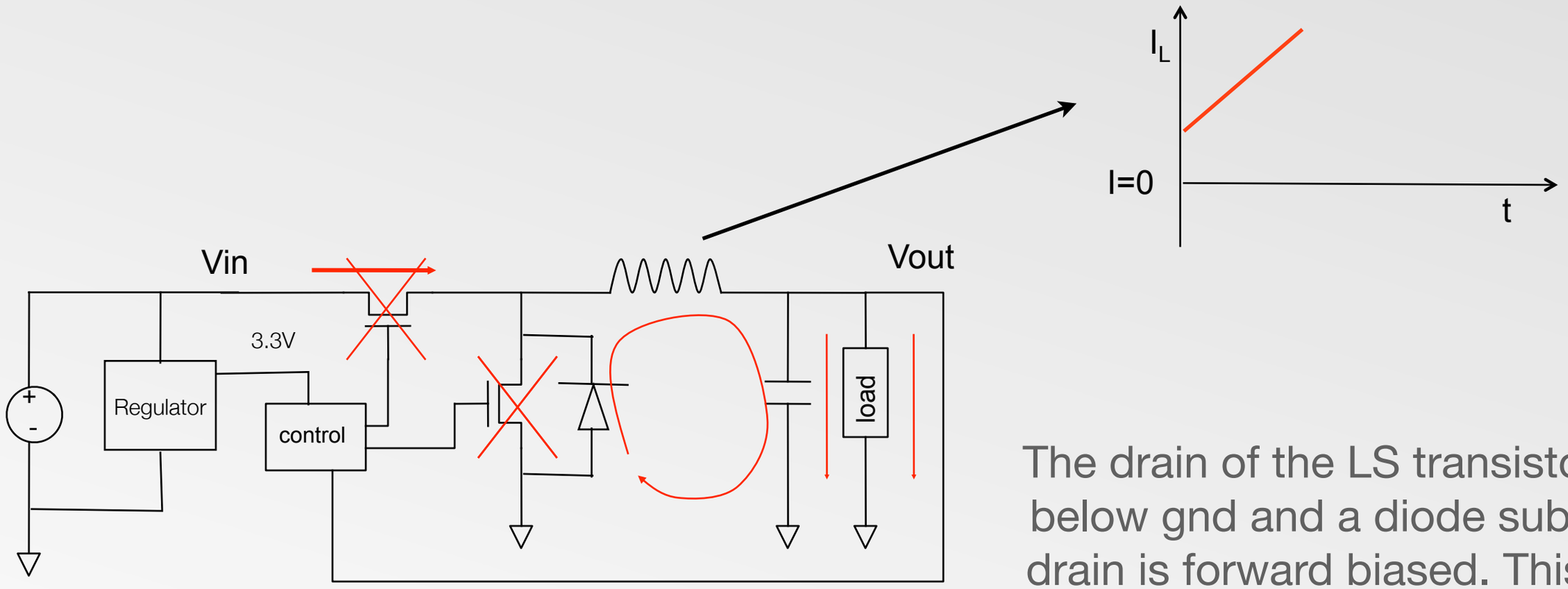
A bad surprise

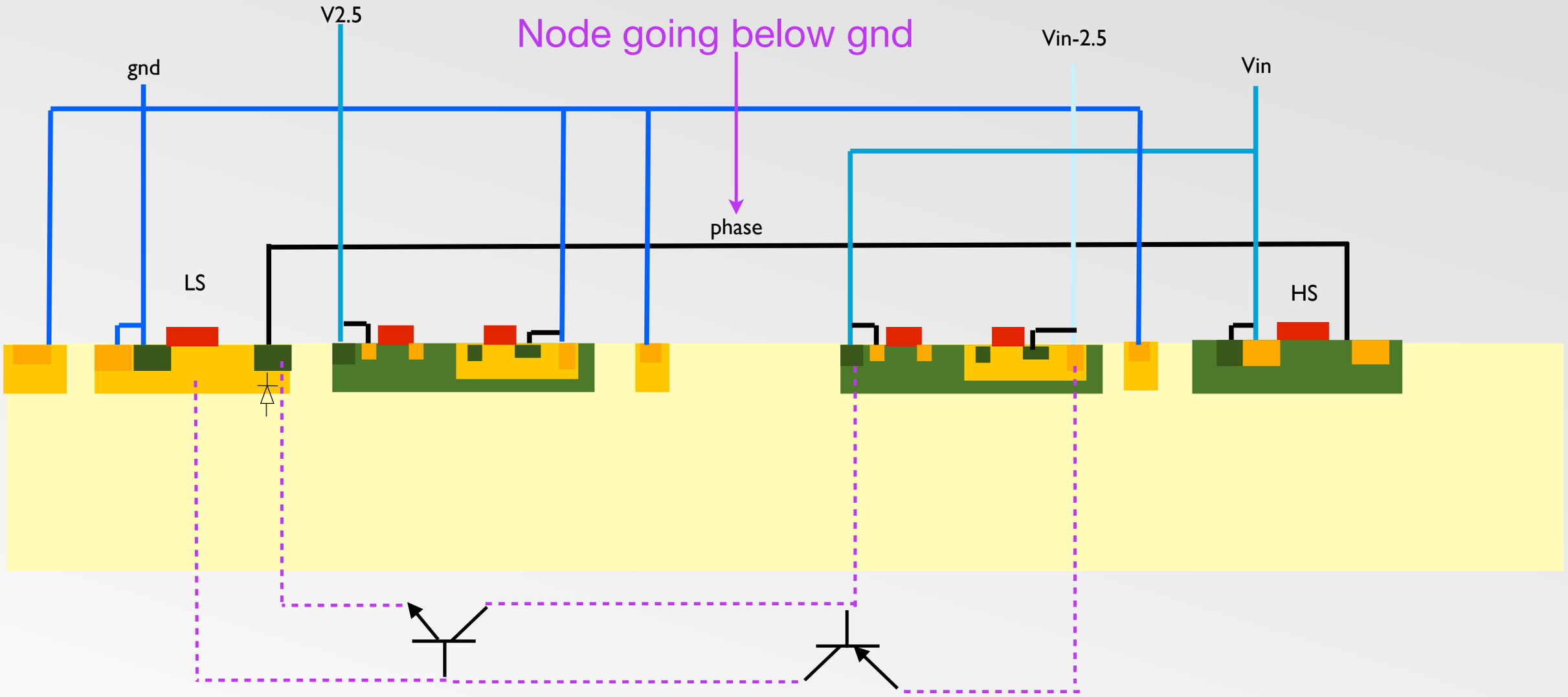
- Although working well at first, DCDC samples destructively failed with no warning when switching conditions were modified (I_{load}, V_{in})
- Failure happened more easily at higher switching frequency
- Circuit features had an impact on the failures:
  - Over-current circuitry contributed to failures, since it was inappropriately detecting over-current events and put the converter in a ‘dangerous’ state
  - Change in load to bring the converter in the transition between QSW and CCM also contributed to failures, since it introduced oscillations in the converter output
- BUT failures happened also with the above features disabled, and sometimes after hours of successful operation....

Specificity of a synchronous buck converter



The drain of the LS transistor goes below gnd and a diode substrate-drain is forward biased. This is the base-emitter part of a bipolar NPN. Similarly, a PNP can turn ‘on’ for the HS transistor (in QSW operation).

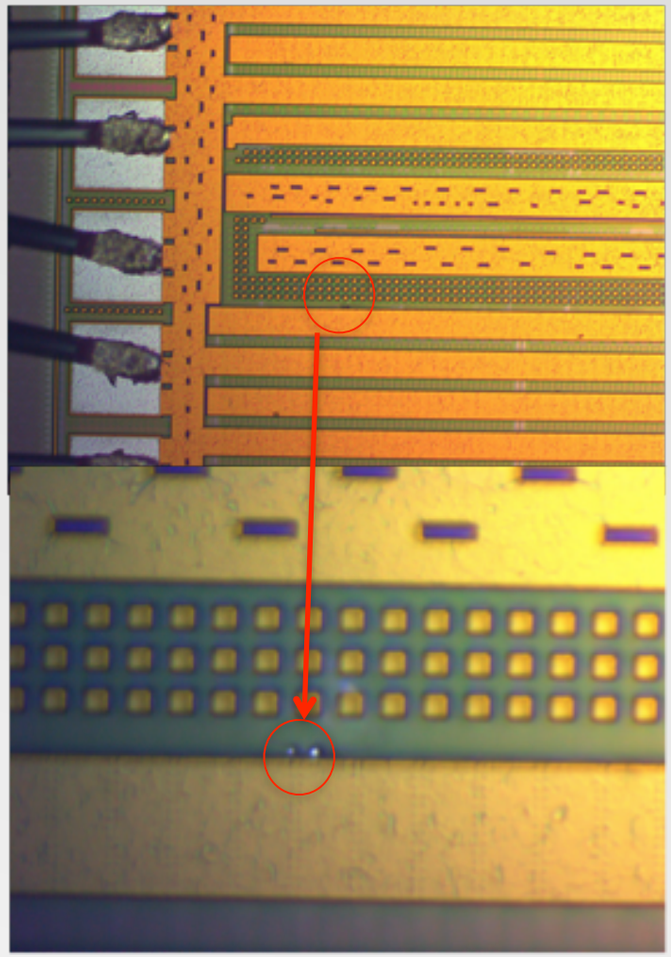
Danger of a forward-biased junction in a synchronous buck



Latch-up is a real threat with large switching currents!

Evidences confirming the latchup

- Visual inspection of damaged samples: location of the ‘signature’ of hot spots
  - in positions with highest R to power source
- Behavior of the regulator (Vin-2.5V)
- Addition of a schottky diode in parallel to the drain-substrate parasitic diode (NLDMOS)
- Observation of consequences of a forced injection of current from the substrate to the drain of the NLDMOS
- Measurement in test structures of the collection of charge at neighbor n-diffusion pockets, after injection of charge in a forward-biased n-substrate junction
- **Techniques to protect agains latchup problems in synchronous converters exist**
  - their need and effectiveness have to be specifically evaluated in each technology



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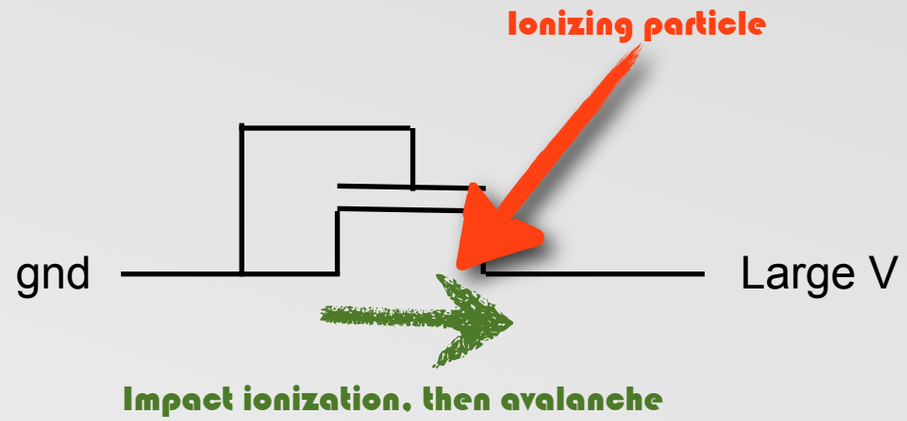
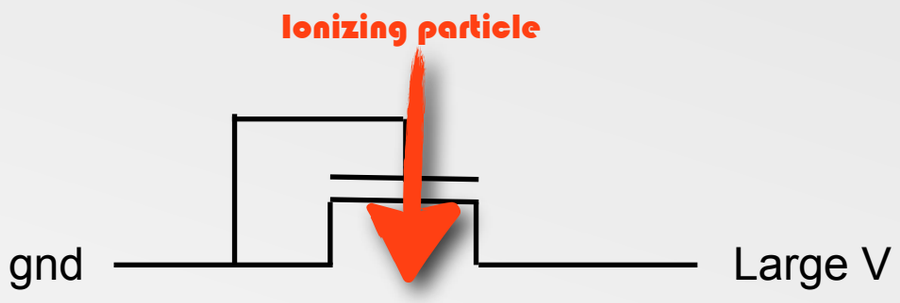
Other threatening radiation effects: SEB and SEGR

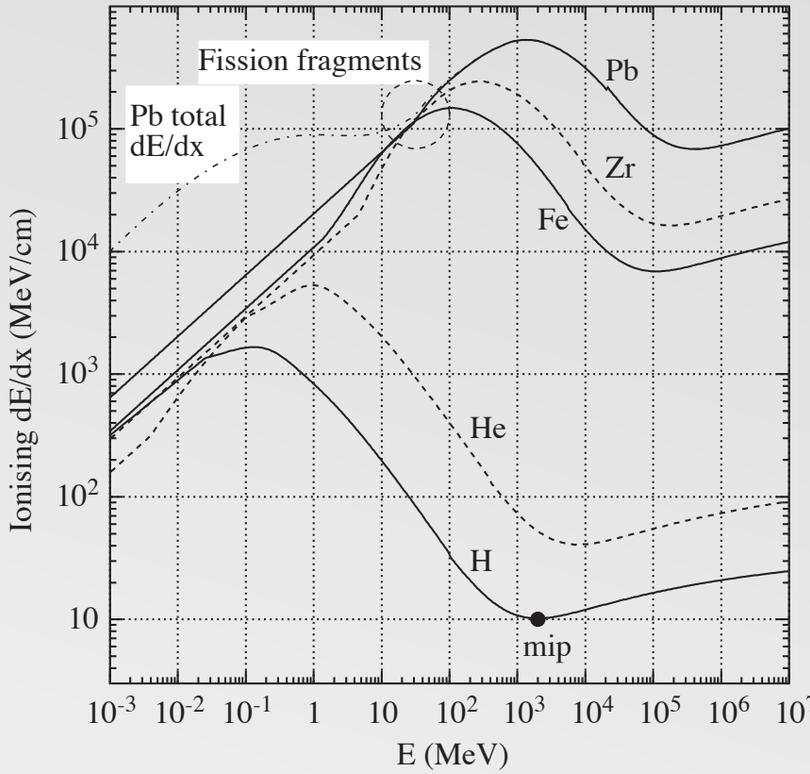
- These Single Event Effects can lead to catastrophic failure of power devices
  - SEB happens as a consequence of a particle strike when the power transistor is off (at high V_{ds}), and is due to avalanche multiplication of carriers in the high field region
  - SEGR appears as a gate current increase that can lead to device failure (gate breakdown)





Testing for SEB and SEGR

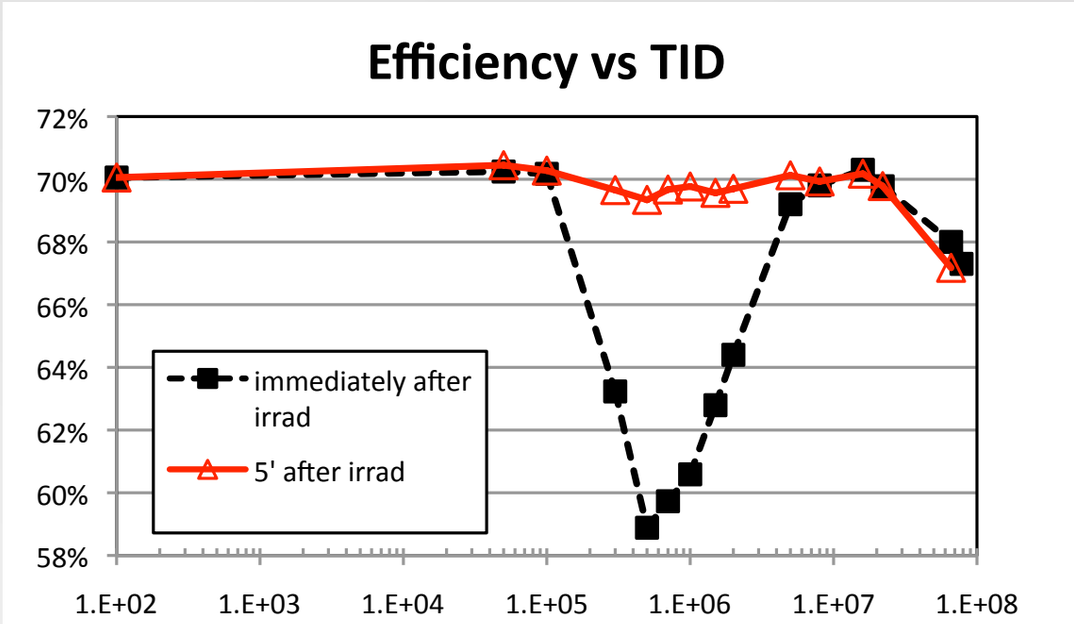
- Although they can happen in a hadron radiation environment, testing with proton beams is not adequate to confidently exclude their occurrence in the real application (statistical problem)
- Heavy ion beams, where the energy deposition by each particle is known, are a much better tool
  - Need for the choice of appropriate HI LET and penetration
- Tests were performed at CRC (Louvain-la-Neuve, Be) using their high-penetration HI cocktail (min. range 80µm) up to the maximum LET of 31 $MeVcm^2mg^{-1}$



Simulated ionizing energy loss of fragments in $PbWO_4$ (after M.Huhtinen et al, NIM A 545 (2005) 63-87).
In Si, the dE/dx is approximately 40% of the one in this plot.
Fe and Zr are fission fragments from W, and could possibly be generated by interaction of hadrons with the W in a Si integrated circuit (extremely rare event, also because of the small amount of W).
In Si, this would lead to a maximum LET of about 43 $MeVcm^2mg^{-1}$ - but these fragments would have very short range

Radiation tolerance - DCDC25A and B

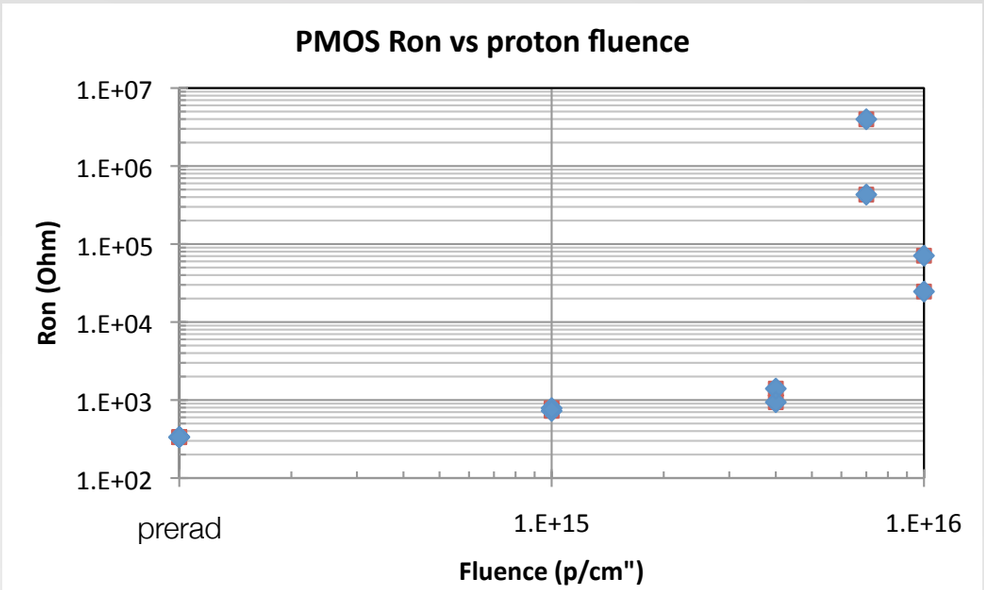
- Only a few working samples available for DCDC25A, and hermetically packaged: no radiation test done
  - LDMOS used in DCDC25A have been individually tested for TID and displacement damage, and were OK
- For DCDC25B, radiation test were mandatory because of the use of ‘new’ Generation3 LDMOS transistors (N, P, and isolated N)
  - These transistors had not been measured for radiation effects before
- TID irradiation was performed with X-rays - difficult because it required the DCDC to reliably work for several days (latchup problem...). The converter was switching at 1.5MHz, regulating 2.5V (0.5A) at the output from 10V input

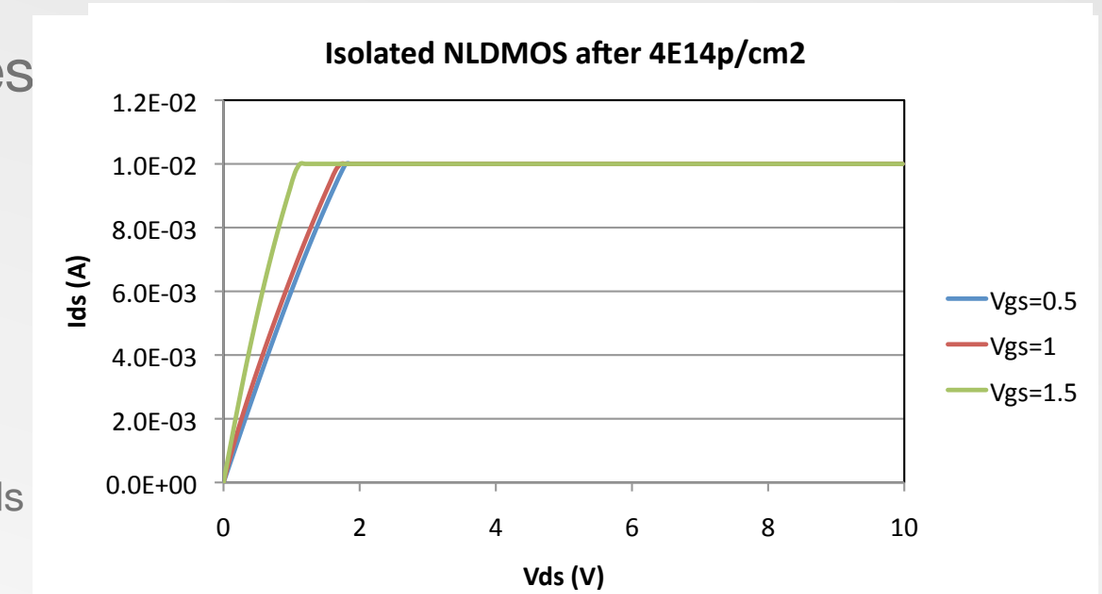


TID result for a DCDC25B sample, up to 78Mrad (1.5MHz, 220nH, I_{out}=0.5A). After that, latchup-induced failure occurred. Another sample was functional up to 171Mrad before failure. Efficiency is low since the beginning in the chosen test conditions, which were taylored at decreasing the probability of latchup to occur (without much success...)

Proton irradiation of DCDC25B

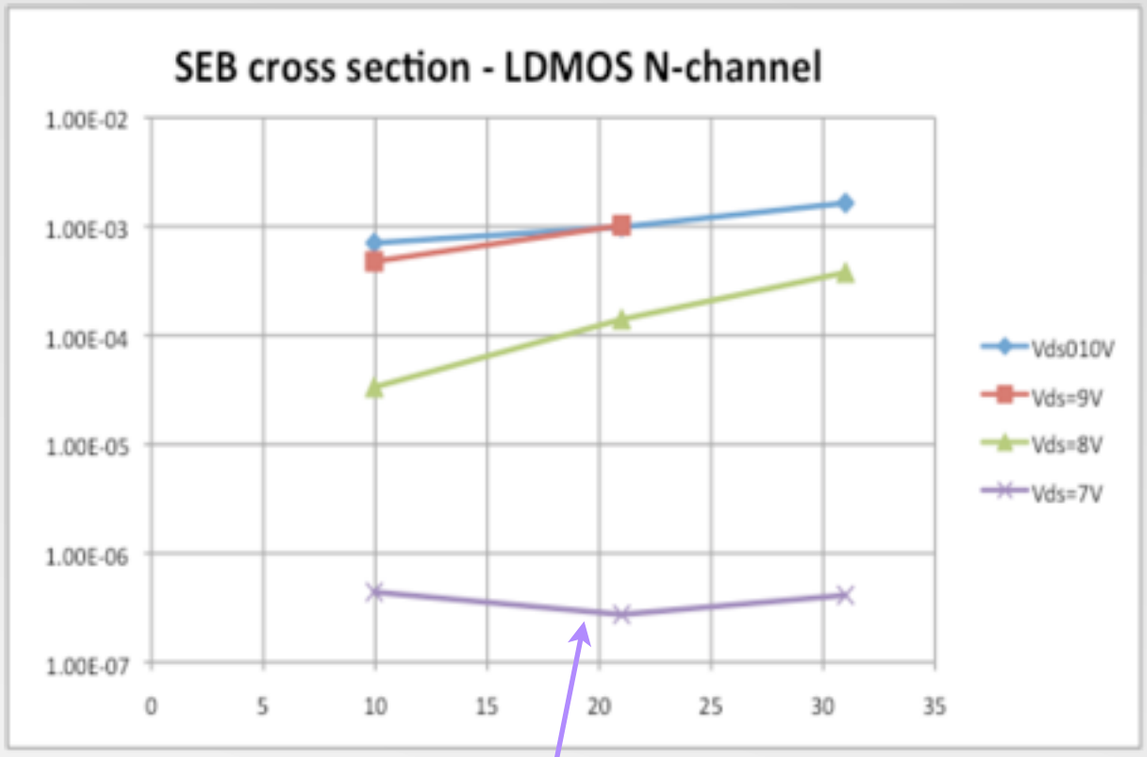
- Proton irradiation performed at CERN IRRAD1 facility (24GeV/c), on unbiased samples
  - 5 samples irradiated at fluences of 1, 4, 7 and 10 10^{15} p/cm^2
- None of the samples was working after irradiation - already the on-chip pre-regulator was not providing the correct voltage
- Measurement of test LDMOS transistors (of the same Generation3, in the SEBchip test structures confirmed that these transistors are heavily damaged by protons, in particular:
  - PLDMOS: very large increase of Ron and decrease of current capability
  - INLDMOS: their capability of holding large V_{ds} compromised





SEB and SEGR test results (0.25µm generation3)

- SEB (measurements on individual transistors)
  - A large number of SEB events has been observed for N LDMOS
    - Protection network prevents permanent damage of the transistors and allows for computation of the cross-section (sigma)
    - Sensitivity observed for V_{ds} as low as 8V and for Heavy Ion LET as low as 10 $MeVcm^2mg^{-1}$
  - No event observed for PMOS during the full test (up to 13V)
- SEGR
  - No measurable increase of the gate current during irradiation or PIGS



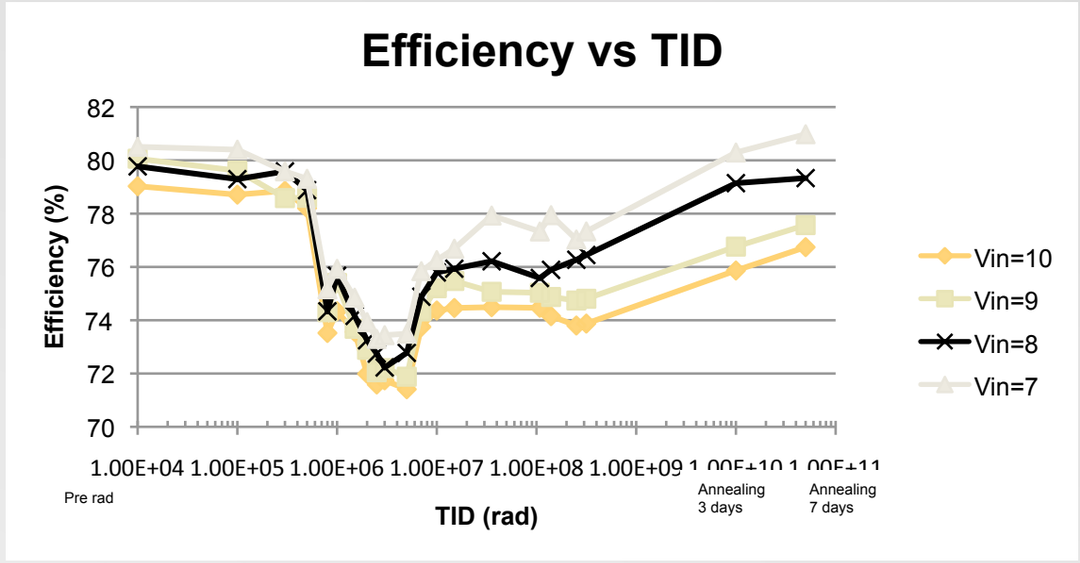
Limit cross-section, no SEB observed

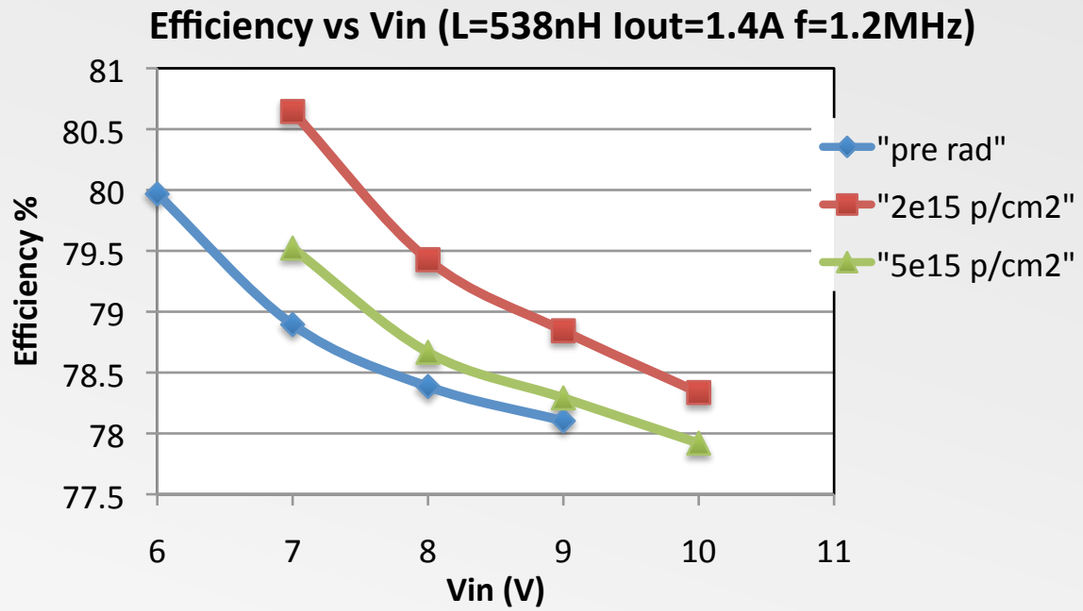
Conclusion on DCDC25B

- With respect to the former prototype DCDC25A, the differences that led to relevant consequences were:
  - The change of N and P LDMOS to the ‘new’ Generation3 transistors
  - The use of Isolated NLDMOS transistors
  - The integration of the on-chip regulators and duplication of the buffers driving the switches (all other layouts that might contribute to the observed problems remained unchanged)
- As a result, the converter suffers destructive failures due to latchup and is not tolerant to the required level of displacement damage
- Moreover, NLDMOS transistors suffer SEB potentially leading to catastrophic failure in the DCDC (we ignore whether this would be an issue for Generation2 transistors)
- Further design of a full DCDC converter in the 0.25µm technology has to wait until an appropriate set of LDMOS transistors has been qualified and brought to a sufficient level of maturity

Radiation effects - DCDC35B

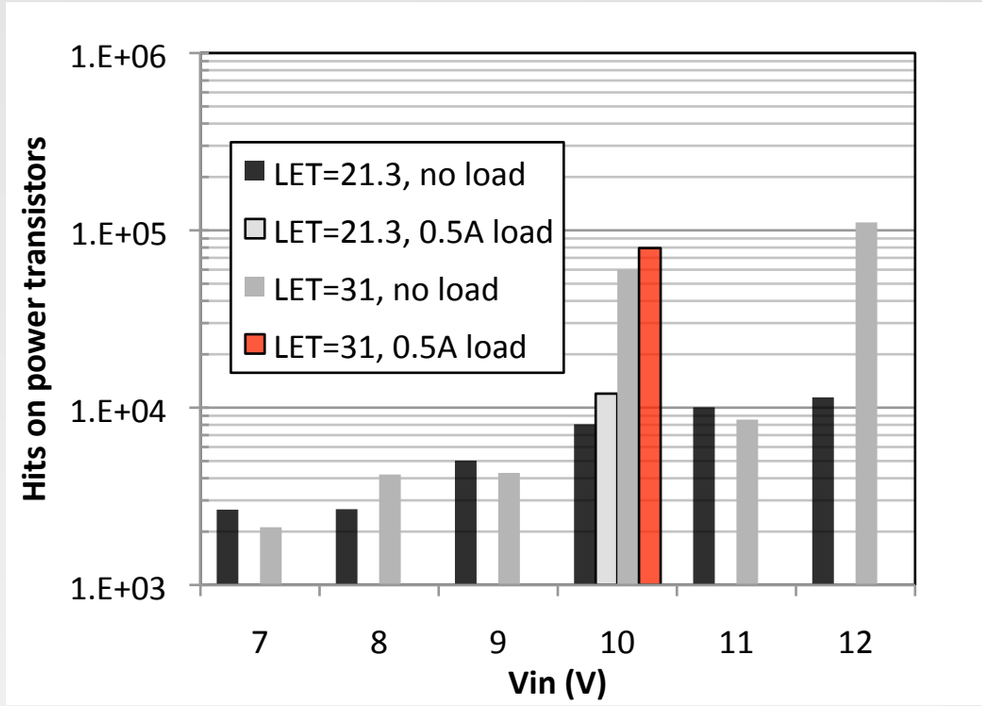
- While the main emphasis was on the design of ASICs in 0.25µm, radiation tests have been made ‘in the background’ on the DCDC35B prototype
  - TID at high dose rate (~3Mrad/hour) induce increase of leakage current, leading to efficiency losses. This will be much less relevant at the low dose rate of the real application
    - proton irradiation does not influence the converter’s performance
- These results indicated that the 0.35µm ‘backup’ technology could be an adequate substrate for the converter’s design - but SEE test needed to be run to uncover possible sensitivity to SEB





SEB test of DCDC35B

- HI irradiation test performed 2 weeks ago at CRC (Louvain-la-Neuve), again with their high penetration cocktail
- Measurements done on both:
  - Individual NLDMOS transistor with protection resistor in series (and external comparator)
  - Full switching DCDC35B converter (increasing V_{in} from 6 to 12V, V_{out}=2.5V, f=1MHz, L=500nH, without load or with 0.5A load in some conditions). 2 samples exposed.
- No SEB observed in any of the tests with LET of 21 or 31 MeVcm^{2}mg^{-1}, up to a maximum V_{ds} of 12V
- The 0.35µm technology is fully radiation qualified and adequate for the integration of a DCDC converter



Conclusion

- Three prototype DCDC converter ASICs, with increasing complexity, have been produced and tested
  - The chosen circuit solutions have been verified and improved leading to higher efficiencies and getting closer to a final complete design (with all protection features)
  - The design methodology has been improved with the addition of a behavioral simulation approach considerably shortening simulation time (and allowing study of system stability)
- With the introduction of ‘new’ LDMOS transistors, and of increased on-chip functionality (regulators), the most recent prototype in the 0.25µm technology has problems incompatible with a final reliable and radiation-tolerant design
  - Further developments in this technology have to wait the qualification and maturity of a set of LDMOS transistors
- Meanwhile, the successful full radiation qualification of the DCDC35B DCDC in the 0.35µm technology indicates a safe path for the rapid development of a radiation-tolerant converter