High speed data transfer with FPGAs and QSFP+ modules

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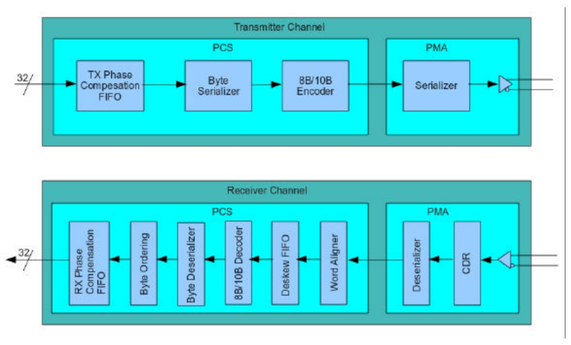
ABSTRACT –We present test results and characterization of a data transmission system based on a last generation FPGA and a commercial QSFP+ module. QSFP+ standard defines a hot-pluggable transceiver available in copper or optical cable assemblies for an aggregated bandwidth of up to 40 Gbps. We implemented a complete testbench based on a commercial development card mounting an Altera Stratix IV FPGA with 24 serdes at 8.5 Gbps, together with a custom mezzanine hosting three QSFP+ modules. We present test results and signal integrity measurements up to 12 Gbps.

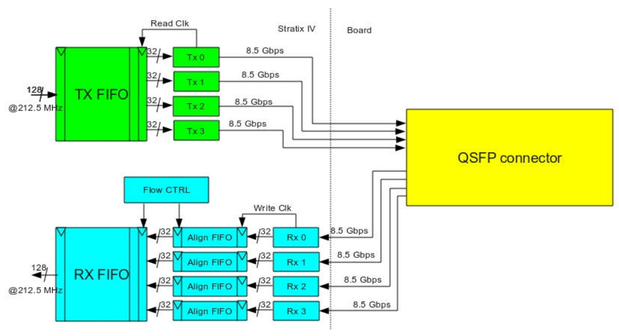
High speed serializer/deserializer

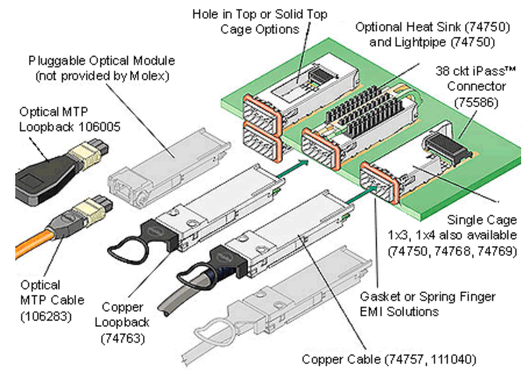
- Stratix IV GX embedded Altera transceivers
- Full duplex ser/des
- Data rates from 600 Mbps to 8.5 Gbps
- Single or dual data rate
- 8b/10b enconding with clock data recovery
- Channel bonding (up to 8x)
- Programmable pre-emphasys and equalization



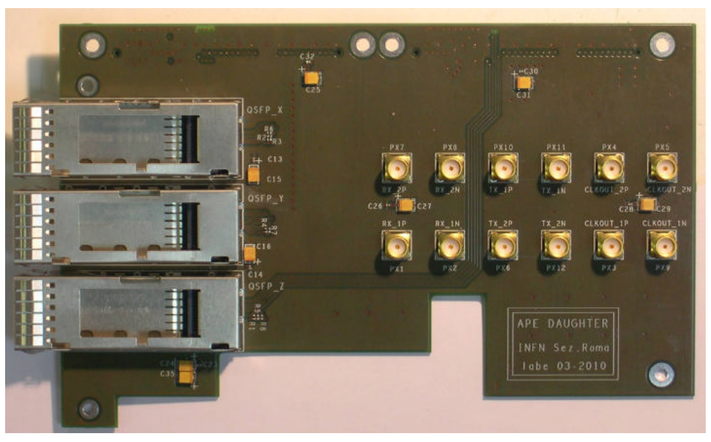
QSFP+ standard

- SFP+ (Small Form Pluggable) electrical and mechanical standard for point-to-point links over copper or optical fibers with data rate up to 10 Gbps
- QSFP+ (Quad SFP+) hot-pluggable transceiver with 4 transmit and 4 receive channels
- Aggregated bandwidth up to 40 Gbps per direction
- High speed data rate, high-density and low-power applications
- Passive copper (< 5m), active copper (< 15m) and active optical (< 100m) modules available on the market
- 100 Ohm AC coupled CML differential lines



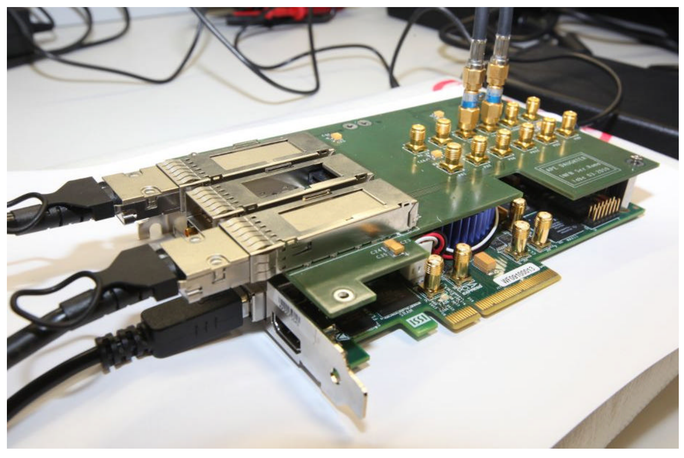


Test system



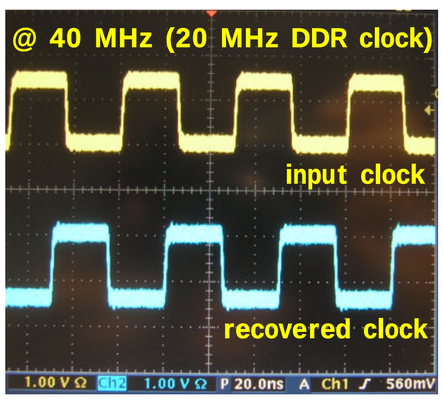
- Altera Stratix IV GX 230 development kit
- 230k Logic Elements, 24 serializers / deserializers
- PCI-Express gen 2

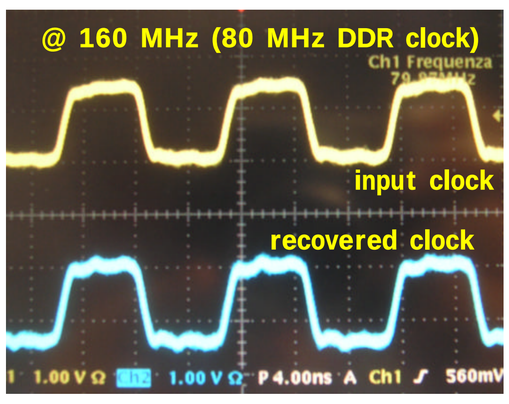
- Custom mezzanine (designed at LABE INFN Roma)
- 3 QSFP+ connectors
- 2 high-speed Samtec connectors
- SMA test connectors



Recovered clock

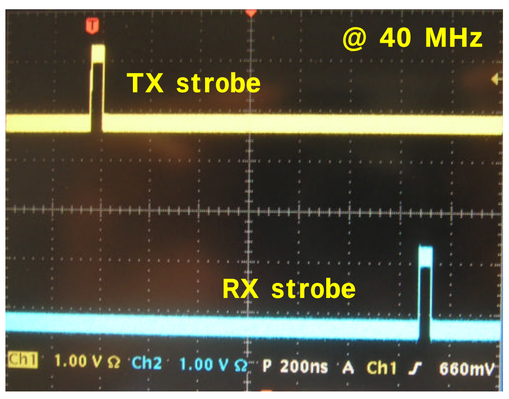
- Recovered clock stable and in phase up to 400 MHz (200 MHz DDR clock)

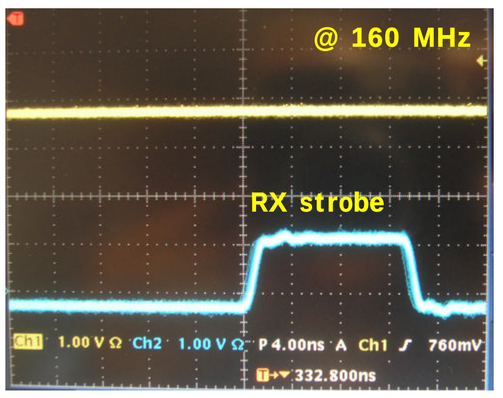




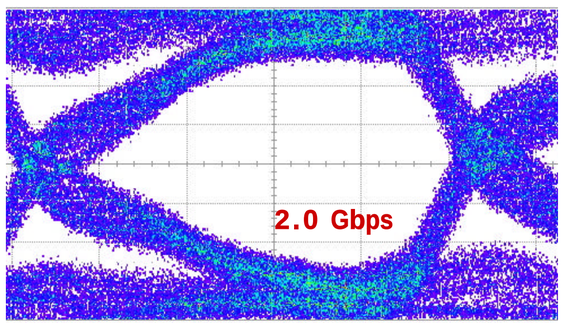
Latency

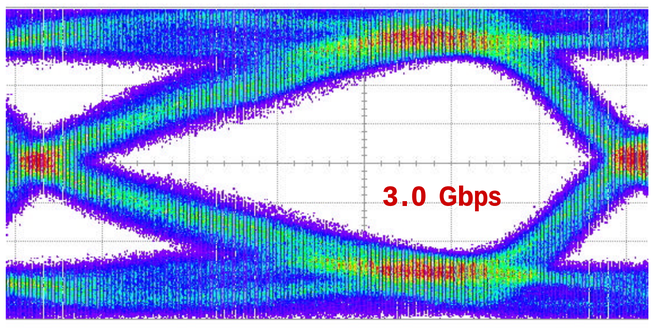
- Pseudorandom data stream
- Output strobe on a specific data word





Signal integrity





- 20 GHz sampling scope with external clock data recovery
- 2^{32} pseudorandom data stream
- Eye diagram at 2 and 3 Gbps (without pre-emphasys)
- Above 3 Gbps pre-emphasys needed (work ongoing!)

Conclusions

- High speed embedded serdes mature and reliable technology with single line data rate up to 8.5 Gbps
- QSFP+ emerging standard for high-density, low power applications high-data rate applications
- Successfully tested up to 12 Gbps aggregated bandwidth

References

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