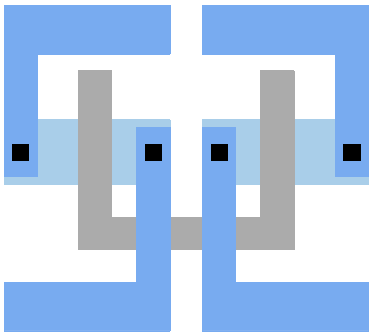
UNIVERSITÄT
HEIDELBERG

DCDB - A 256 Channel 8-Bit Current Digitizer ASIC for the Belle-II PXD



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TWEPP 2010, Aachen

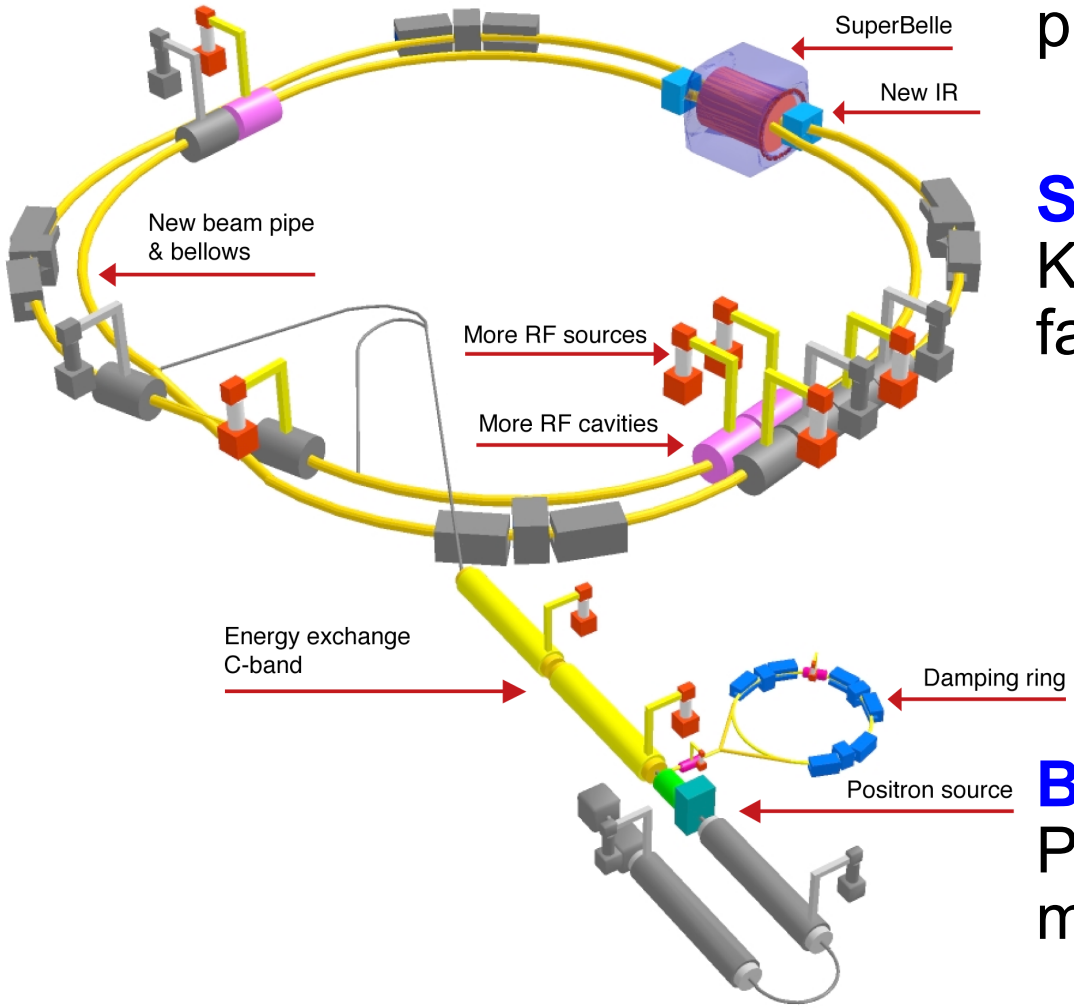
22.09.2010

Outline

- The Belle-II Experiment
- DEPFET as Pixel Detector for the Belle-II Experiment
- Introduction: DEPFET Current Digitizer for Belle-II (DCDB)
- DCDB Test Setup
- Measurement Results

The Belle-II Experiment

The Belle-II Experiment at KEK (Japan)



KEK:
Japan's leading high energy physics laboratory

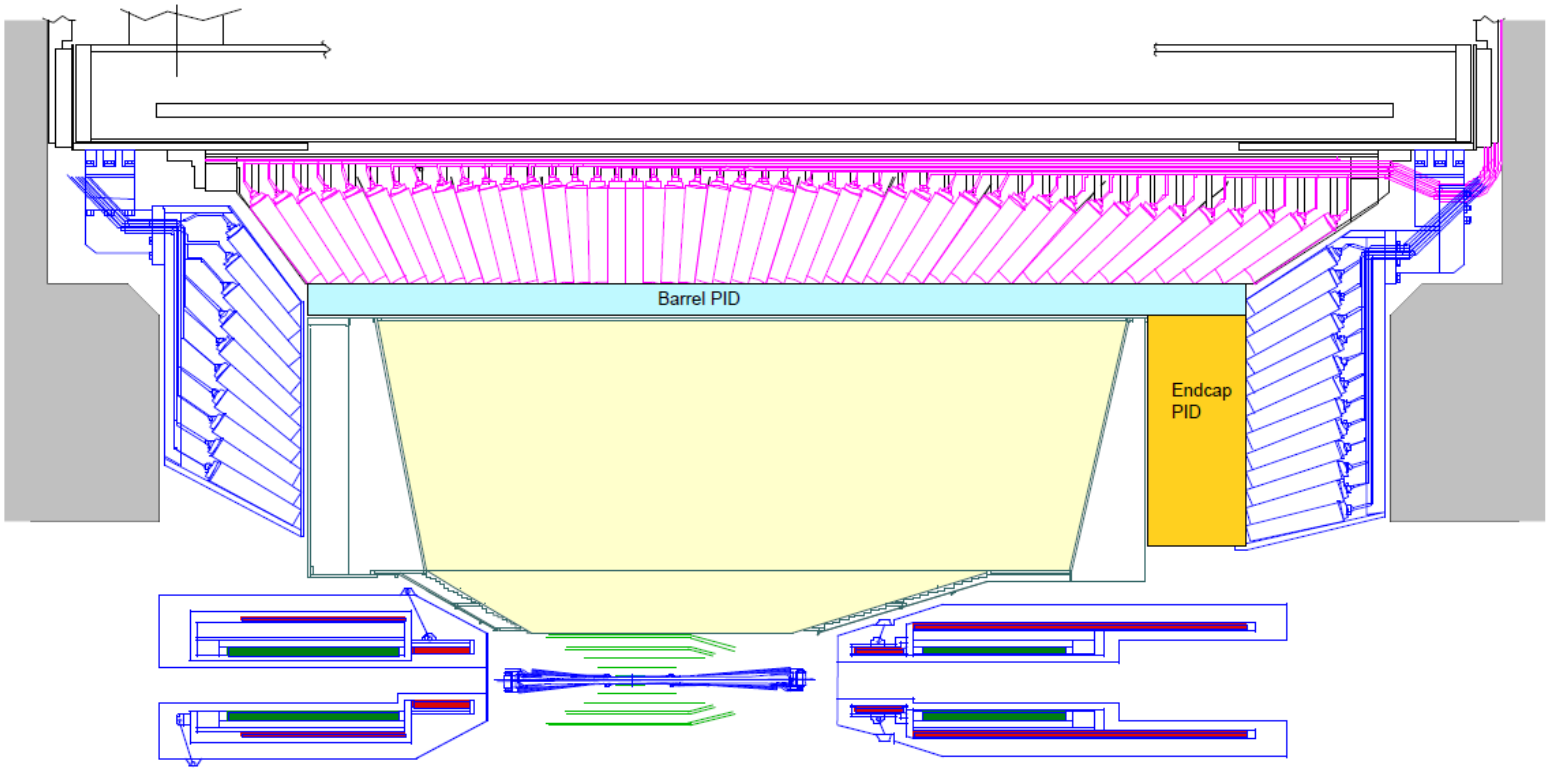
SuperKEKB:
KEK's next generation B-meson factory

- Asymmetric electron/positron collider (3.5 GeV, 8 GeV)
- Luminosity up to $8 * 10^{35} 1/s \cdot cm^2$
- Nano beam design: 3,7 / 2,1 A

Belle-II (aka SuperBelle):
Particle detector at the SuperKEKB machine

- Study CP violation via $B_0 / \overline{B_0}$ decays

Detector Upgrades: From Belle to Belle-II



Challenges:

- Higher Background (x20): radiation damage, occupancy
- Higher event rate (x50): higher trigger rate, DAQ, computing

Silicon vertex detector upgrade:

- Belle: 4 layers of Strip Detector
- Belle-II: 2 layers of Pixel Detector plus 4 layers of Strip Detector

Various upgrades for all sub-detectors:

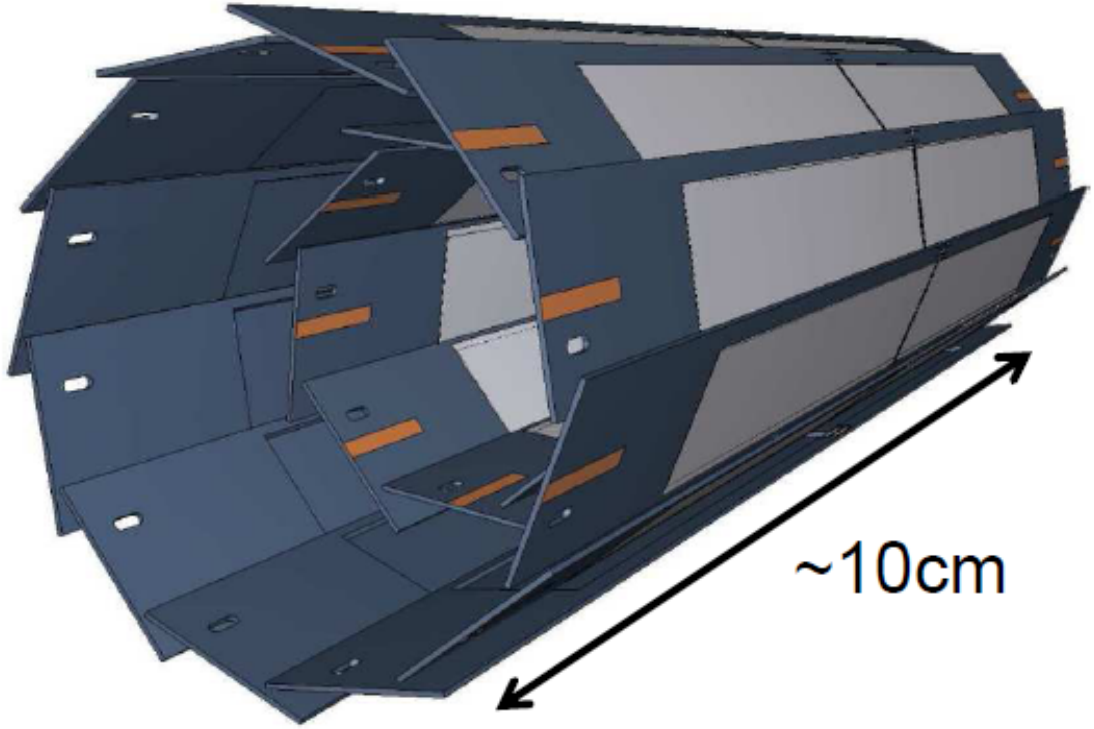
- Vertex resolution
- Rate capability
- Particle identification

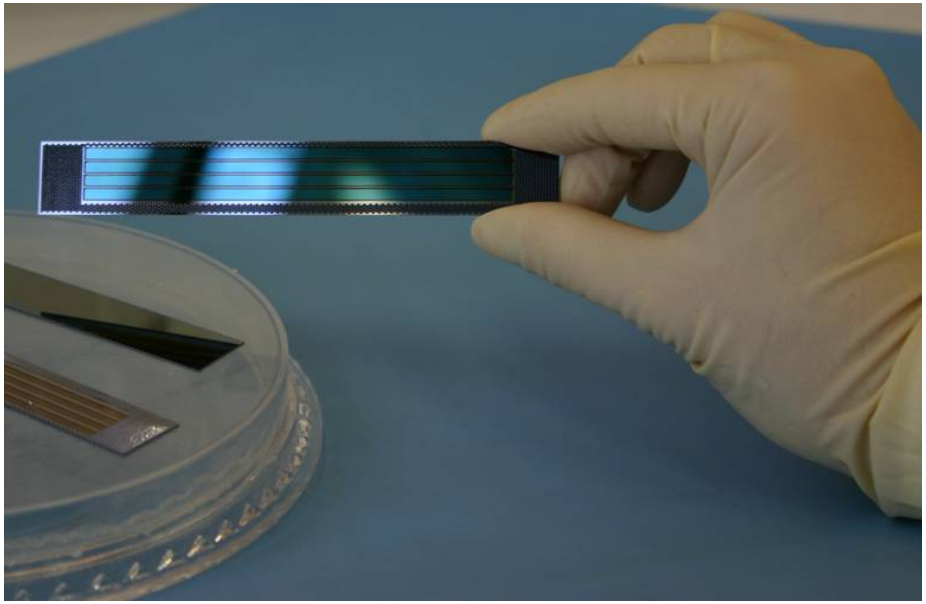
DEPFET as Pixel Detector for the Belle-II Experiment

The DEPFET Collaboration

- University of Barcelona
- CNM, Barcelona
- Ramon Llull University
- Bonn University
- Heidelberg University
- Göttingen University
- Karlsruhe University
- IFJ PAN, Krakow
- MPI Munich
- Charles University, Prague
- TU Munich
- IFIC,CSIC-UVEG, Valencia
- University of Giessen
- LMU Munich
- University of Santiago de Compostela

The DEPFET Pixel Detector for Belle-II



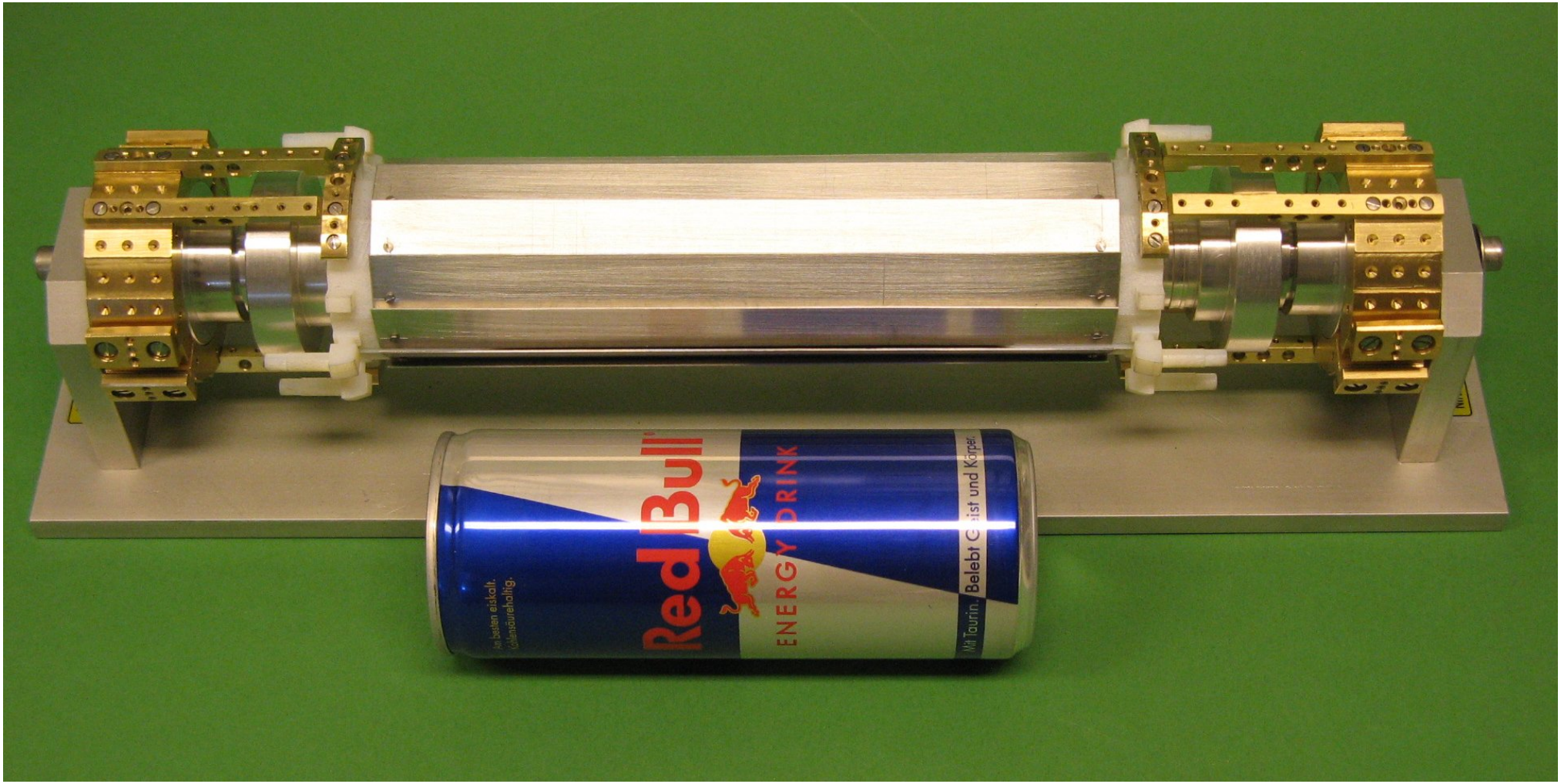


2 layers @ **r=1.4cm** and **r=2.2cm**

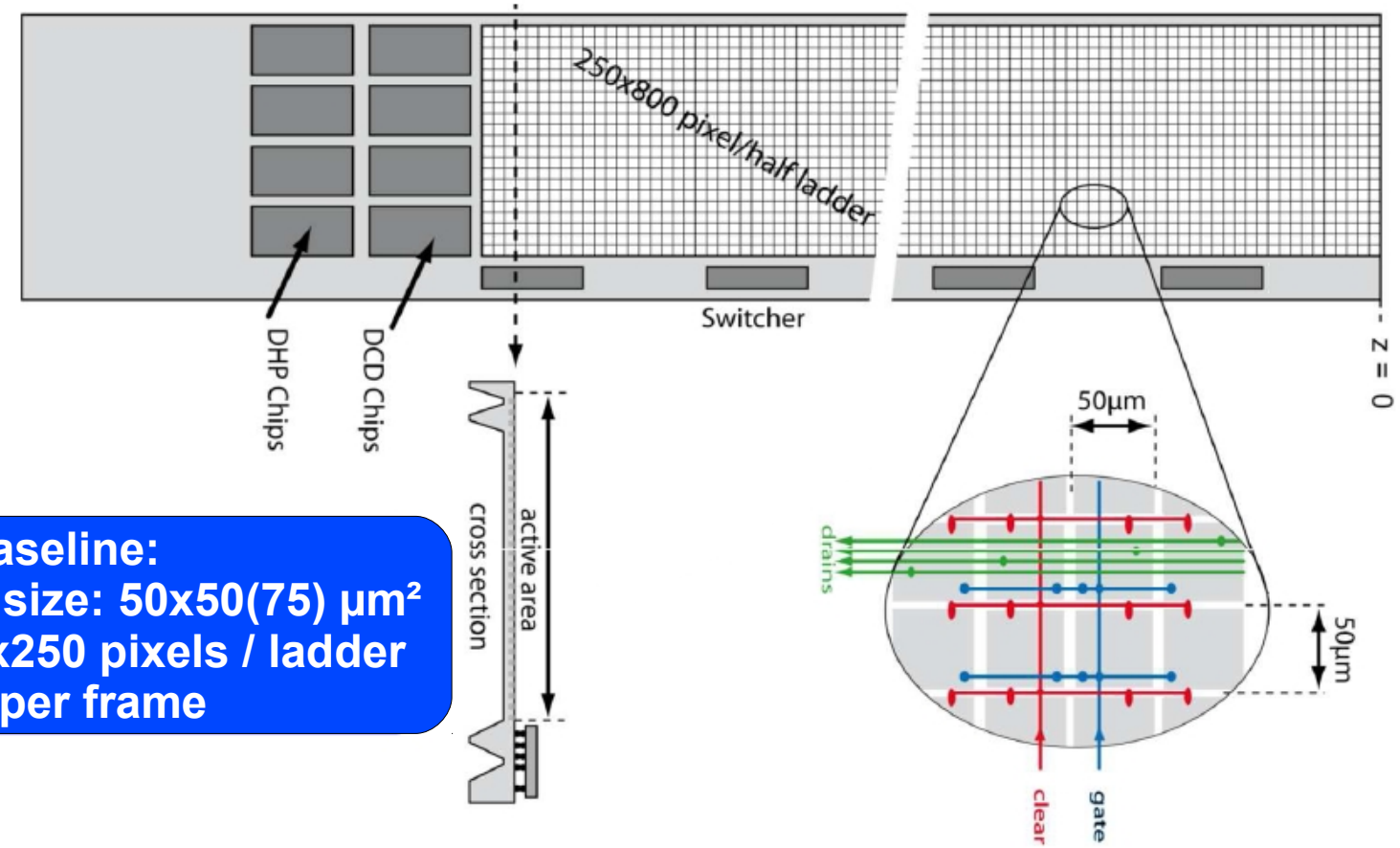
All-silicon modules

Self-supporting structure

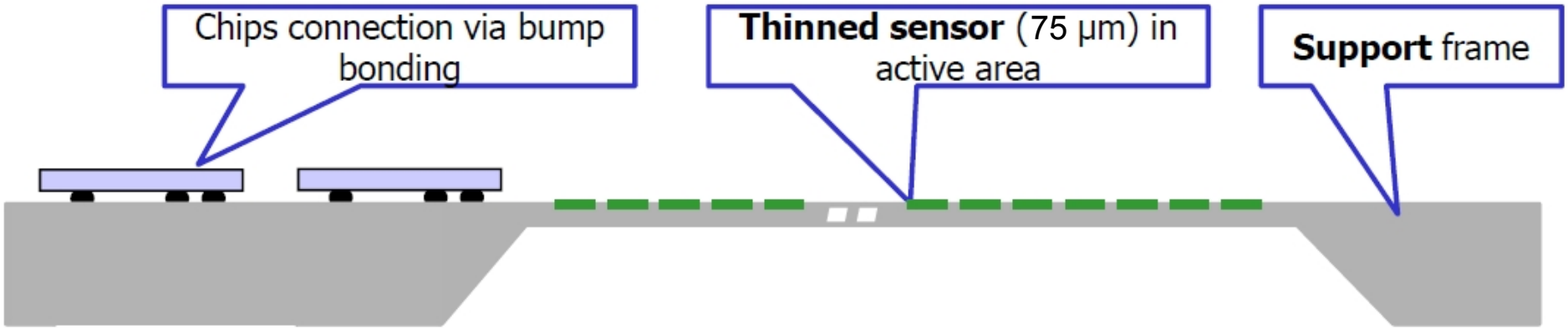
DEPFET Assembly Model



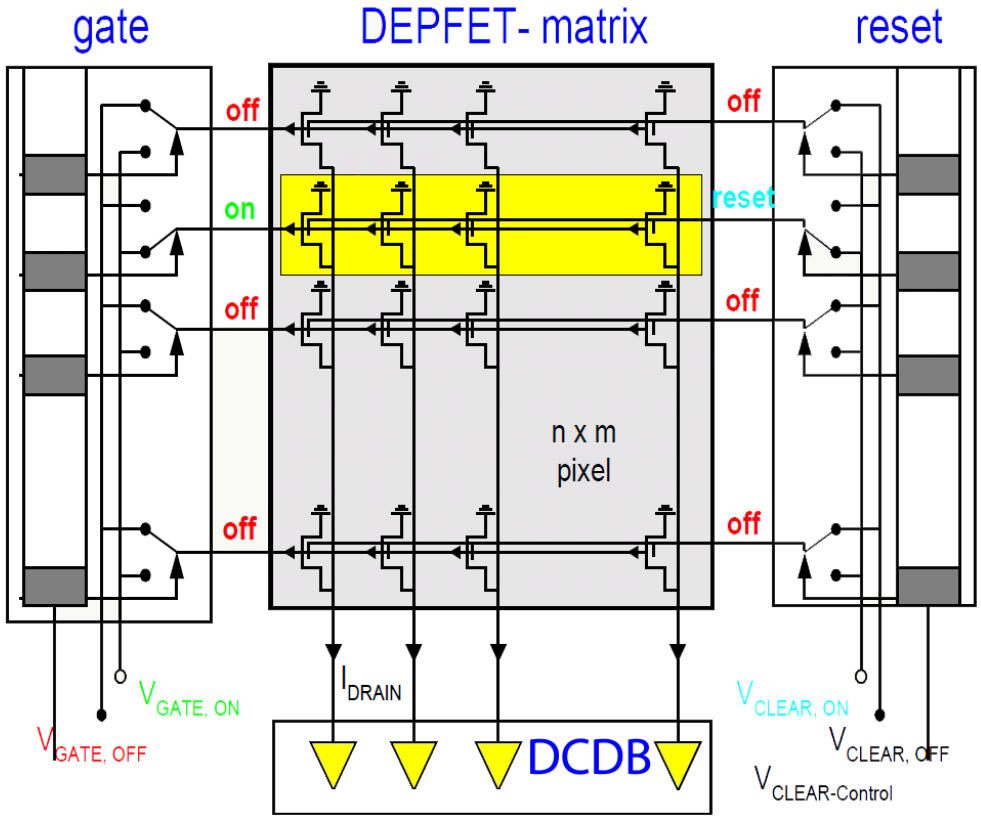
The DEPFET Detector Ladder



Belle-II Baseline:
Pixel size: 50x50(75) µm²
1600x250 pixels / ladder
20µs per frame



DPEFET Detector Readout Scheme



Rolling shutter readout mode:

- Steering chips select row by row
- DCDB digitizes selected pixels in parallel
- 20µs readout time for entire frame

Requirements:

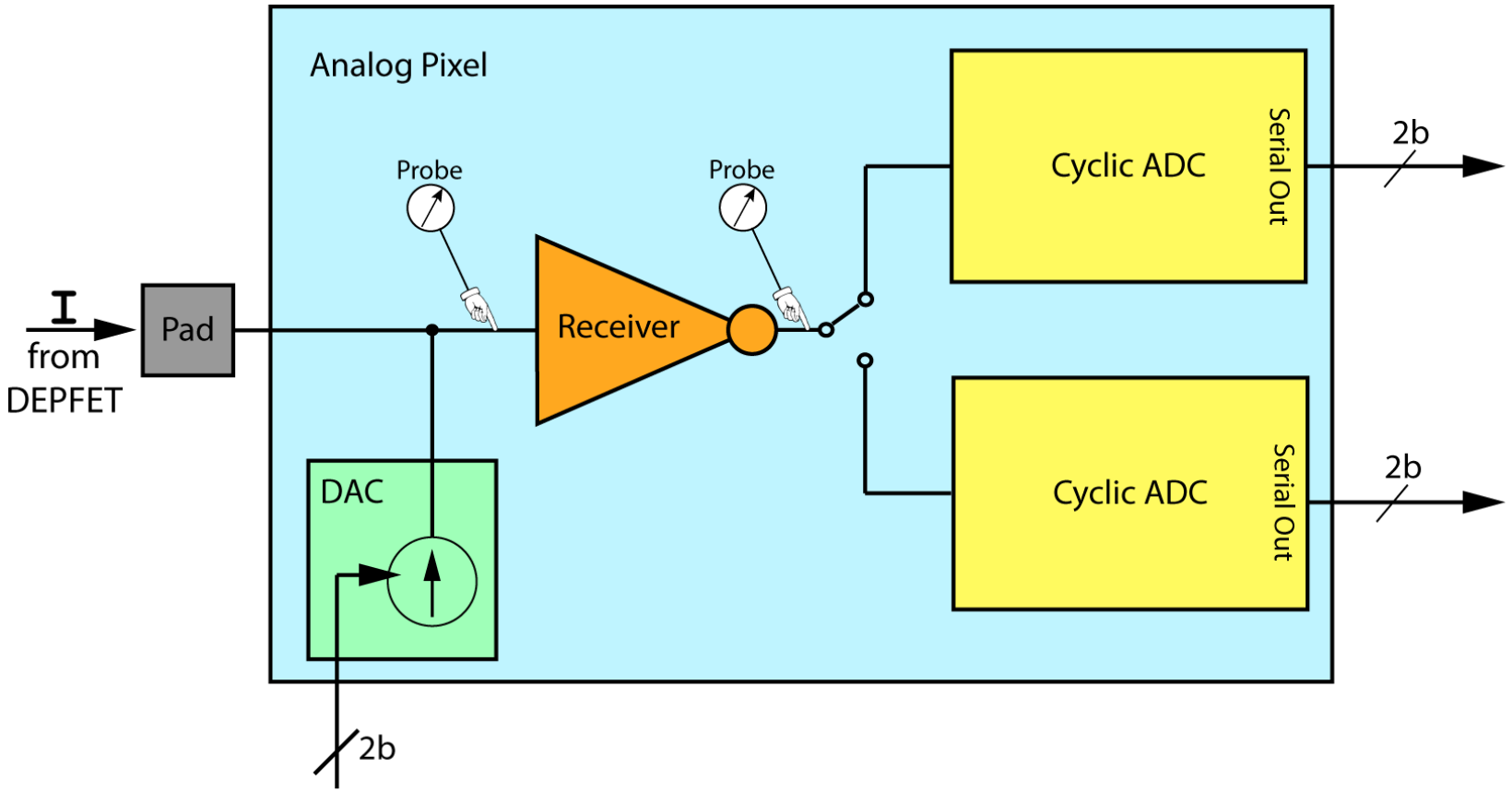
MIP hitting 75µm thin Si → ~6000 electron-hole-pairs

DEPFET gain: 500pA/e → ~3µA signal per MIP

S/N target of 10-20 → **Noise target < 150-300nA**

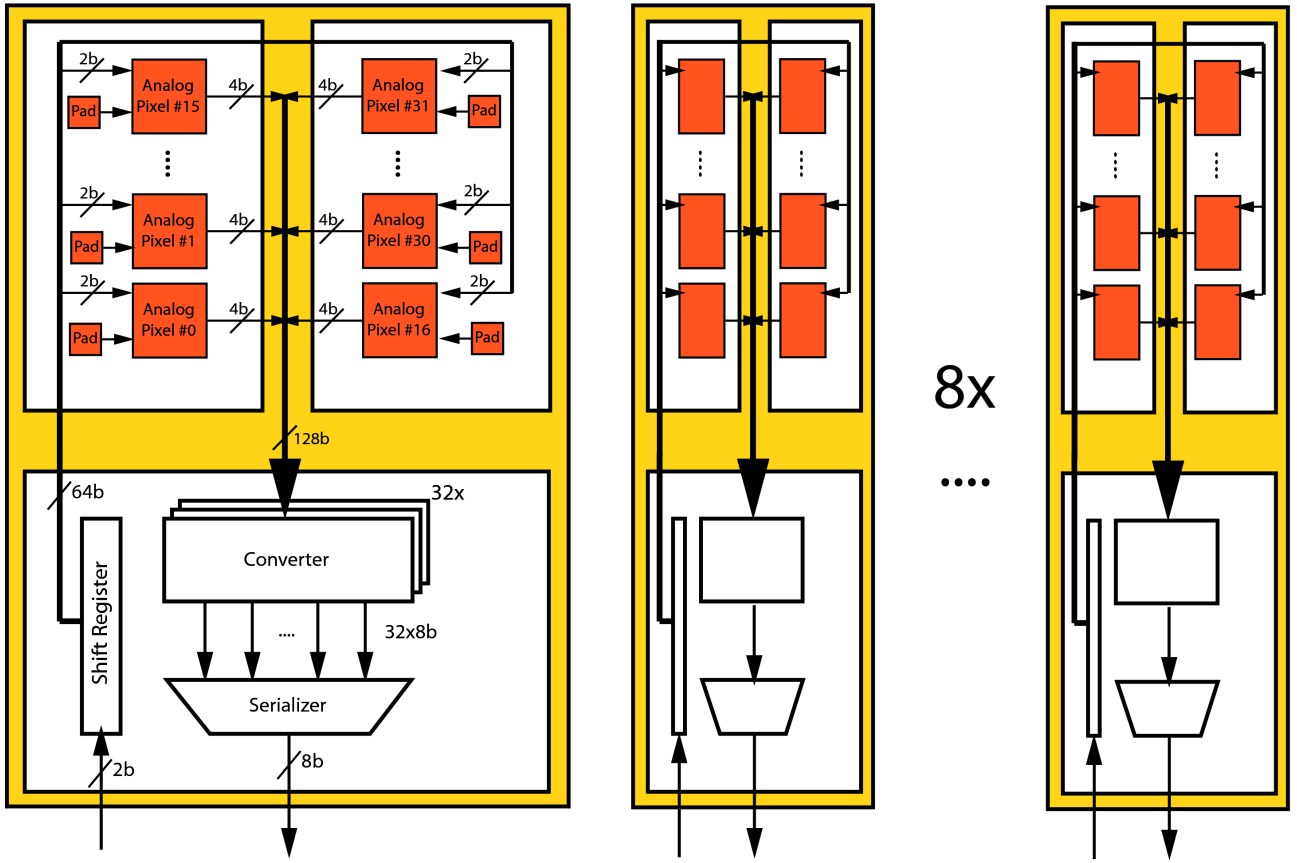
Introduction:
DEPFET Current Digitizer for Belle-II (DCDB)

DCDB's Analog Pixel (simplified!)



- DAC: Dynamic offset correction by adding a variable current to the input node
- Receiver: Trans-Impedance Amplifier for amplification of the input current
- Two Cyclic ADCs: Alternating conversion of analog input current to digital value
- Probes: The input and output node of every pixel's receiver is accessible via the monitor pin
- Optional operation mode: double correlated sampling

DCDB Main Features



256 Channels:

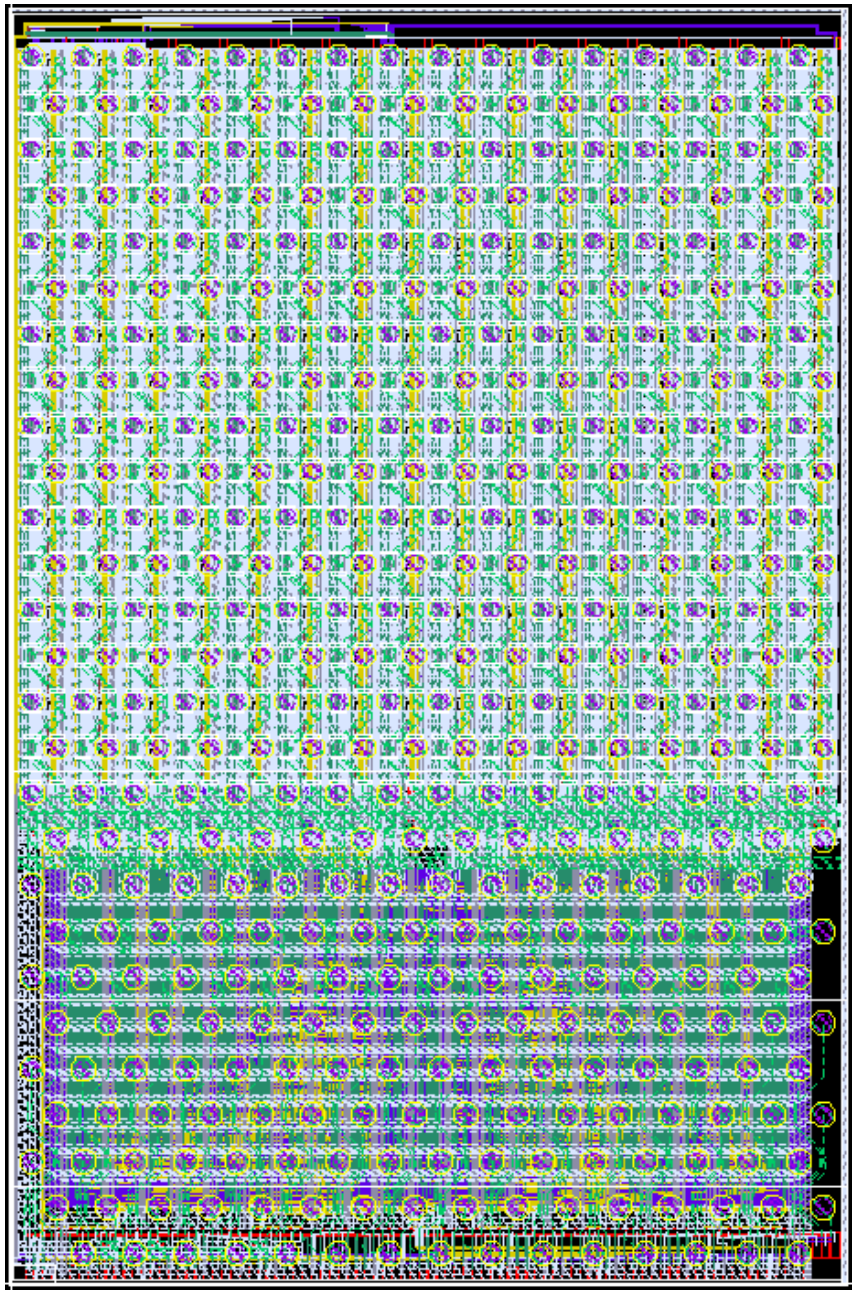
- 8 bit data output (~6 bit ADC resolution req.)
- Dynamic offset adjustment
- 80ns target sampling period
- Power: ~4mW per channel (analog + digital)

Fully synthesized digital readout:

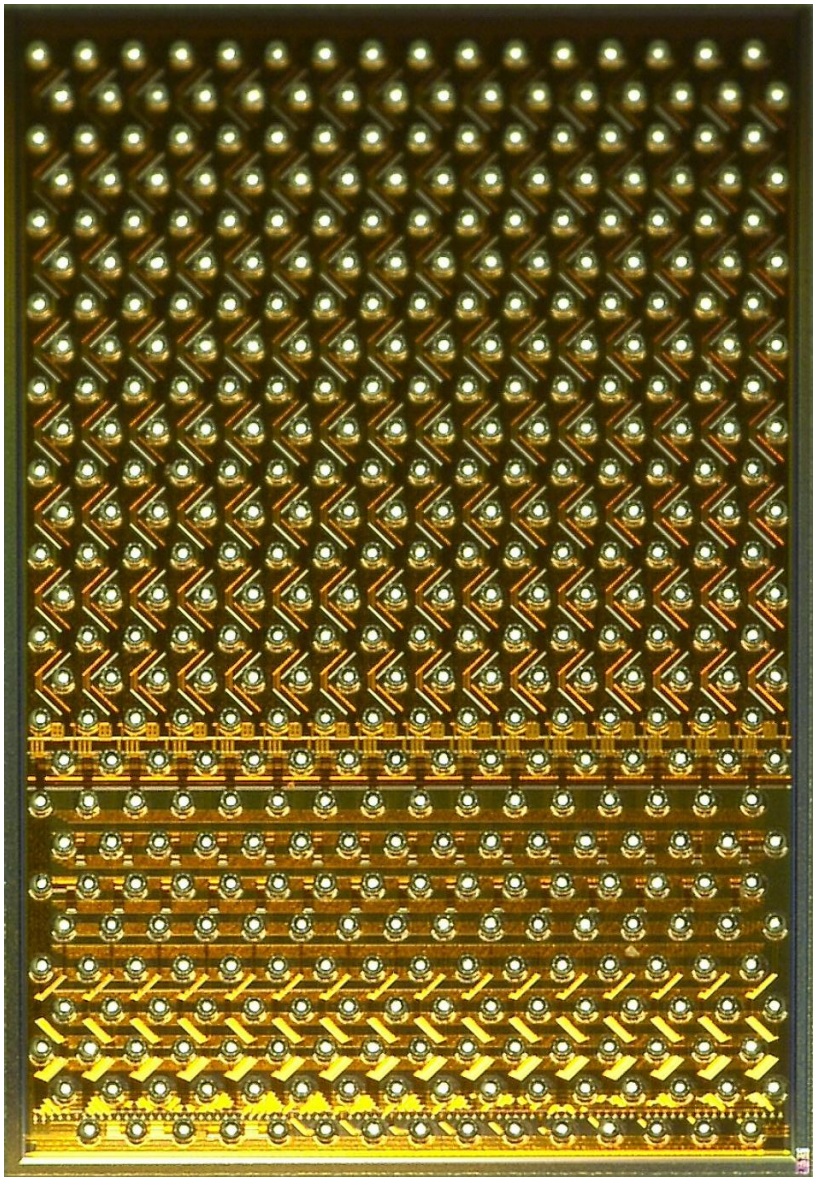
- 8x 8 Bit data output @ 300-400MHz
- JTAG configuration interface
- Using self-made standard cell library

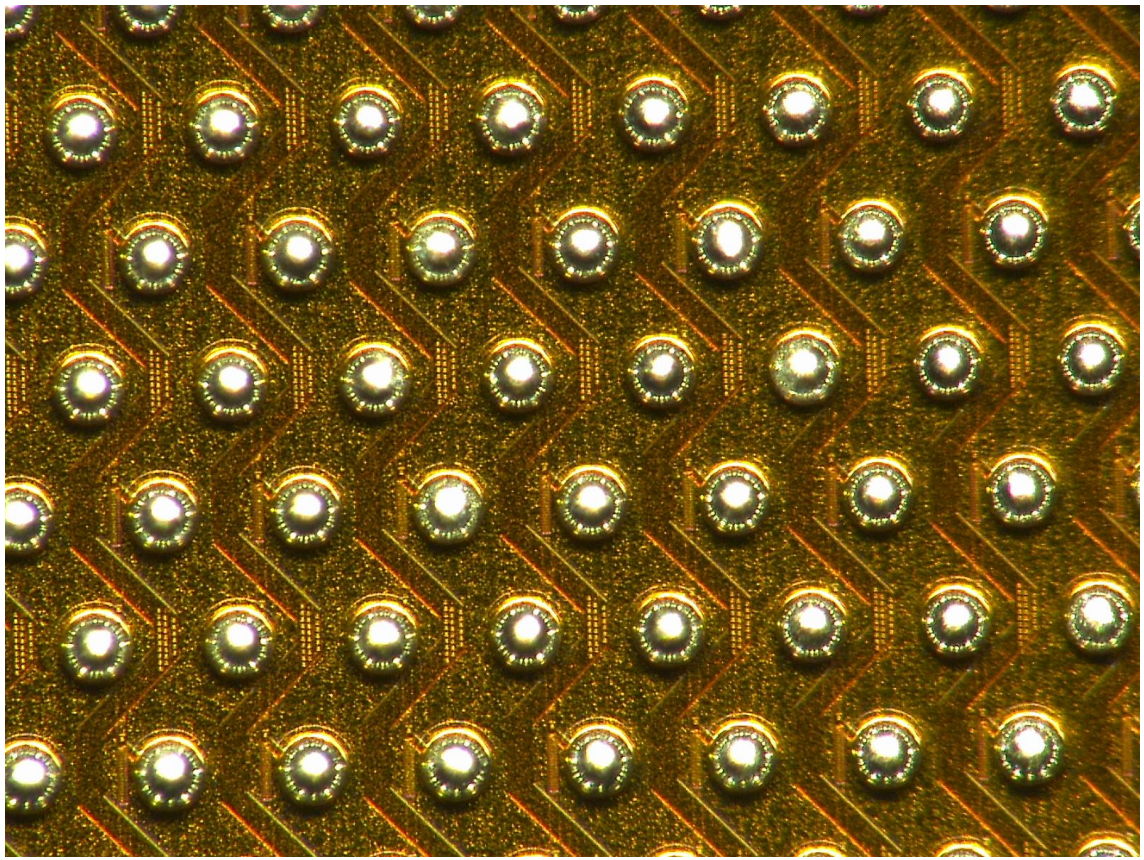
DCDB Production Details

- Implemented in UMC 180nm CMOS technology
- Area: 3240x4969 µm²
- ~ 2x3 Mini@sic Blocks on a EuroPractice MPW run
- Additional 7th metal layer (redistribution layer) with bump-bond pads including bumps
- Production + bumping costs: ~ 20800 EUR (for 60 pcs.)
- Production time: 5 months total
  - 3 months: MPW run
  - 2 months: 7th metal layer + bumping



DCDB Pictures

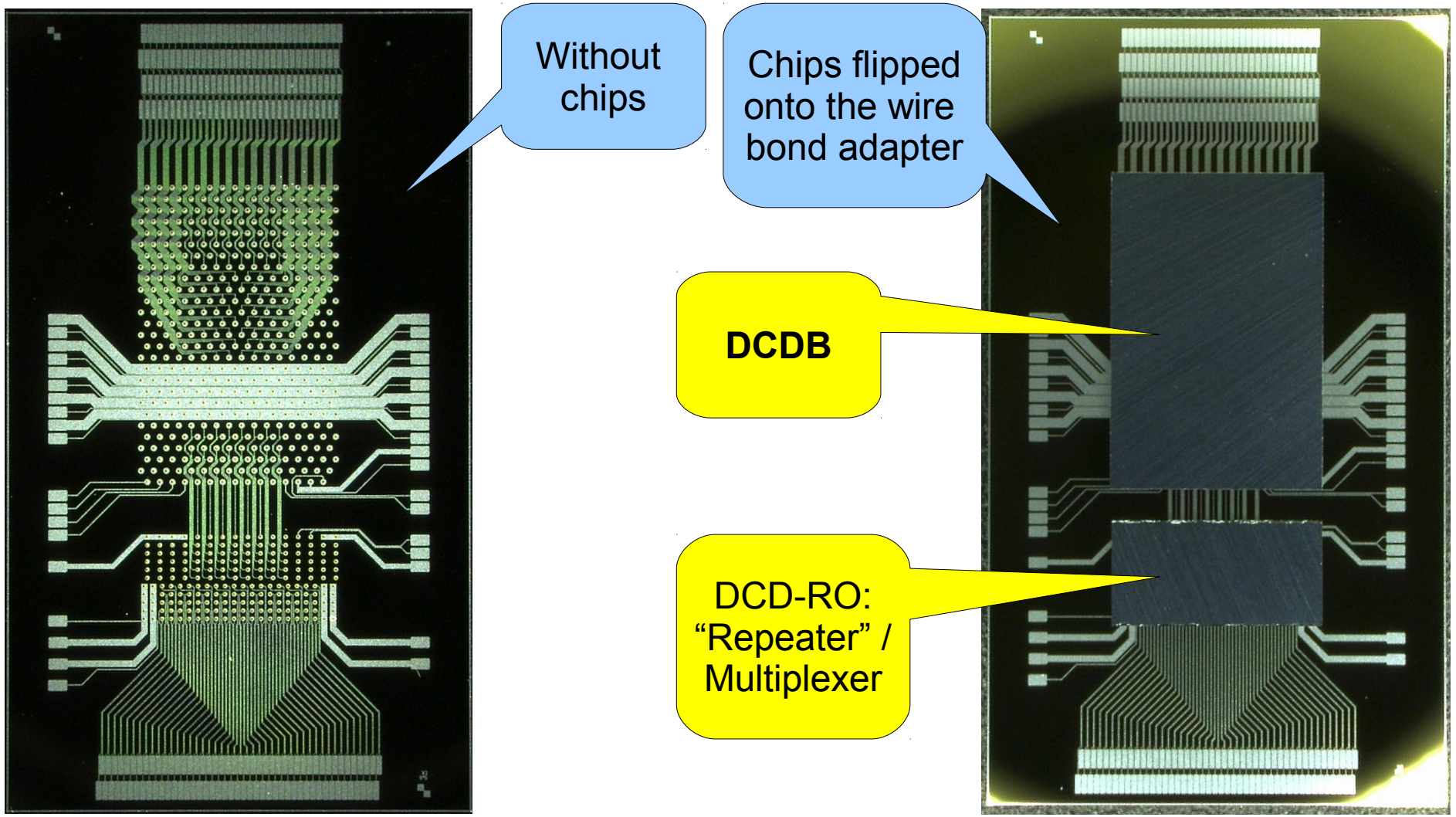




- Bumps @ 200µm pitch
- Increased density by hexagonal pattern

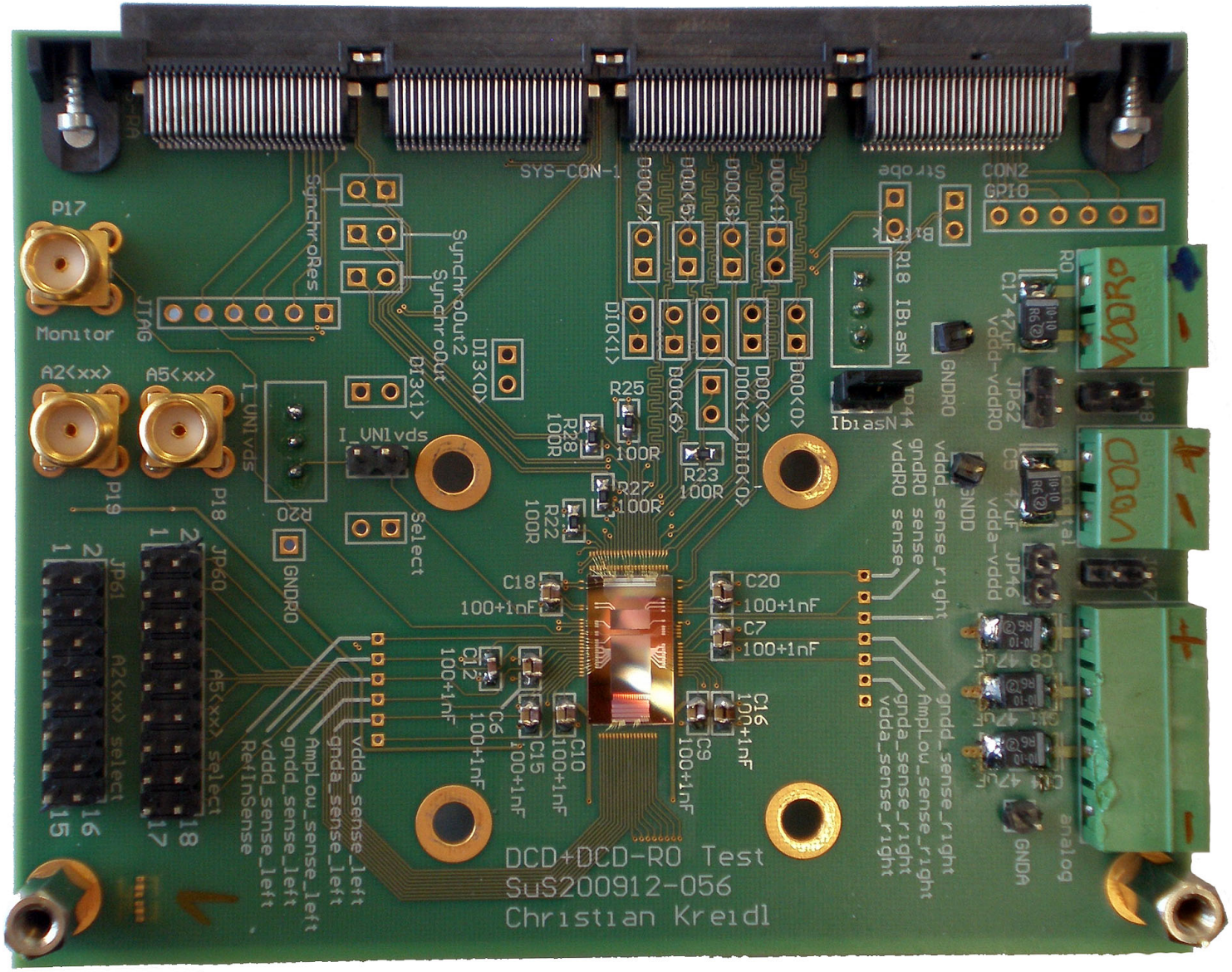
DCDB Test Setup

DCDB Test Environment: Wire-Bond-Adapter

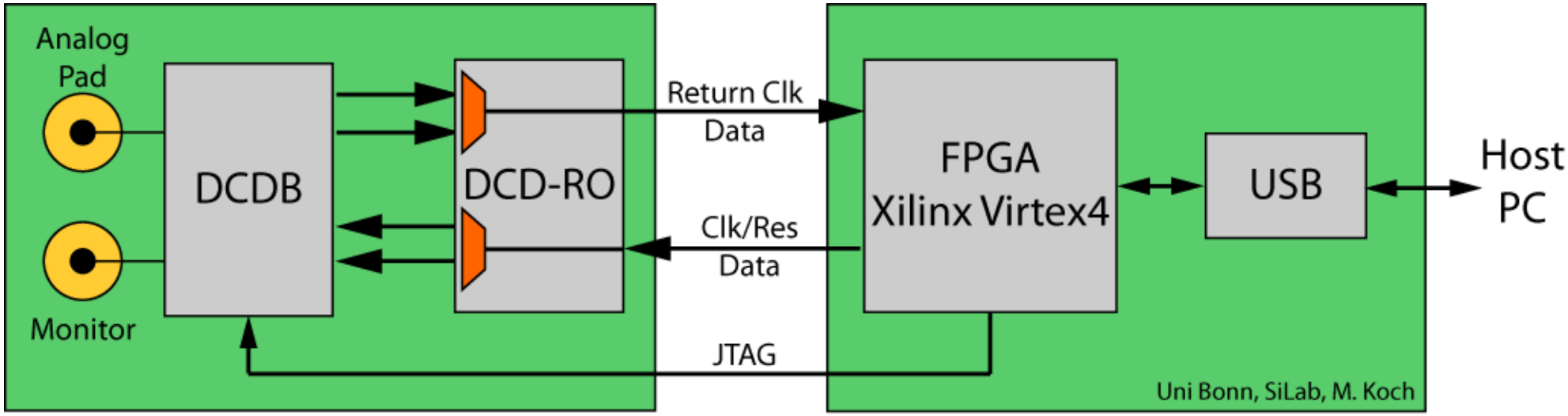


- Substrates designed in Heidelberg, produced at MPG-HLL in Munich
- Flipped using gold studs as under bump metalization

DCDB Test Environment: Pictures

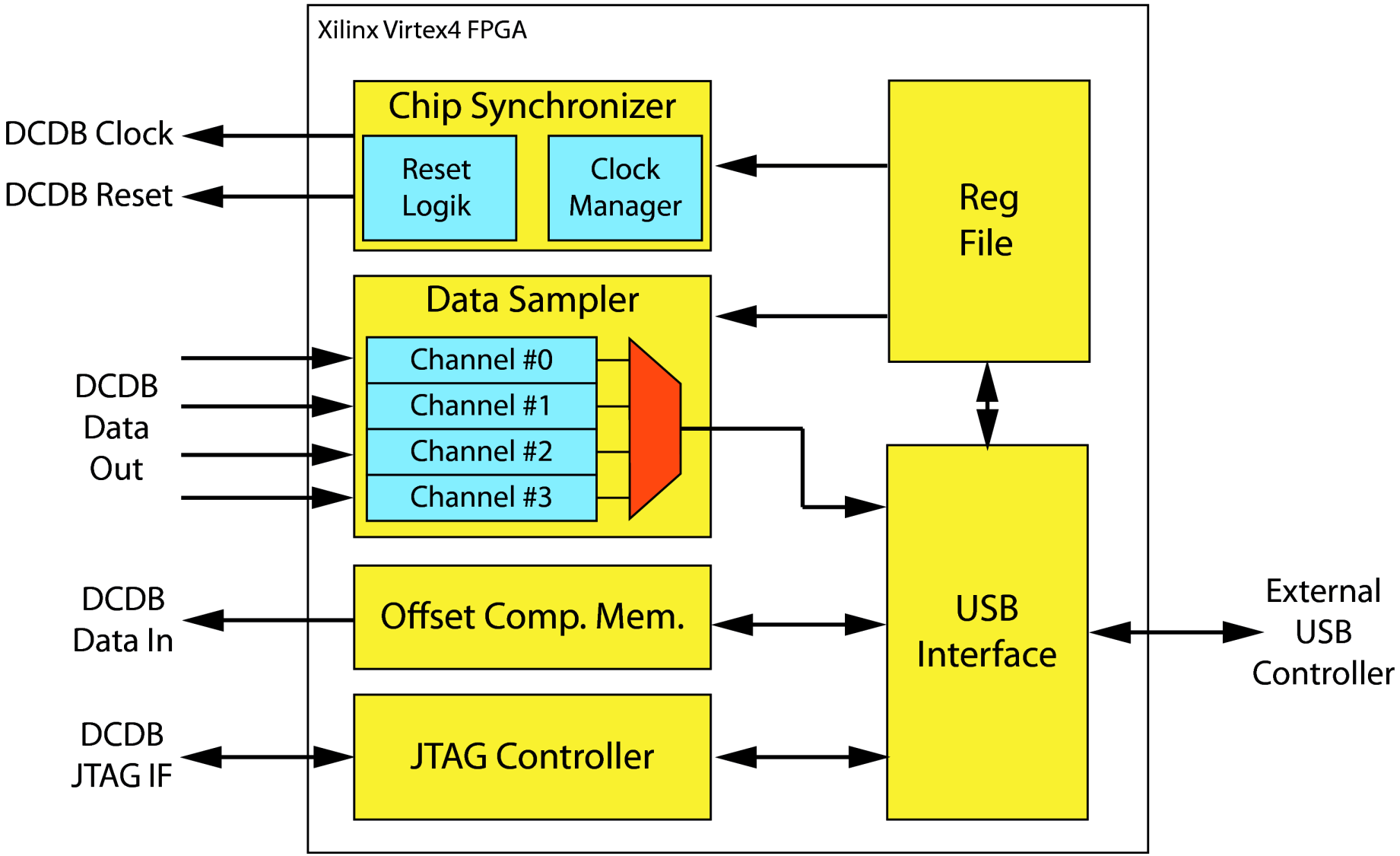


DCDB Test Environment: Hardware



- The test environment is based on a Virtex4 LX40 FPGA board (SiLab - Uni Bonn)
- The FPGA is used for configuring, controlling and reading the DCDB
- The DCD-RO is used for signal conversion / repeating and static 2:1 multiplexing
- SMA connectors bonded to the monitor and some of the analog input pads provide direct access to the DCDB's analog channels

DCDB Test Environment: FPGA Firmware Details



Measurement Results

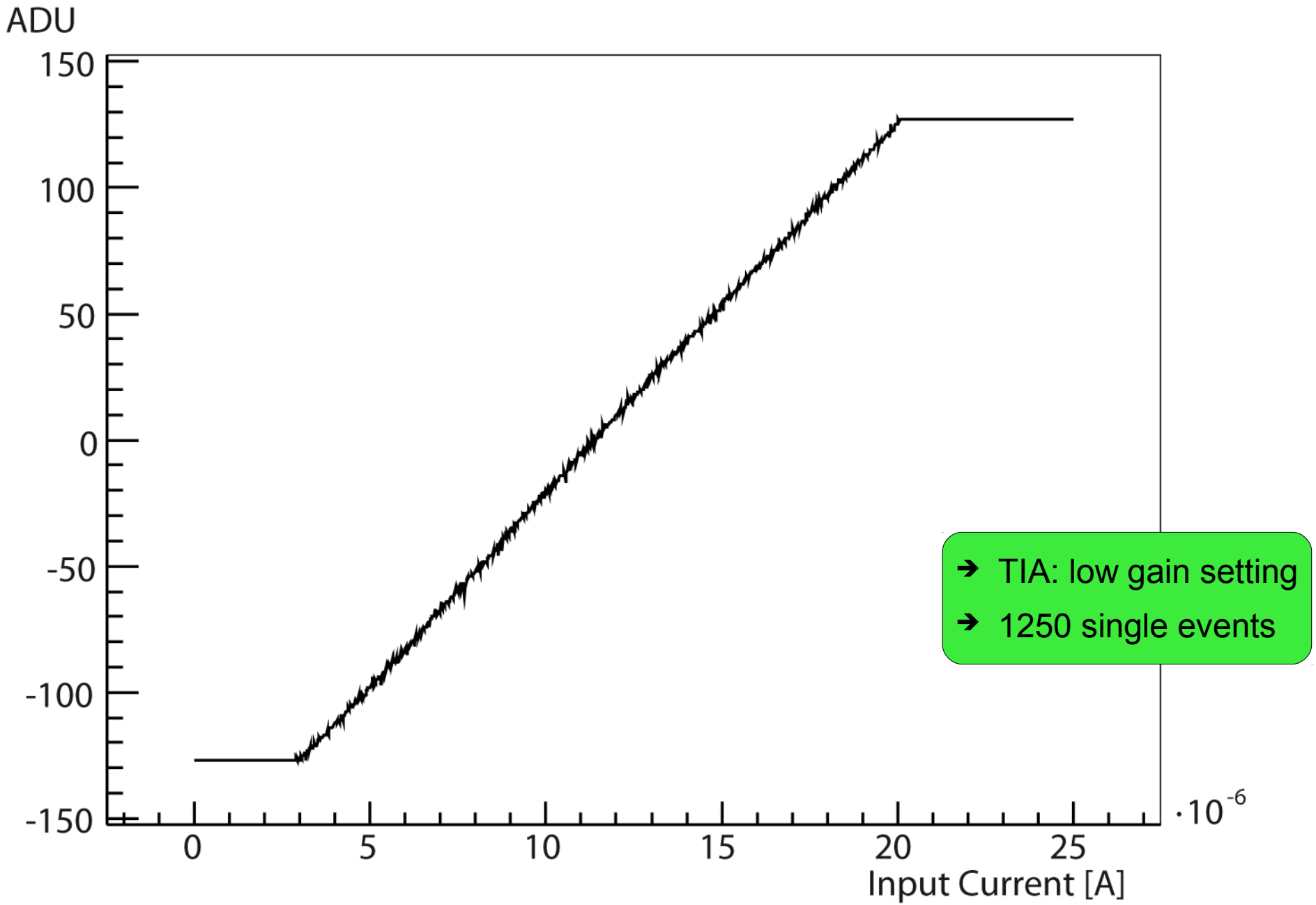
Speed Considerations

- Minimum speed requirement to fulfill 20µs frame readout time:
  - 10MHz ADC sample rate
  - Leads to 320MHz clock frequency
- Digital part: Operates well up to 355MHz (PCB traces not optimized!)
- Analog part:
  - Default clock frequency: 100MHz (→ 3,125MHz ADC sample rate)
  - Operates OK @ 200MHz, but higher noise
- Similar design on test chip operates well up to 350MHz

→ Further investigation necessary

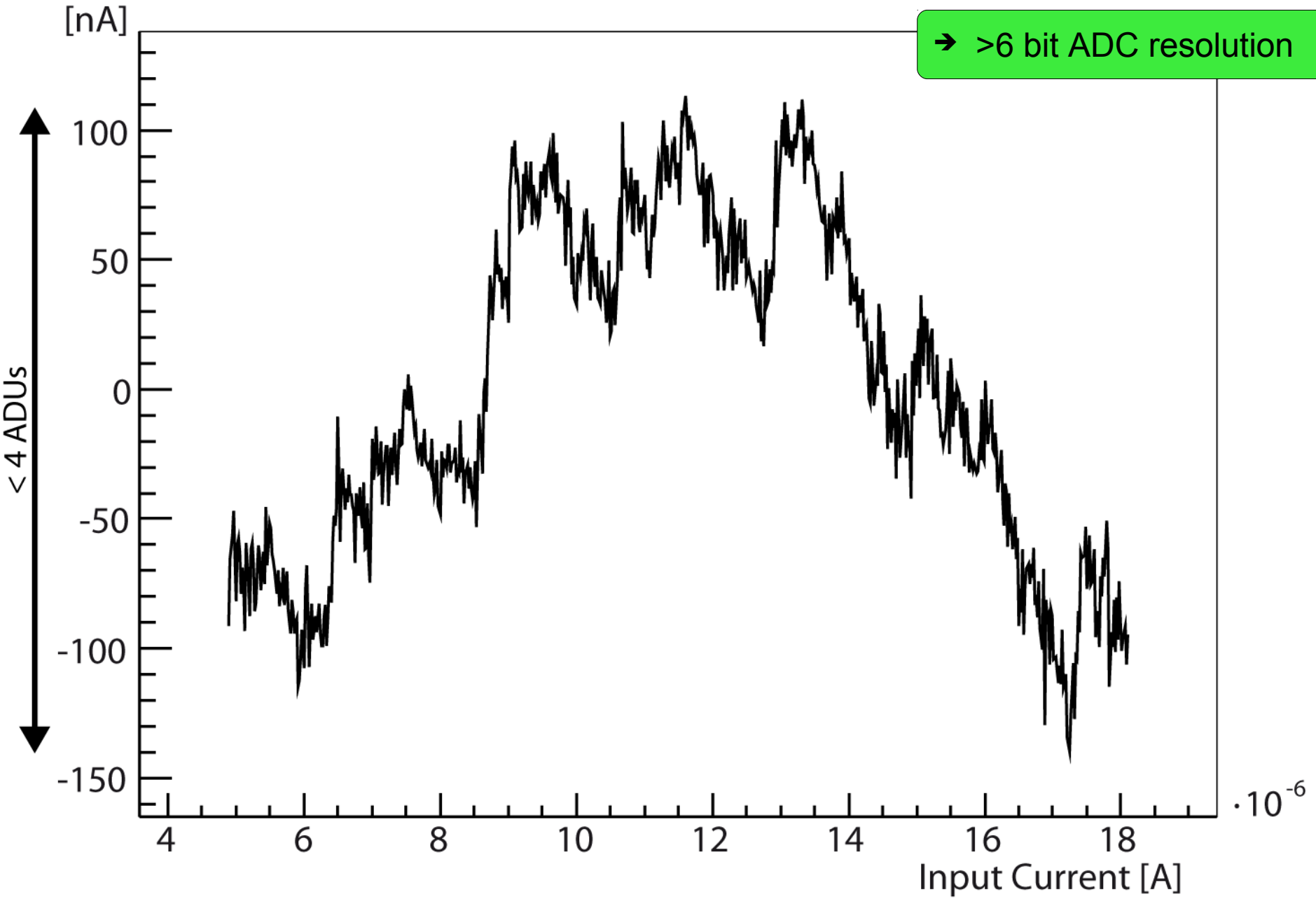
→ Results on following slides were obtained using the default clock frequency of 100MHz

ADC's Transfer Characteristic



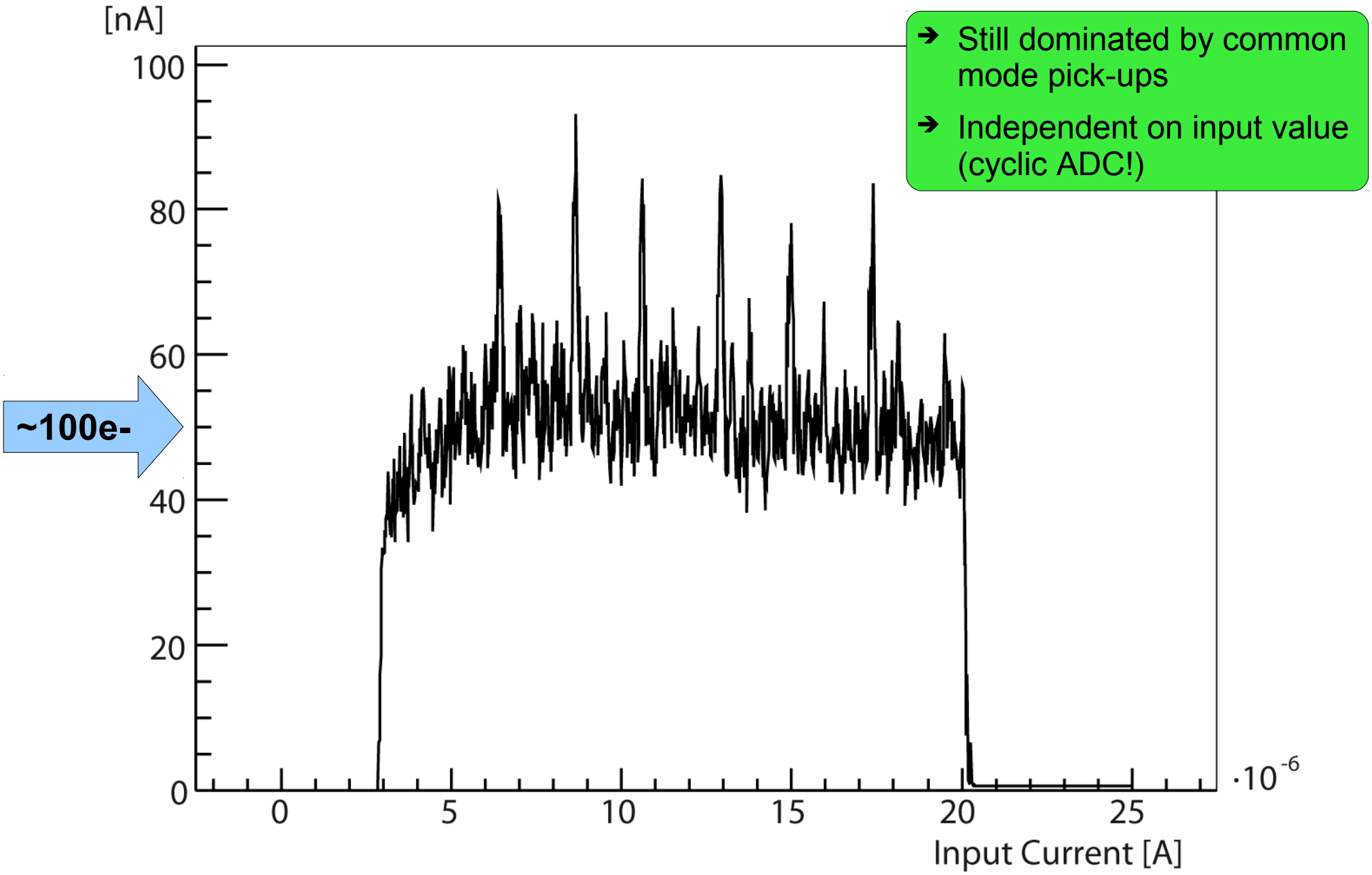
- TIA: low gain setting
- 1250 single events

ADC's Integral Non-Linearity



➔ >6 bit ADC resolution

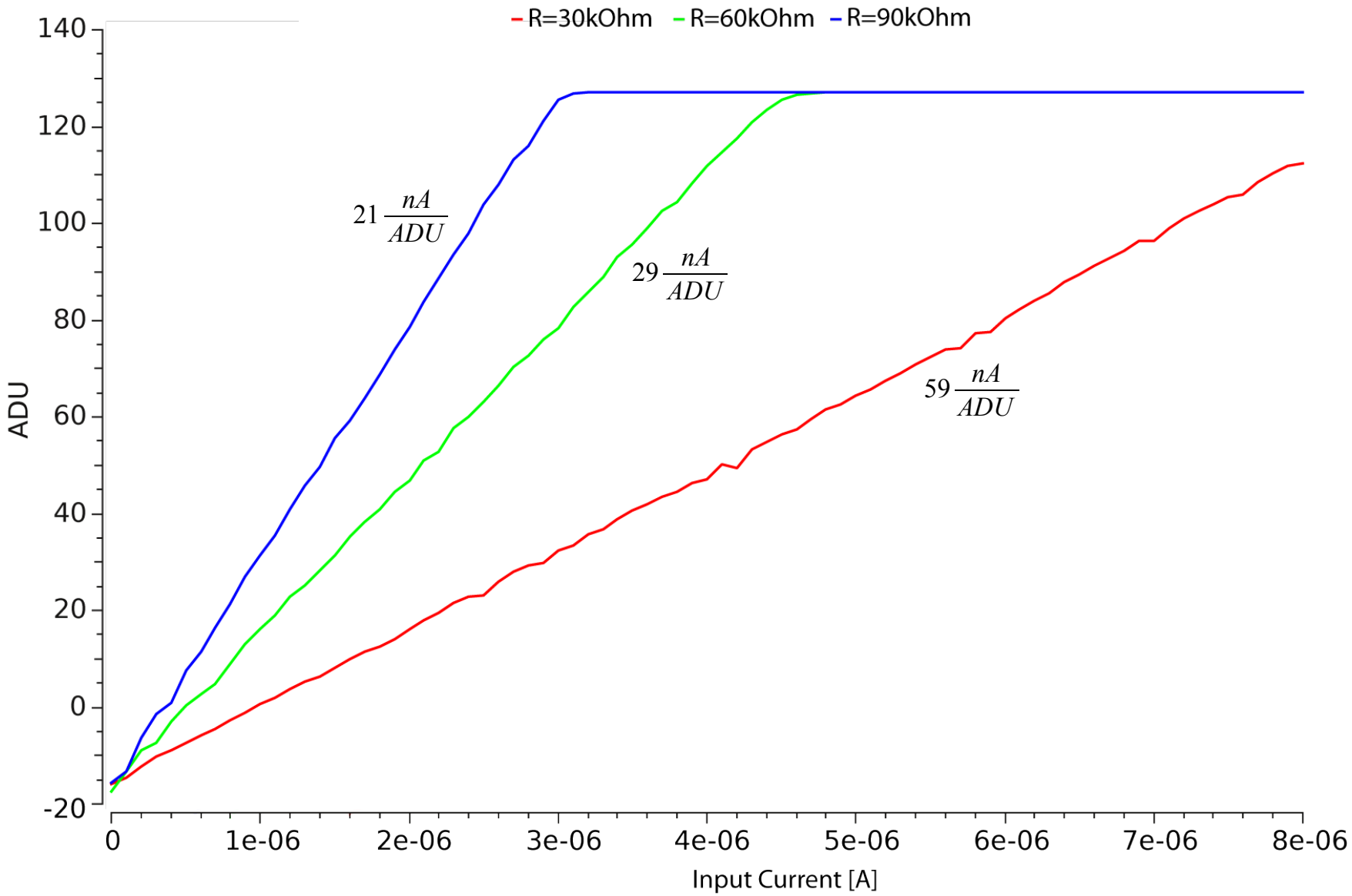
ADC's Noise (RMS)



- Still dominated by common mode pick-ups
- Independent on input value (cyclic ADC!)

Gain Switching

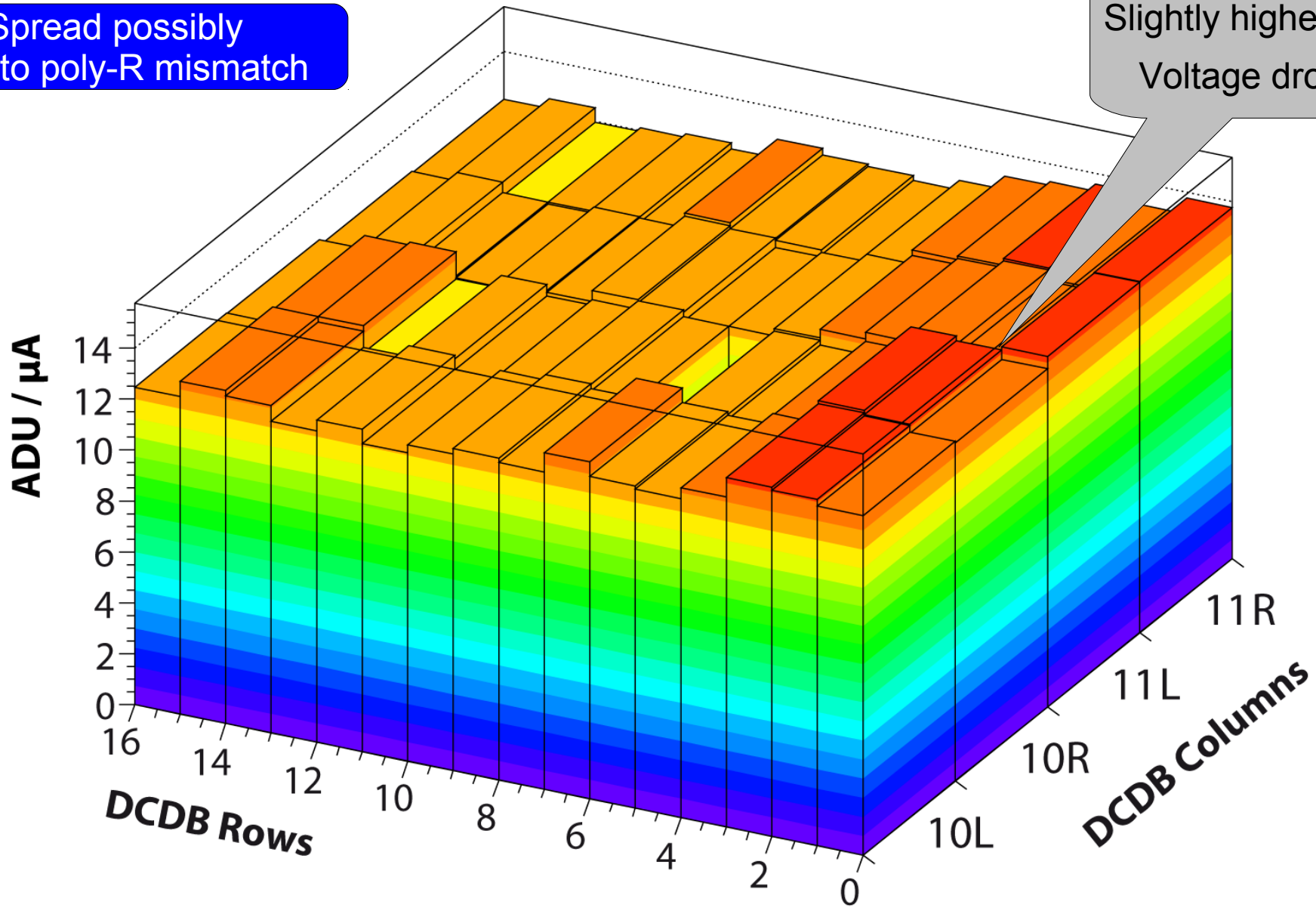
TIA Gain = Feedback Resistor (30k, 60k, 90k)



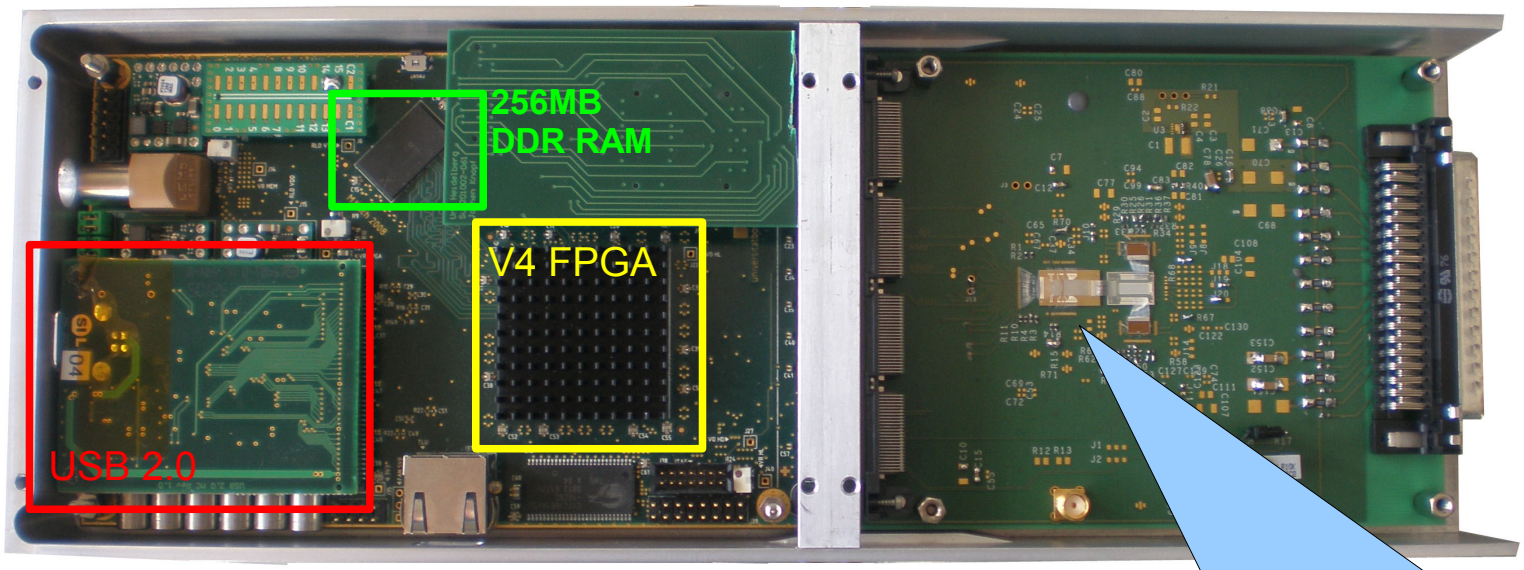
Gain Map

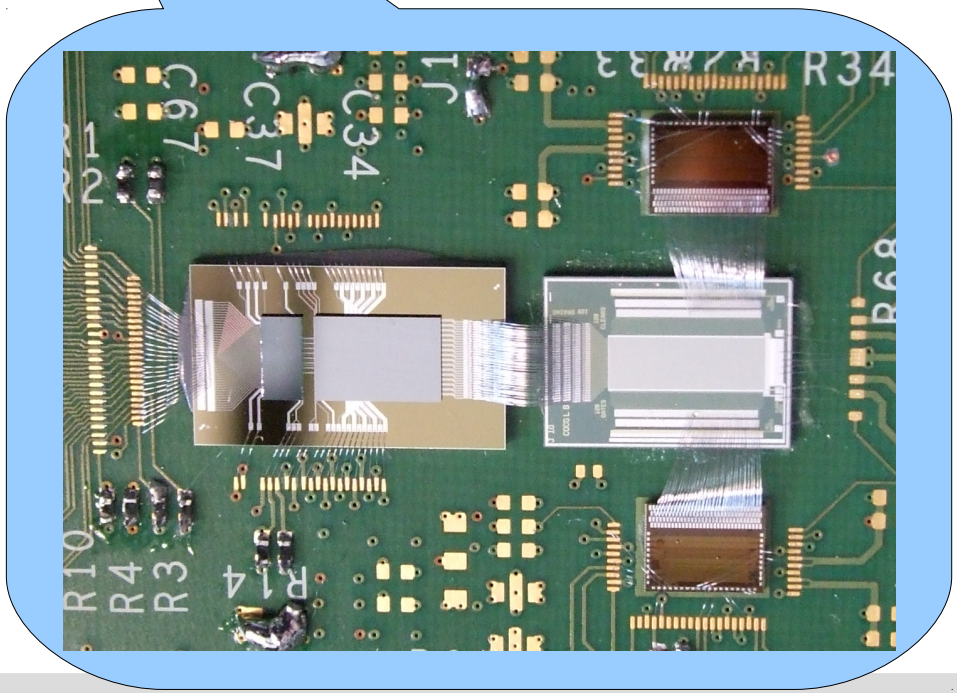
Spread possibly due to poly-R mismatch

Slightly higher gain. Voltage drop??



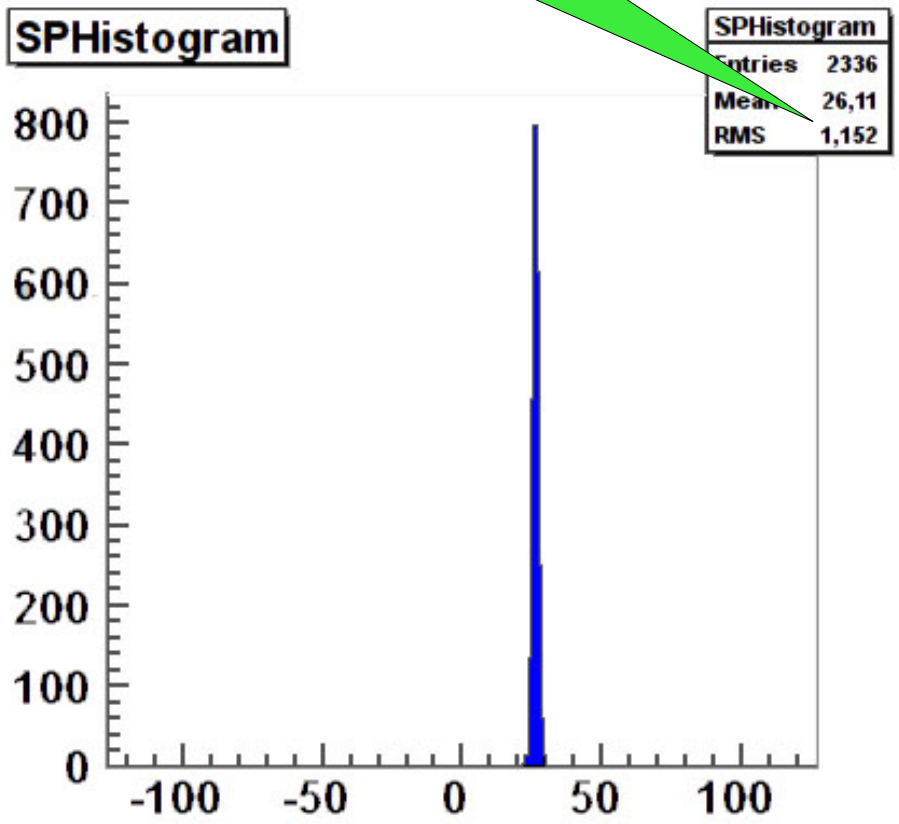
DEPFET Prototype Readout System



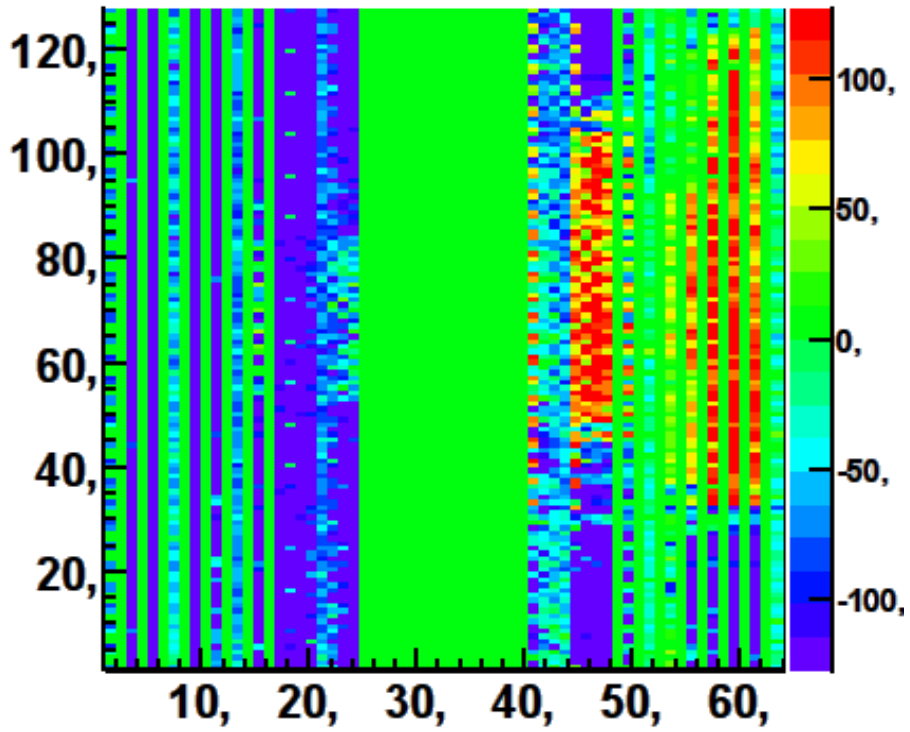


Testbeam @ CERN planned for November 2010

Single pixel noise after common mode correction:
→ 38nA



Laser pointer spot:



Half of the columns are not connected

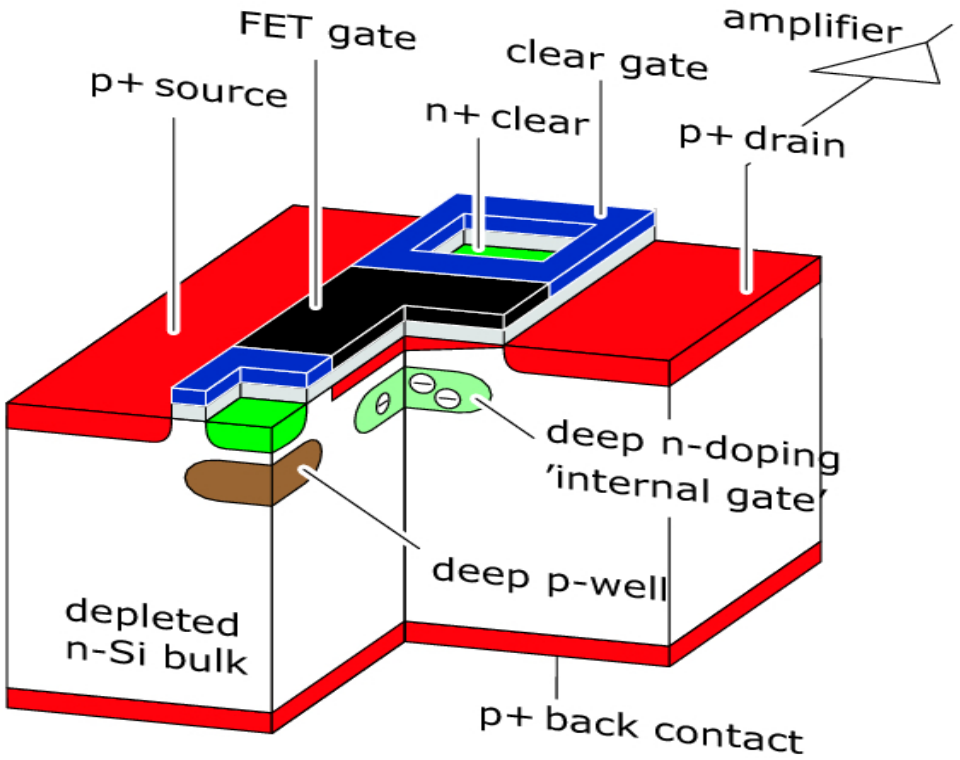
Summary

- DCDB is a complex multi channel readout ASIC for Belle-II PXD
- It contains 256 fast (10MHz sample rate) low power (4mW per channel) ADC channels with 6-8 bit resolution
- Data is digitally transferred off-chip using 8x 8 bit low power links
- Connectivity relies only on bump bonds
- Speed:
  - ➔ Digital part: OK! (~355MHz)
  - ➔ Analog part: 100-200MHz → Investigations necessary
- Noise:
  - ➔ ~50nA dominated by common mode pick-up
  - ➔ ~38nA after correction
- A DEPFET prototype system has been operated successfully

Thank you!

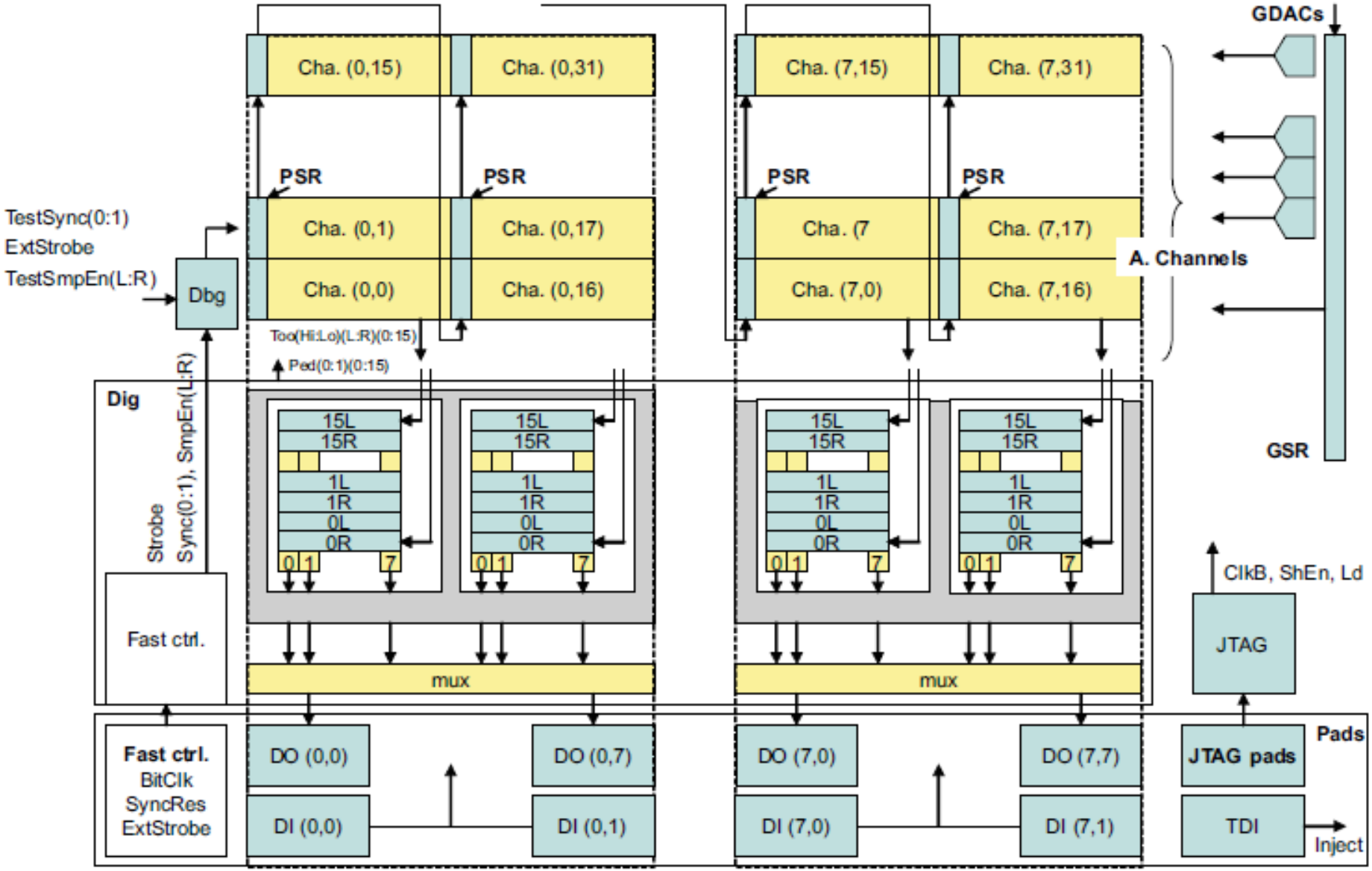
Backup Slides

The DEPFET Transistor

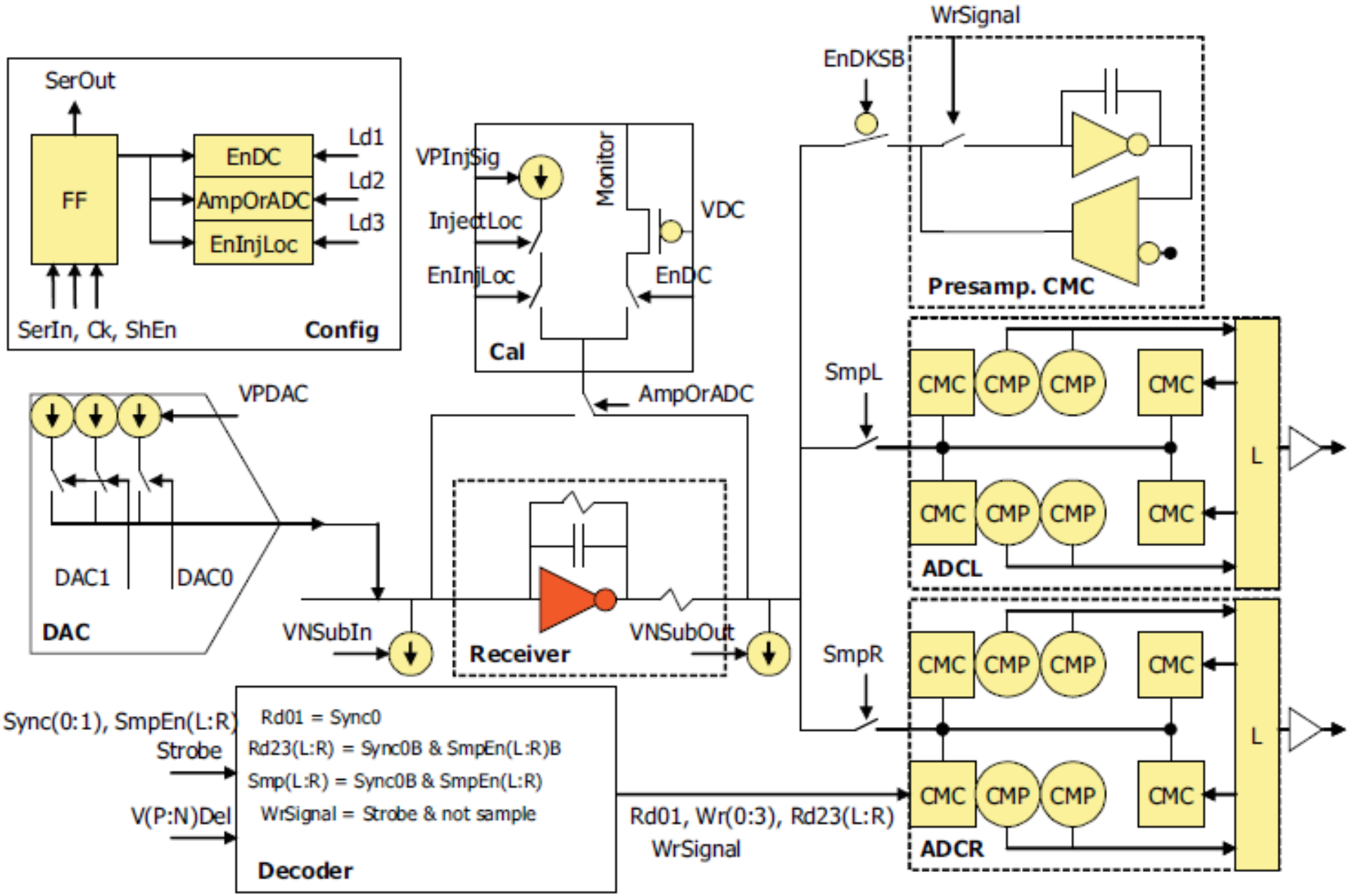


- Each pixel is a p-channel FET on a completely depleted bulk (sidewards depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons underneath the gate (internal gate)
- Signal electrons accumulate in the internal gate and modulate the transistor current (gq≈400pA/e-)
- Accumulated charge can be removed by a clear contact

DCDB's internal Structure



DCDB's Analog Pixel



Measurements: Power Consumption

	Clock Off	100 MHz	200 MHz	400 MHz (extrapolated)
VDDA [mA]	225 (max. 357)	231 (max. 362)	238 (max. 370)	259 (max. 390)
VDDD [mA]	78	131	183	290
RefIn [mA]	18	28	28	28
AmpLow [mA]	129 (max. 250)	128 (max. 250)	128 (max. 250)	128 (max. 250)
Total Power [W]	0,56 (max. 0,8)	0,68 (max. 0,92)	0,79 (max. 1,02)	1,02 (max. 1,25)