An SEU-robust register for application in HEP detector ASICs

S. Bonacini
CERN, European Organization for Nuclear Research, Geneva, Switzerland

Abstract

A new SEU-robust D-flip-flop register structure was designed in 130 nm CMOS for implementation of front-end detector ASICs. The register was tested in a heavy ion beam facility and showed a cross section lower than 10^{-10} cm²/bit throughout all the explored LET range (1.2 – 62.0 MeVcm²/mg), representing an improvement of more than 10^3 times over previously studied standard library cells. No errors at all were observed at LETs under 30 MeVcm²/mg.

Introduction

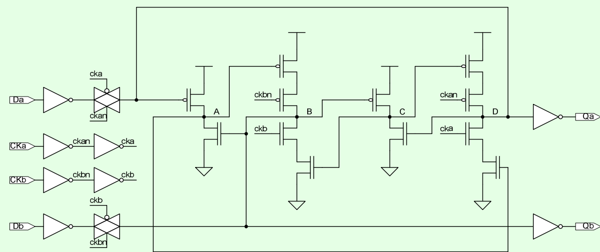
The LHC upgrade will require an increase of the number of detector channels by one order of magnitude with respect to the present setup, necessitating a reduction in power consumption per channel. Though the typical solution used in detector ASICs to the vulnerability of flip-flops in digital logic is Triple Modular Redundancy (TMR), its backdraw is a 3× increased power consumption and area requirement.

The alternative solution proposed in this work is a SEU-robust cell which presents 2× redundancy of the circuitry with respect to a standard D-flip-flop (D-FF), and it is based on the Dual-Interlocked Cell (DICE) scheme. Additional layout techniques are employed to protect the upset-sensitive nodes of the circuit avoiding loss of area.

The register circuit proposed was designed in IBM CMOS 130 nm technology, and fabricated in a chip containing a shift-register of 4096 register cells.

The chips were irradiated in a heavy-ion beam facility in order to assess the register SEU tolerance. The results are compared to a standard library register available in the same technology and previously tested in the same facility.

Irradiation tests were conducted at two different orientations of the chip with respect to the beam in order to assess the sensitivity to multiple-node hits (tilted chip and beam transverse/normal to standard cell rows). No significant difference in the behavior of the circuit was found in the two orientations.



The SEU-robust latch

The SEU-robust register is made of two identical cascaded latches, the first being the master and the second being the slave. The two latches are a modified version of the Dual Interlocked Cell (DICE), which is intrinsically insensitive to single-node particle hits on its memory nodes.

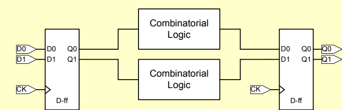
Nevertheless, the DICE latch is vulnerable in case a particle hits multiple nodes, an event also referred to as multiple node charge collection. Additional layout techniques protect the latch from this mode of failure.

The latch is Fully 2×-redundant, having two input terminals, two output terminals and two local clock-buffers. Duplicating the local clock buffer avoids a weakness present in the DICE: if the clock buffer is upset, the whole cell is compromised. The same concept applies to the input pins.

Protection against SETs

The combinatorial part of the logic can be hit by a particle and generate a Single-Event Transient (SET). If the logic is fast enough to propagate the induced transient pulse, the SET can appear at the input of the following latch, where it can be sampled, erroneously, as a valid signal. Whether or not the SET is stored in the latch depends on the temporal relationship between its arrival time and duration, and the falling or rising edge of the clock.

A way of protecting the combinatorial part of the circuitry is redundancy, exploiting the double input and double output of the SEU-robust register.

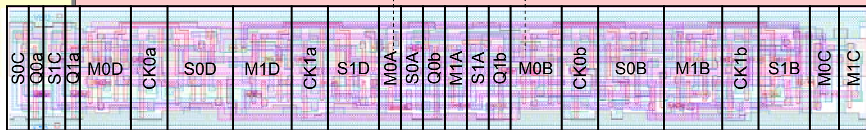


The combinatorial blocks can be duplicated, like in the figure above, in such a way to have two redundant copies of the logic connected to the two redundant inputs of the flip-flops. In this work, the combinatorial part is limited to the inverters/buffers between each element of the shift-register of the test chip.

Protection against multiple-node particle hits

Ionizing particles that travel along the circuit deposit most of their energy in the first microns of trajectory in silicon, thus in order to reduce the probability of this mode of failure, a layout topology which increases the distance of the sensitive correlated nodes is employed.

minimum distance 4.5 µm



In order to achieve spacing with no loss of area, the devices of two registers are interleaved. The cell obtained is therefore a bank of 2 logically independent registers, which are mixed in layout. The figure depicts the layout of the 2× SEU-robust register bank. The register bank layout size is 29.2×3.6 µm² therefore a single register occupies an area of 14.6×3.6 µm², giving a storage density of 19 kbit/mm².

There are a total of 4 latches in the layout and each latch has 4 memory nodes whose mutual distance must be maximized. The figure is divided into the areas which affect the corresponding nodes in the network (drain areas). The master latches nodes are M_xA, M_xB, M_xC, M_xD, while the slave latches S_xA, S_xB, S_xC, S_xD; where x indicates the two registers in the bank '0' or '1'. Clock buffers are indicated with CK_xa and CK_xb, while output buffers with Q_xa and Q_xb.

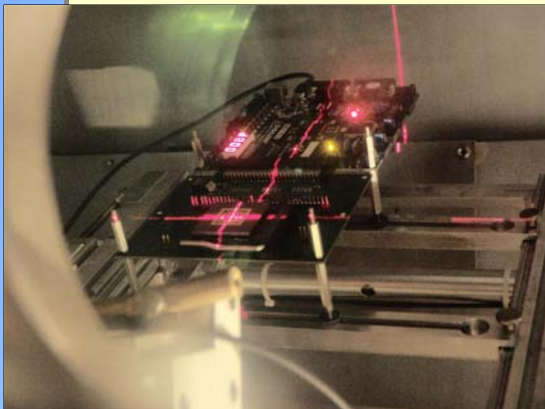
For instance node S0C in the figure must be far away from S0A, S0B and S0D, which belong to the same latch, but it's independent from the rest of the circuit. The minimum (weakest) distance between correlated nodes is 4.5 µm and it is found between nodes M0A and M0B.

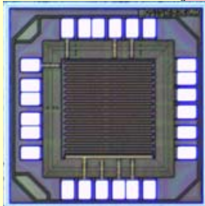
Maximizing the distance between devices implies longer and denser wiring. In the presented layout, most of the routing space of the first 3 levels of metal is necessarily used.

Test chip

A test chip containing 4096 SEU-robust registers (2048 banks of 2 registers), organized in a shift-register, was fabricated in a CMOS 130 nm technology with 8 metal layers. The chip size is 1×1 mm².

The test chip has a dual clock tree, providing timing to the registers through two clock pads.





The dual clock tree avoids SEUs due to hits on the clock buffers.

Two input pads and two output pads are present for the datapath in order to avoid SETs coming from the I/O pads.

Two test chips were packaged in PGA100 for irradiation for increased measurement statistics.

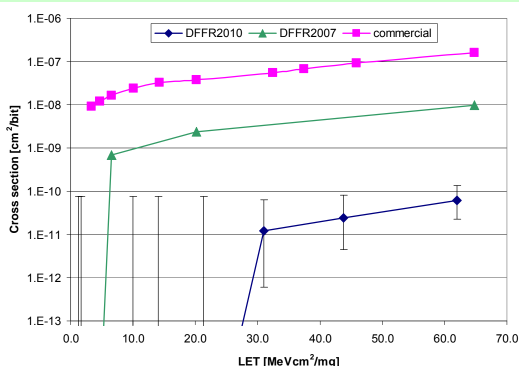
Heavy-ion SEU tests

The chip was tested using a heavy-ion beam facility, applying a checkerboard pattern to the shift-register input of the chips while acquiring and checking the output. All tests were run at 30 MHz frequency. Only dynamic tests were performed (clock running during irradiation).

The present work's SEU-robust register (DFFR2010) proved to be SEU immune in the tests up to an LET of 31 cm²MeV/mg, since no errors were observed below this LET. The register showed a cross-section of 6.09×10^{-11} cm²/bit at an LET of 62.0 cm²MeV/mg, representing a more than 2000× soft-error rate improvement with respect to a commercial standard cell register available in the same technology.

Considering the whole LET range explored, the cross-section of the DFFR2010 is always below 1.13×10^{-10} cm²/bit (upper bound given with 95% confidence level).

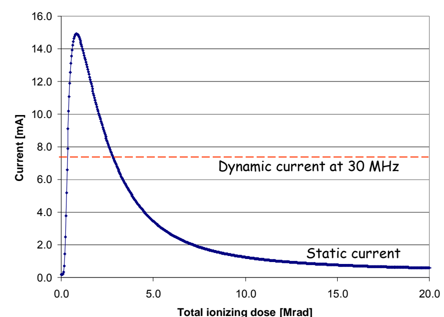
Compared to a previously designed register (DFFR2007), the present flip-flop also shows a big improvement (higher LET threshold, cross-section 150× lower). The DFFR2007 suffered from multiple-node charge collection, since the cross-section showed to be strongly dependent on the angle of incidence of the beam. With the new layout style in DFFR2010 the issue is greatly alleviated.



An especially important result is that the LET threshold of DFFR2010 is above the maximum LET of particles in the LHC environment (about 17 cm²MeV/mg).

Total Ionizing Dose test

A test chip was irradiated in an X-ray beam up to 100 Mrad in order to measure the variation in leakage current of the core shift-register. The test was conducted keeping the chip powered but not clocked (static). Results are shown in the adjacent plot. A maximum increase of the leakage current of 80× with respect to its pre-rad value is visible in the data around 1 Mrad.



After reaching this peak, the leakage current settles back to a value close to the pre-rad, with increasing irradiation steps. Annealing for a week at 100°C reduces further the leakage current below the pre-rad value.

A second test chip was irradiated in dynamic mode (clocked, checkerboard pattern data).

Functionality and supply current were monitored during beam exposure. The chip was functional throughout all the test. The dynamic current of the core when running at 30 MHz is in the order of 40× the pre-rad leakage current, therefore during operation the increase in leakage current due to TID results in a rise of around 3× of the total current, nevertheless not affecting the functionality.

Conclusions

The SEU-robust register presented showed an LET threshold above 30 cm²MeV/mg, higher than the maximum LET of particles in the LHC. The observed cross-section was always lower than 10×10^{-10} cm²/bit. TID tests show a limited increase in operating current with radiation but no change in functionality. From these tests it is evident that the cell is suitable for the use in the LHC environment.

Acknowledgements

The quality of this work was greatly enhanced by the gracious assistance of Dr. Kostas Kloukinas and Dr. Federico Faccio whose advice on design, and help with subsequent analysis, was truly invaluable.