Summary of the Power WG

Ph. Farthouat, M. Hansen, CERN

Agenda

- Power session
  - Development of custom radiation-tolerant DCDC converter ASICs, F. Faccio
  - Progress and Advances in Serial Powering of Silicon Modules for the ATLAS Tracker Upgrade, J. Matheson
  - DC-DC Buck Converters for the CMS Upgrade at SLHC, K. Klein
  - A serial powering scheme for the ATLAS pixel detector at SLHC, L. Gonella
  - Low Noise DC to DC Converters for the sLHC Experiments, G. Blanchot
- Working group
  - Serial power protection, D. Lynn
  - Study and methodology for decreasing noise emissions of DC-DC converters
  - through PCB layout, C. Fuentes
  - EMC CMS tracker upgrade project status, F. Arteche
  - Follow-up of previous meeting

Power working group

- Previous meeting in March
  - http://indico.cern.ch/conferenceDisplay.py?confId=85278
- Does not aim at defining a common solution
- Aims at having the information flowing and at sharing what can be shared
- Good place for seeing the progress of the two possible solutions
  - DC-DC converters
  - Serial power

Progress in DC-DC

- ASIC design
  - Some disappointments
- Module design and EMC issues
  - A lot of progress

Progress in DC-DC – ASIC design

Conclusion

- Three prototype DCDC converter ASICs, with increasing complexity, have been produced and tested
  - The chosen circuit solutions have been verified and improved leading to higher efficiencies and getting closer to a final complete design (with all protection features)
  - The design methodology has been improved with the addition of a behavioral simulation approach considerably shortening simulation time (and allowing study of system stability)
- With the introduction of 'new' LDMOS transistors, and of increased on-chip functionality (regulators), the most recent prototype in the 0.25µm technology has problems incompatible with a final reliable and radiation-tolerant design
  - Further developments in this technology have to wait the qualification and maturity of a set of LDMOS transistors
- Meanwhile, the successful full radiation qualification of the AMIS2 DCDC in the 0.35µm technology indicates a safe path for the rapid development of a radiation-tolerant converter

TWEPP 2010 F.Faccio - CERN/PH/ESE 31

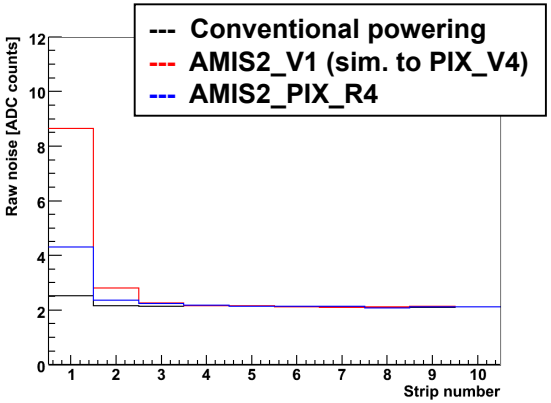
F. Faccio Presentation

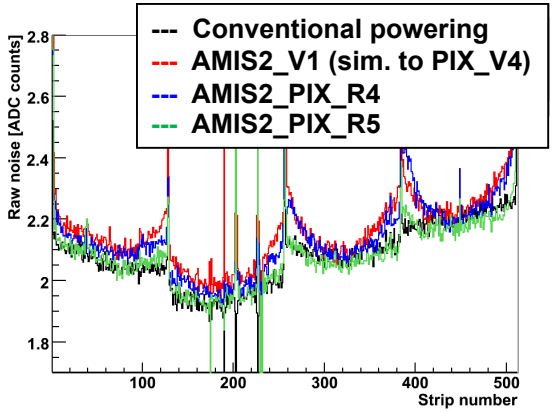
Progress in DC-DC – Modules design

- Modules have been designed with the developped radiation ASICs and also with some commercial components
  - Aachen and CERN
- Aims at understanding all EMC issues and at solving them

- Very nice presentation from C. Fuentes during the WG going in implementation details to reduce the noise
  - Contains a lot of usefull practical information

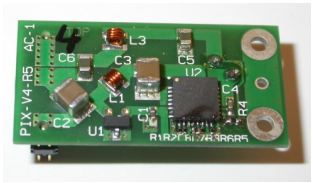
DC-DC Modules: Aachen work

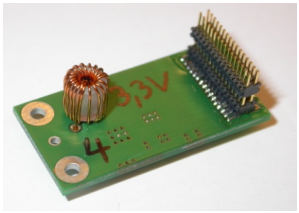




K. Klein Presentation

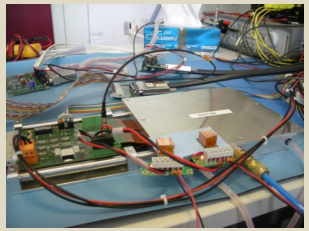
- Less conductive noise with PIX_V4_R4
- Reduction of radiative pick-up when coil is soldered on backside of board (R5)





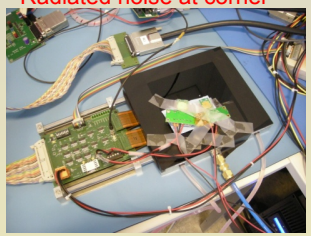
DC-DC Modules: CERN work

Optimized AMIS2 DCDC on UniGe Module

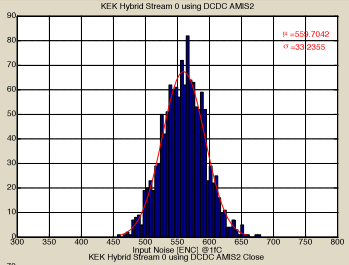


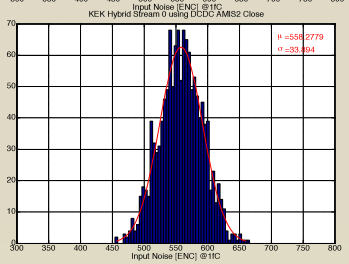
Conducted noise test

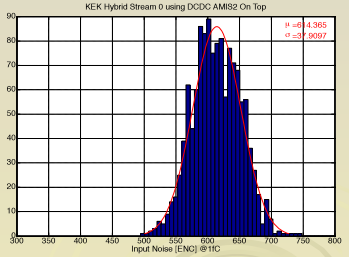
Radiated noise at corner



Radiated noise on top of hybrid







- **AMIS2_DCDC, shield:** — **ENC** — **Sigma**
  - Reference: 560 32
  - Conducted: 560 33
  - Radiated Corner: 558 34
  - **Radiated Top: 614 38**

VCC and VDD are each powered from two different DCDC converter, without regulator on VCC.

The AMIS2-PIB, induces 10% more noise with respect to the reference configuration, when two converters are place straight on top of the hybrids.

The improvement is very significant, and is in line with the noise reduction observed on the reference test stand (CM and DM noise).

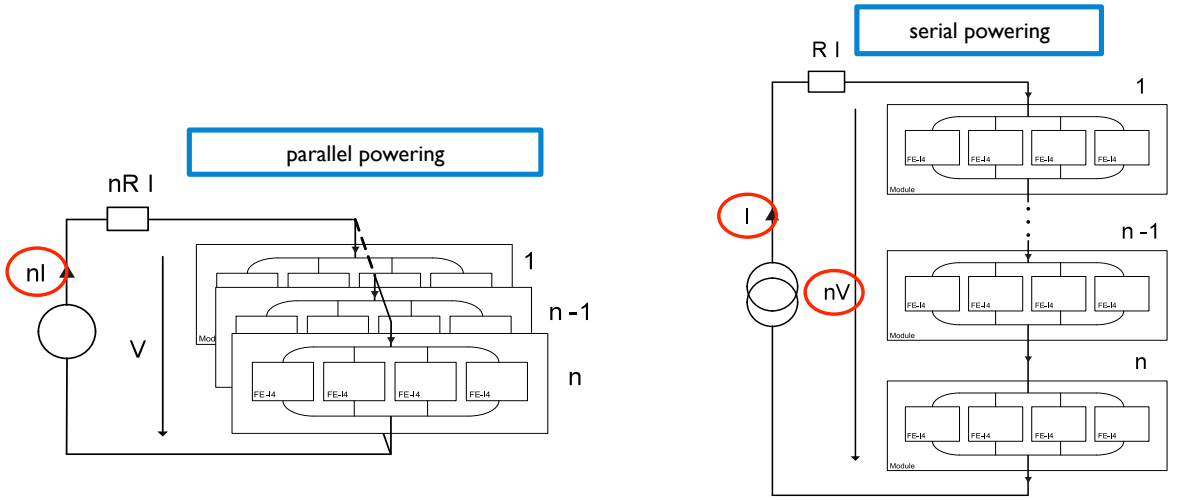
TWEPP 2010 G. Blanchot, PH/ESE 16

G. Blanchot Presentation

Serial powering

- Allows transmitting power at low currents and high voltages
  - A chain of n modules is powered in series by a constant current I
  - Current to voltage conversion is performed locally (on chip/module) by regulators
- Key facts
  - I scales of a factor n, with respect to parallel powering
  - V_{drop} is limited only by the power density and the I source output voltage capability
    - Allows optimal trade off between efficiency and material

L. Gonella Presentation



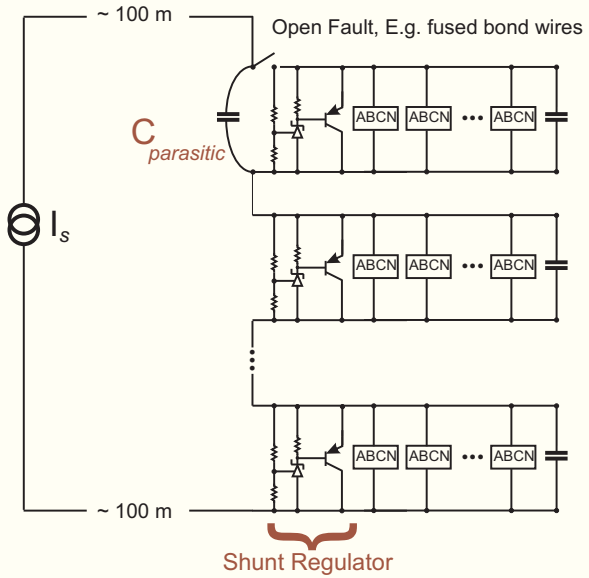
Progress on Serial Power

- Systems aspects have been developed
  - Protection
  - Efficient switching off of a module
- On going developments and tests for the ATLAS pixels and strips
  - Very good performances with a strip stavelet

Serial Power: Protection

Motivation and Design of Serial Power Protection

- For a sudden open circuit, local protection is needed as current source power supplies are too far away to shut off current to stave; For example...
- If the current source is far away (~100m in Atlas), the quickest time current could be shut off at stave is approximately 200m / (2/3 speed of light) = 1μs.
- If I_s= 1 A , $\Delta V = \Delta t\ (I/C_{para})$ = 100kV!! Sparks would likely develop before the supply could respond and may unpredictably further damage stave and make a subsequent DCS enabled bypass ineffective. Stave may become inoperable.

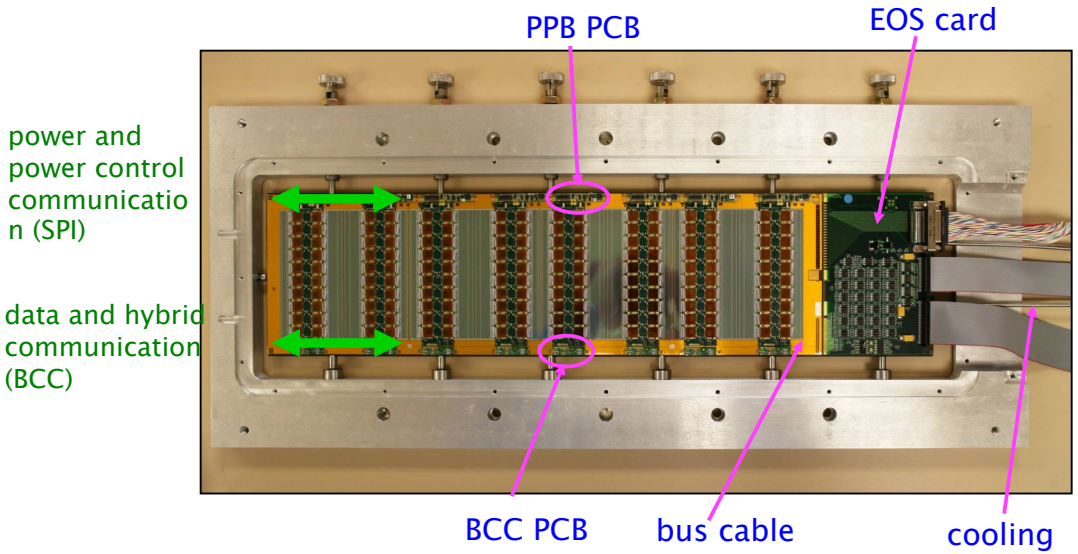


D. Lynn Presentation

- In addition to such local *Real-Time* protection, a DCS (or slow controlled) enabled bypass is desirable, e.g. to short a noisy module, or short a module that draws too much current after irradiation. *Slow Control Bypass saves serial power chain from any non-real-time failure mode.*

ATLAS Stavelet for tests

The Stavelet with ABCN-25 readout



J. Matheson Presentation

A stavelet to be used with DC-DC converters is in preparation

- Allows comparison of: Different power configurations, Different bus cable designs, Different grounding and shielding concepts
- Stavelets allow option choices for later stave construction
- One built, second under costruction at RAL
- PPB carries protection and power plugin

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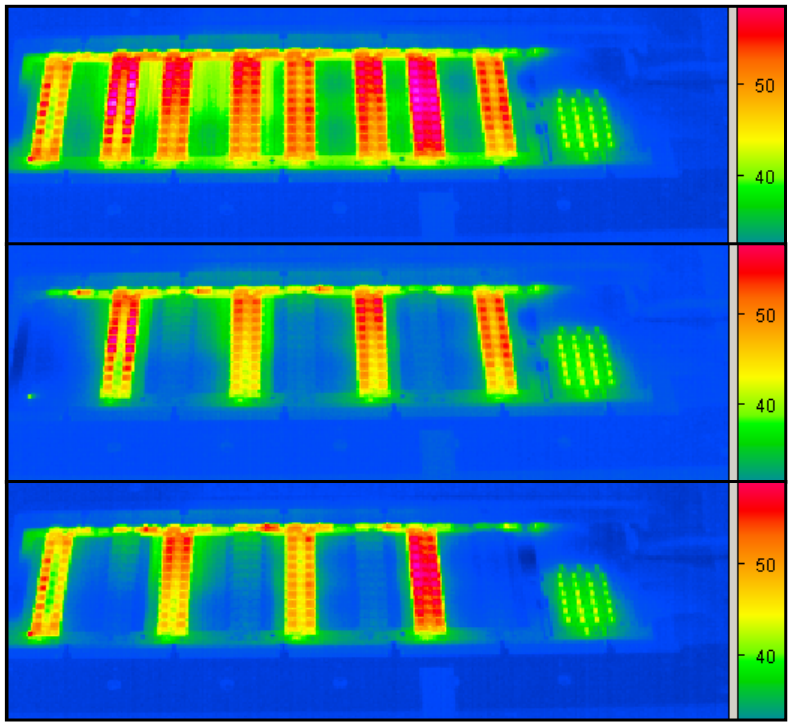
Serial Power: Protection scheme

Thermal images of stavelet in operation



All hybrids on

22.7V
5.09A

Slow control disables odd hybrids

12.7 V
5.09 A

Slow control disables even hybrids

J. Matheson Presentation

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EMC Studies

3. Working packages – Status & Plans

- The project has started in 2010
- It is divided in four working packages
  - WP 1: Power network impedance characterization
  - WP 2: Noise propagation effects in power network
  - WP 3: Noise immunity test in FEE prototypes
  - WP 4: Validation of EM immune OFS for temperature, magnetic field and strain: Effect on overall EM noise
- Strong collaborations with other groups is planned
  - FERMILAB – M. Johnson
  - Aachen – L. Feld & K. Klein
  - CERN – F. Faccio & G. Blanchot
  - Others collaborations are welcome

- An approved (and funded for 3 years) project for CMS aiming at studying EMC of a large system with DC-DC

F. Arteche Presentation

Follow-up of last meeting

- System simulation
  - System simulation was only presented in March for the SP scheme
  - Models are now available also for DC-DC
  - Both simulation to be done with similar system
- Wish list of system tests to be done with all solutions
  - Much more an ATLAS affair
  - However a list of tests and measurements to be done can only help
- Can we define limits on noise emission and system susceptibility as done for ATLAS?
  - The answer is probably yes but nobody volunteered
- Next Power WG during the spring