TWEPP-10
Topical Workshop on Electronics for Particle Physics
Aachen, Germany | 20-24 September 2010

3D-IC MPW runs for HEP

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Agenda

- Introduction
- Motivations for 3D-IC Integration
- CMC-CMP-MOSIS partnering on 3D-IC
- Process Overview
- MPW runs
- Design Platform features for 3D-IC
- 3D-IC automatic Place & Route
- Conclusion

Introduction

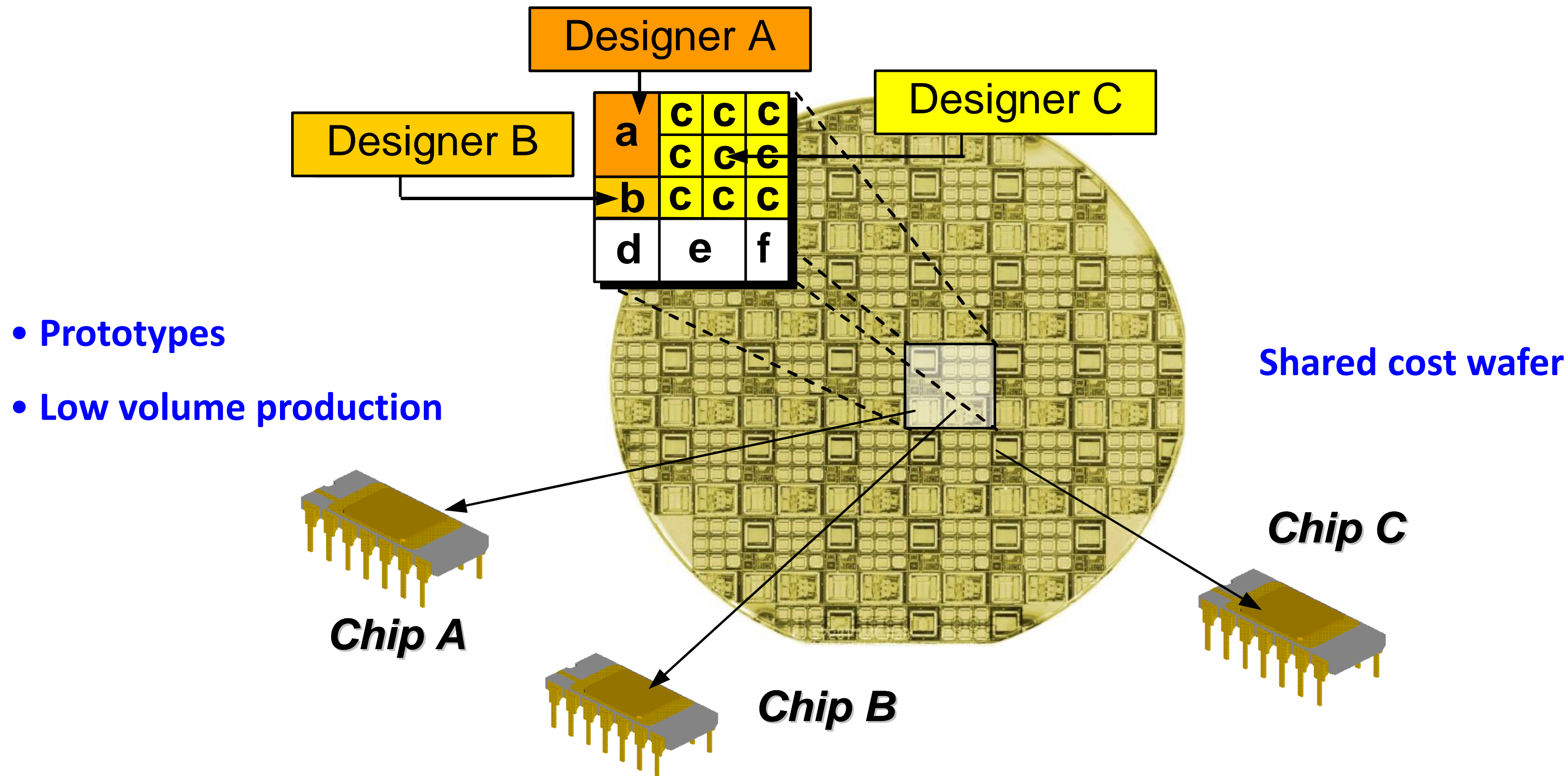
- CMP created in 1981
- Offering industrial quality process lines
  (University process lines cannot offer a stable yield)
- Design-kits to link CAD and MPW, to facilitate the design.
- Customer base development
  + Universities / Research Labs
  + Industry
  + 1000 Institutions in 70 countries
- Non-profit, Non-sponsored

Multi-Project Wafer (MPW)

Multi-Project Wafer runs allow to share the price by sharing the reticle area.

❒ **Prototype fabrication.**

❒ **Low volume productions (some hundreds to hundred thousands parts)**



Technology Processes in 2010

IC :

austriamicrosystems	0.35 µ CMOS / CMOS-Opto 0.35 µ SiGe 0.35 µ HV CMOS 0.35 µ HV CMOS EEPROM	0.18 µ CMOS 0.18 µ HV CMOS
STMicroelectronics	40nm CMOS 7LM 65nm CMOS 7LM 130nm CMOS 6LM	65nm SOI 130nm SOI
		130nm SiGe BiCMOS

3D-IC :

Tezzaron / GlobalFoundries — 2 Tiers 3D-IC / 130nm CMOS

MEMS :

- CMP/austriamicrosystems — 0.35 µ CMOS bulk micromachining
- MEMSCAP — PolyMUMPS, MetalMUMPS, SOI-MUMPS
- SANDIA — SUMMIT V

CAD Tools : Tanner, ARM , Mentor Graphics, SoftMEMS
IP exploitation : ARM cores on STMicroelectronics processes (130nm and 65nm)
Design kits : more than 35 different kits

Packaging : Ceramic, plastic, optical, custom ...

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CMOS Process Roadmap

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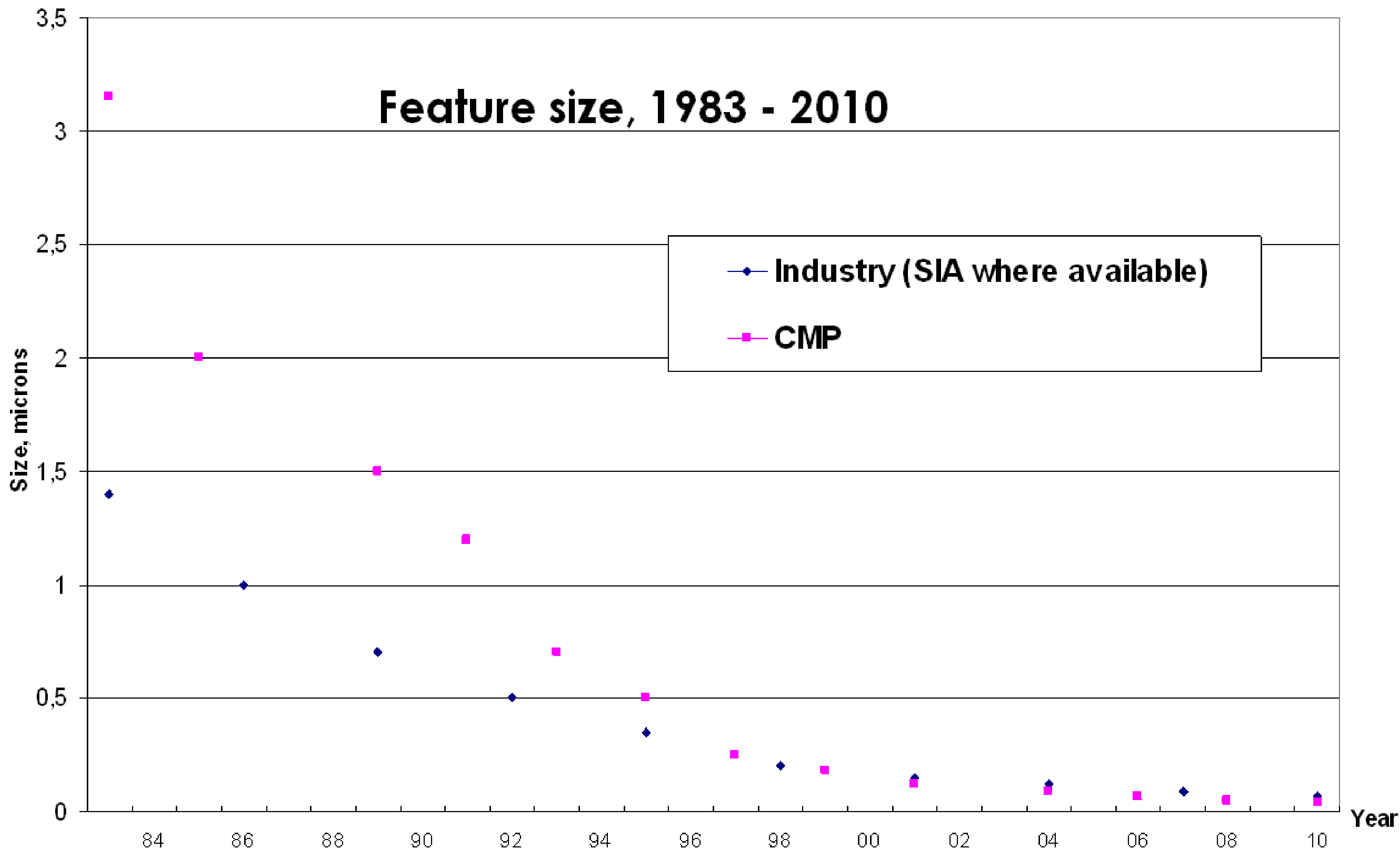

CMOS Feature Size at CMP

- High density
- Low power
- More system Integration
- More Process Features

AMS 0.8μ	AMS 0.6μ	AMS 0.35μ	ST 0.25μ	ST 0.18μ	ST 0.13μ	ST 90nm	ST 65nm	ST 40nm
1.2k gates/mm²	3k gates/mm²	18k gates/mm²	35k gates/mm²	80k gates/mm²	180k gates/mm²	400k gates/mm²	800k gates/mm²	1600k gates/mm²

1994 at CMP **2010 at CMP**

3D-IC Integration : The Other Path for Scaling

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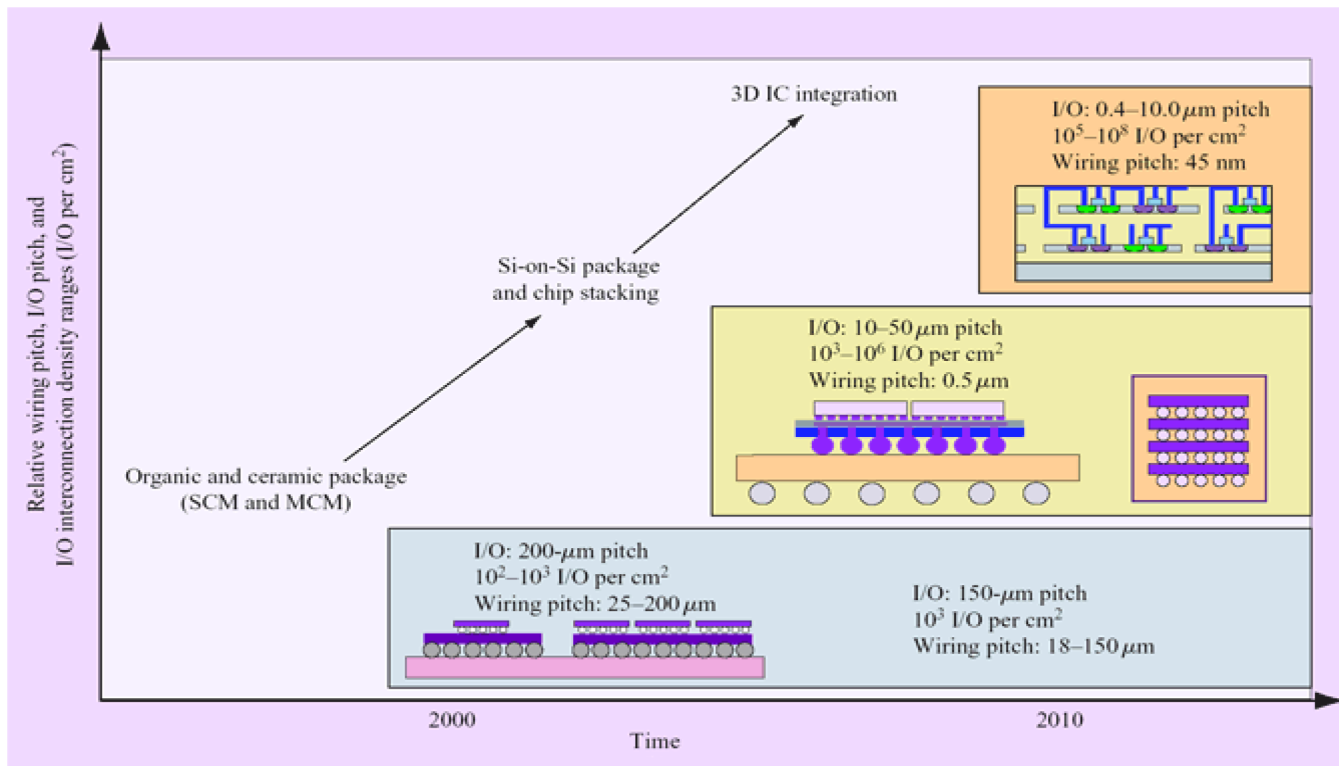


Source IBM http://www.research.ibm.com/journal/rd/526/knickerbocker.html

- **Moore's law by scaling conventional CMOS involves huge investments.**

- **3D IC processes : An opportunity for another path towards continuing the scaling, involving less investments.**

- **Like for conventional CMOS, infrastructures are needed to promote 3D-IC integration, making it available for prototyping at "reasonable" costs.**

3D-IC Integration : Not a New Story

Akasaka, Y., and Nishimura, T., "Concept and Basic Technologies for 3-D IC Structure“ IEEE Proceedings of International Electron Devices Meetings, Vo. 32, **1986**, pp. 488-491.

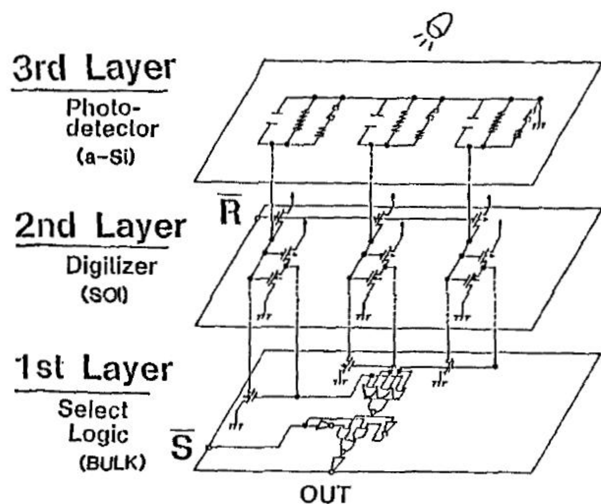


Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

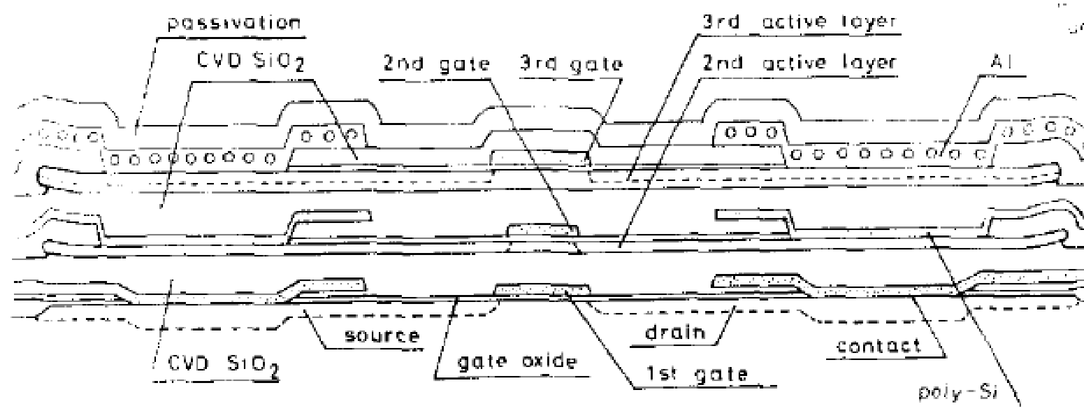


Fig.4 SEM cross sectional photograph and schematic drawing of planarized tripply-stacked IC structure.

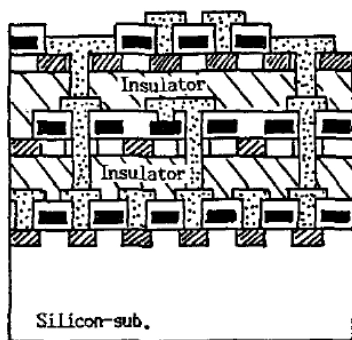
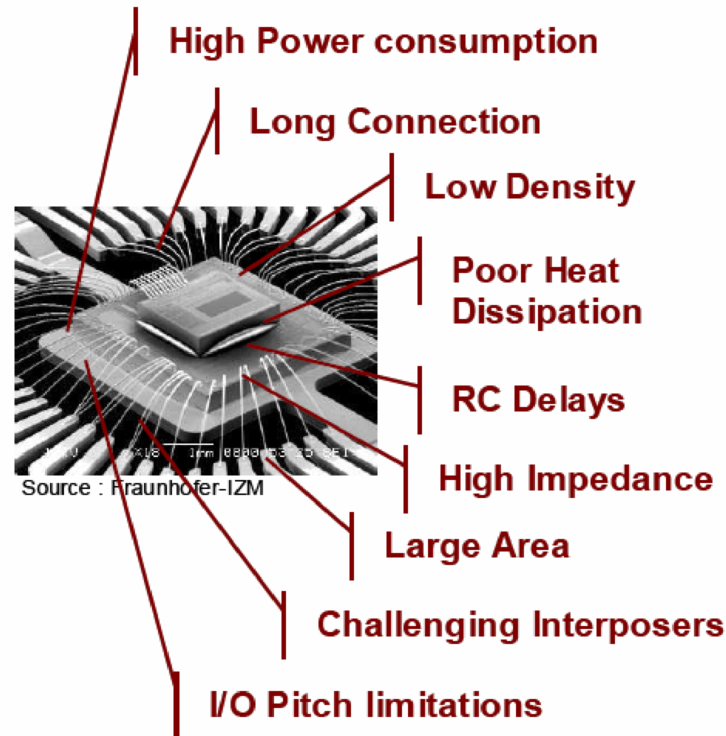


Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

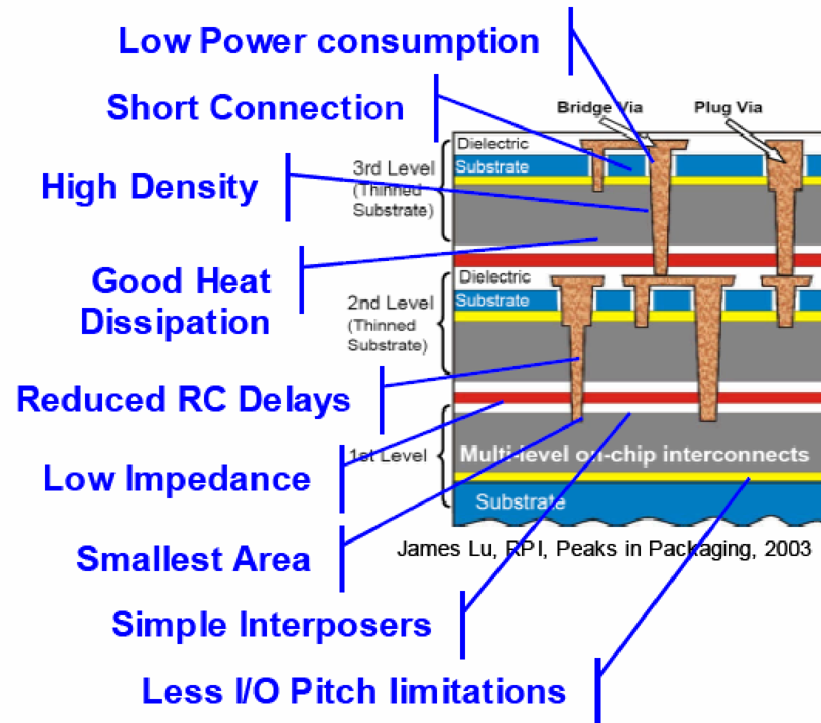
SiP versus 3D-IC

Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



Source : Fraunhofer-IZM



James Lu, RPI, Peaks in Packaging, 2003

TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

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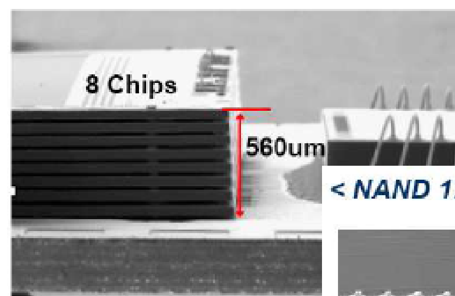
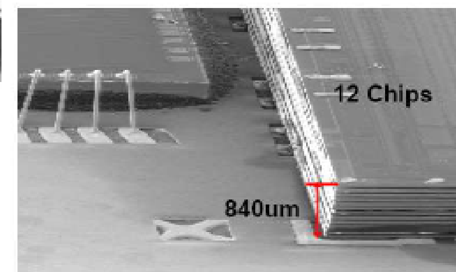
Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
  - Stacked memory chips and memory on CPU
    - IBM expected to provide samples later this year
    - Both IBM and Samsung could be in production next year (2008)
  - Imaging arrays (pixelated devices)
    - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix
    - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

< NAND 8 Stacked Memory Card >

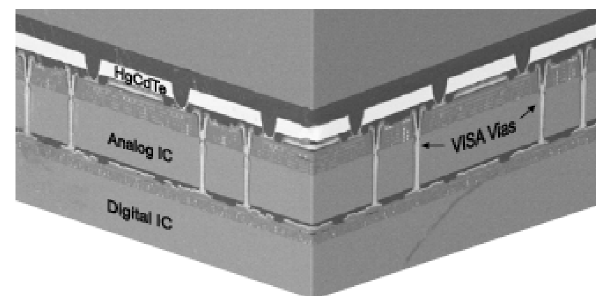


< NAND 12 Stacked Memory Card >



Samsung – 30 um laser drilled vias in 70um chips

RTI Infrared Imager



LHC-ILC Workshop on 3D Integration Techniques

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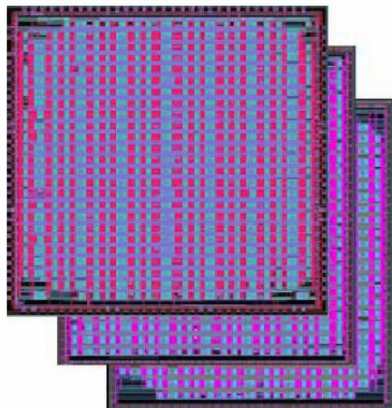
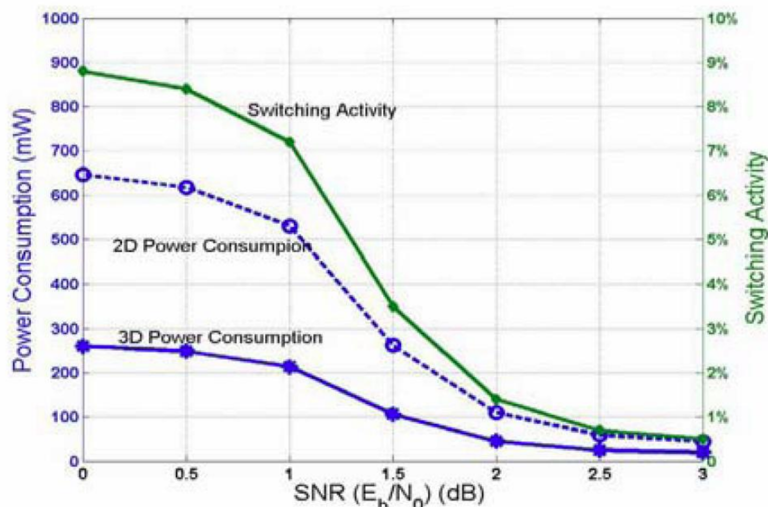
Large Systems Benefits from 3D-IC Integration

"Implementing a 2-Gbs 1024-bit ½-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits"
Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrajarng, Bo Hu, and C.-J. Richard Shi
University of Washington
International Conference on Computer Design, ICCD, Oct. 2007



Final layout view of 3D LDPC structure.



Post-layout power of the LDPC decoder (2D vs 3D).

Comparison between 3D and 2D designs

	2D design	3D design
Area (mm*mm)	18.238*15.92 =**290.35**	(6.4*6.227)*3 = **119.56**
Total wire length (m)	**182.42**	22.39+22.57+22.46 =**67.42**
Max WL before buffer insertion (mm)	**13.82**	**8.68**
Max WL after buffer insertion (mm)	**4**	**4**
Buffer used	**32900**	**24636**
Clock skew (ns)	**2.33**	**1**
Power dissipation (mw)	**646.2**	**260.2**

Performance Factor (Area * Timing * Power) = 14

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CMC-CMP-MOSIS partnering on 3D-IC

CMP/CMC/MOSIS partner to introduce a 3D-IC process

Grenoble, France, 22 June 2010, CMP/CMC/MOSIS are partnering to offer a 3D-IC MPW service based on Tezzaron's SuperContact technology and GLOBALFOUNDRIES 130nm CMOS.

The first MPW run is targeting January 2011:

- 2-tier face-to-face bonded wafers
- 130nm CMOS process for both tiers
- Top tier exposing TSV and backside metal pads for wire bonding.

A design-kit supporting 3D-IC design with standard-cells and IO libraries is available.

Further MPW runs will be scheduled supporting process flavors (multiple tiers beyond 2, different CMOS flavors for different tiers, ...) driven by user requirements.

Potential users are encouraged to contact **CMP** for details : **cmp@imag.fr**

CMC / CMP / MOSIS partnering for 3D-IC process access

- **Stimulate the activity by sharing the expenses for manufacturing.**

- **Join forces for the technical support, and dedicate the roles for each partner.**

- **Make easier the tech support for local users respectively by each local center.**

- **Because there is no standard for the 3D-IC integration, it is urgent to setup an infrastructure making possible a broad adoption of 3D-ICs. That will have a beneficial effect on prices, more frequent MPW runs, and more skilled engineers.**

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CMC - CMP - MOSIS Cooperation

- All 3 in contact with TEZZARON to offer MPW runs service

- New users are presently accessing to the process.

- Roles of each partner :
  - MOSIS is the main contractor with Tezzaron.
  - MOSIS will cluster reticles.
  - CMP is the technical support center.
  - All three address their respective regions for the access to the process and the local technical support.

- Target a First MPW run in March 2011.

CMC - CMP - MOSIS Cooperation

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- CMC supporting Canadian Customers
- CMP supporting European Customers
- MOSIS supporting US Customers
- Each may support other locations

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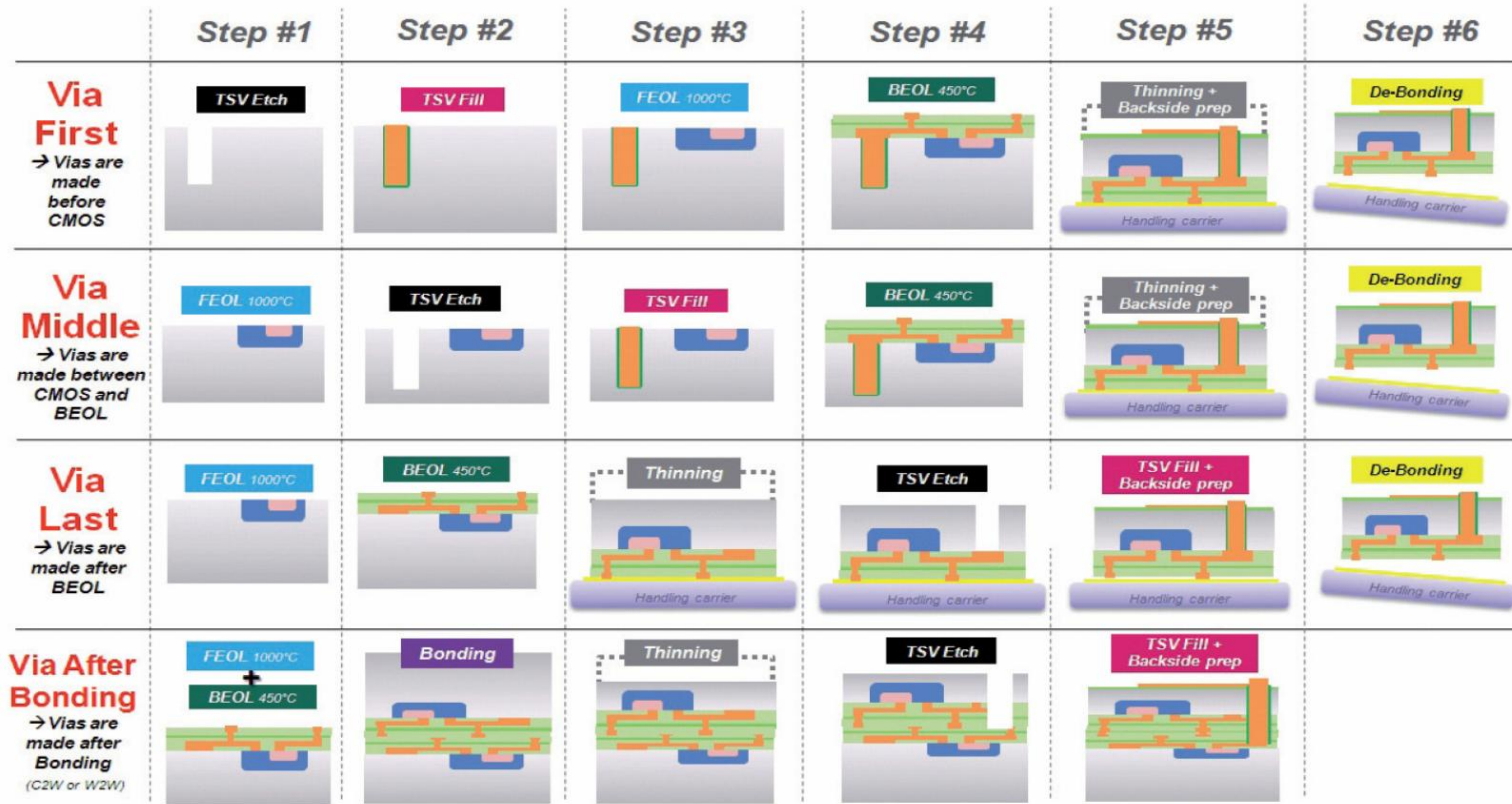
3D TSV via integration MAIN scenarios

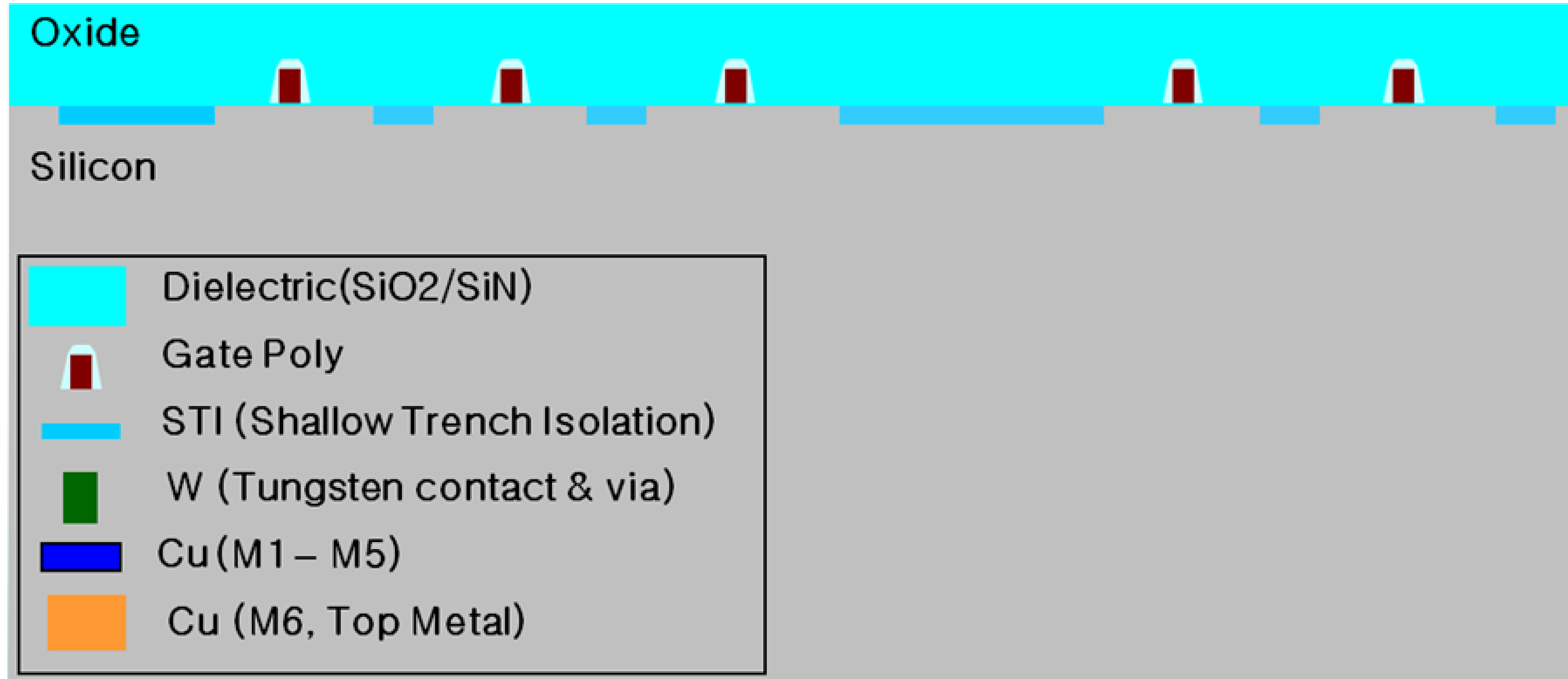


Source Yole Development

Interconnection Technologies

Interconnection Type	Line Width (µm)	Line Thickness (µm)	Line Resistance (Ohm/cm)	Max Length (cm)
Direct Bond Interface (DBI)	2-100	2-100	0	0
Through Si Via (TSV)	1.2-100	1.2-100	500-1000	5-100
On-Chip	0.1-2	0.1-2	100-1000	0.1-1.5
Thin-film	10-25	5-8	1.25-4	20-45
Ceramic	75-100	16-25	0.4-0.7	20-50
Printed Circuit Board	60-100	30-50	0.06-0.08	40-70
Shielded Cables	100-450	35-450	0.0013-0.033	150-500

Tezzaron Process Flow for TSV and DBI (using Via Middle process)



Starting wafer in 130nm (5 Cu metal layers + 6th Cu metal as BDI)

Tezzaron Process Flow for TSV and DBI (using Via Middle process)

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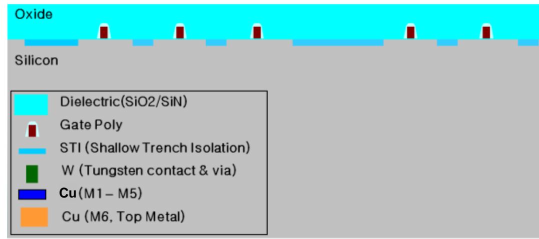
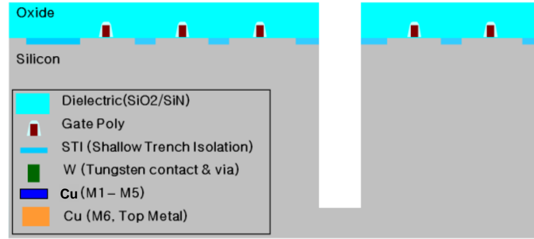
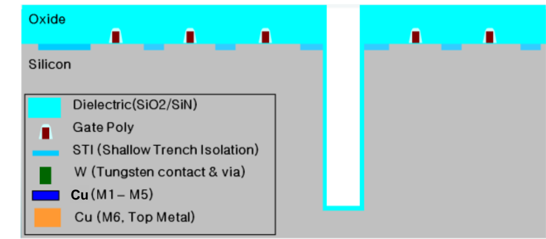
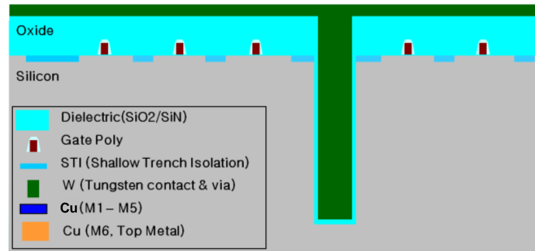
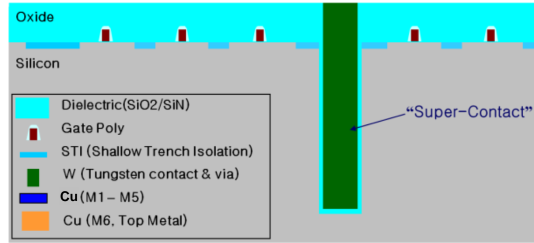
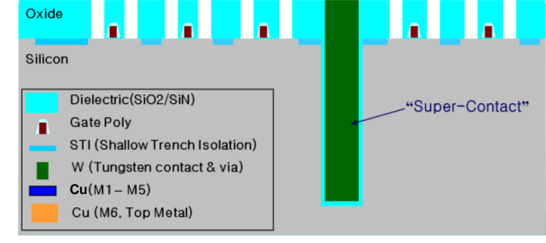


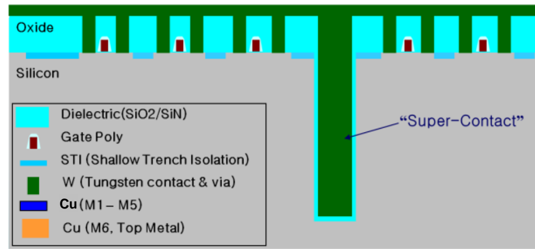


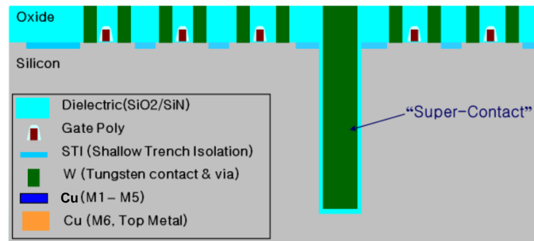


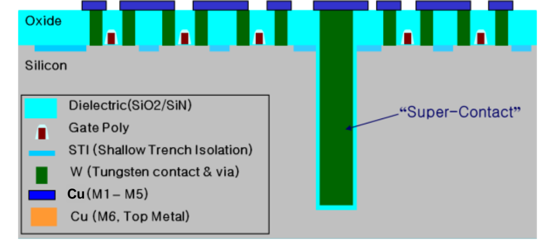


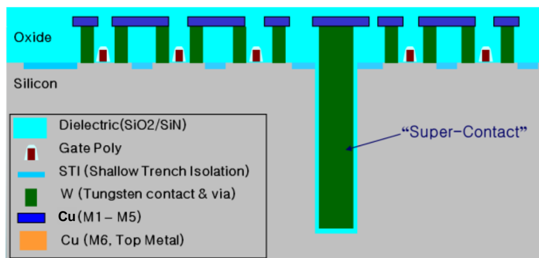


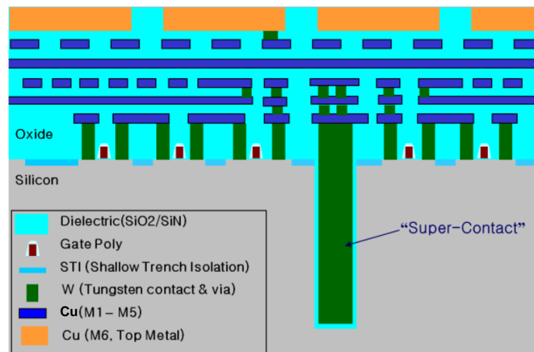




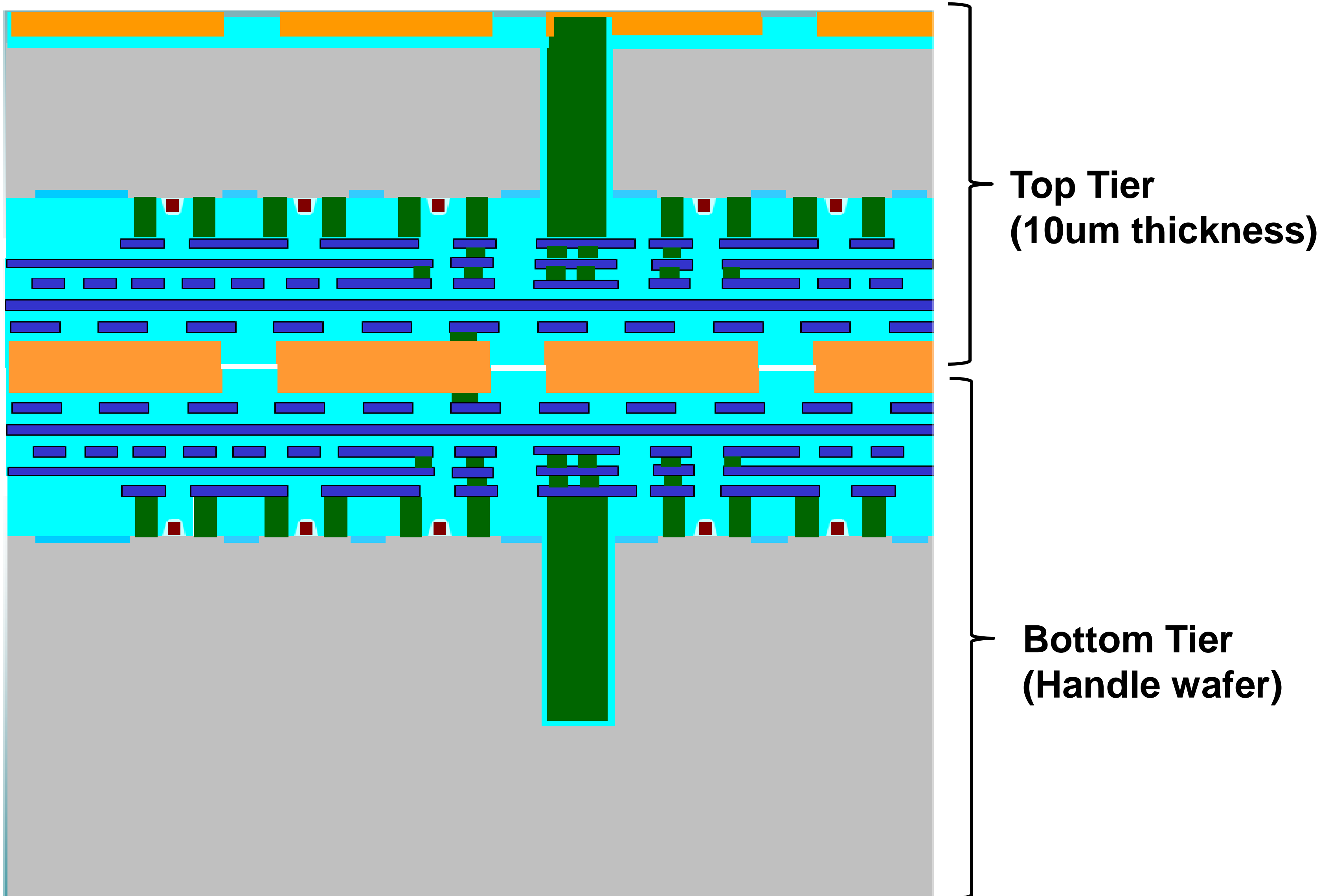






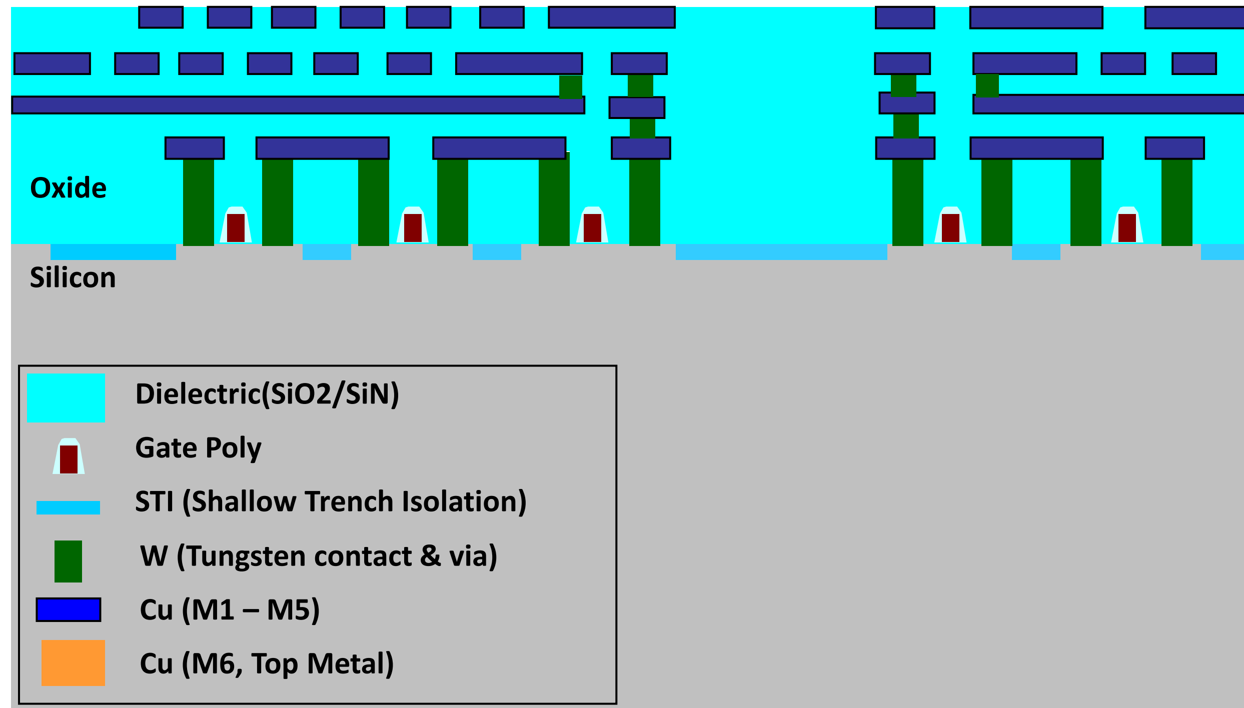


Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)



New Tezzaron Process Flow using "Near End of Line" TSV

Starting wafer in 130nm stopped at Metal 4



130nm Chartered Low Power
Options: Dual gate 2.5, 1.5V
TSV enabled
Deep Nwell
Lvt implant
6 Cu Metal Layers : 5 usable plus a 6th as BDI
No MIM, No High resist poly

New Tezzaron Process Flow using “Near End of Line” TSV

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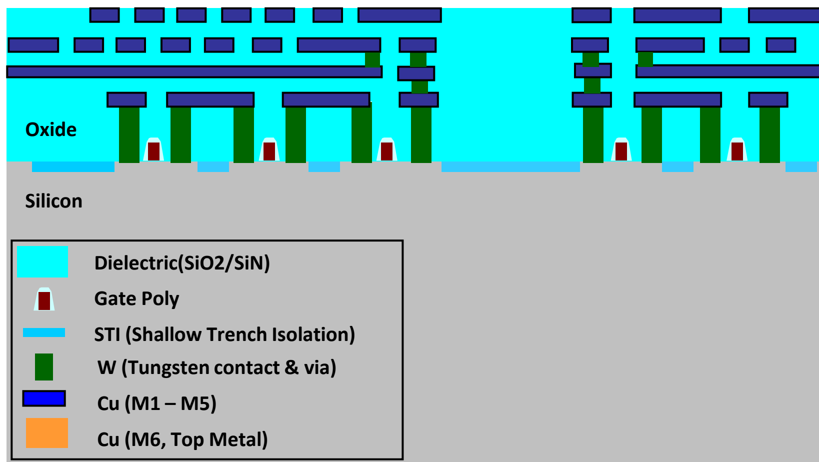
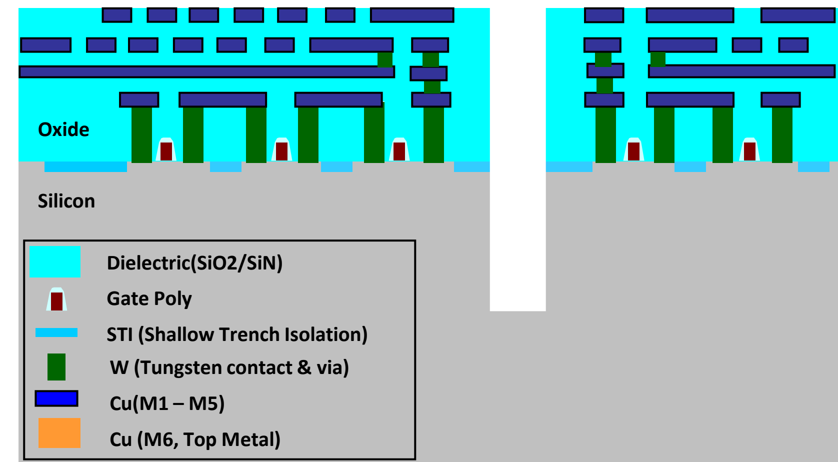
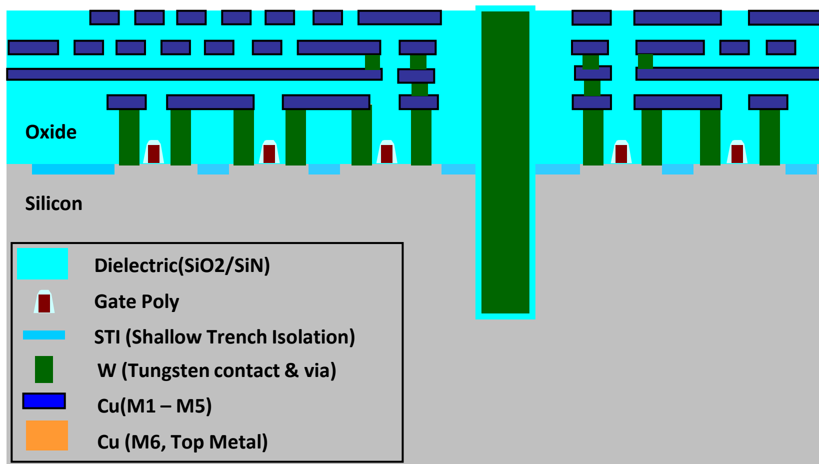


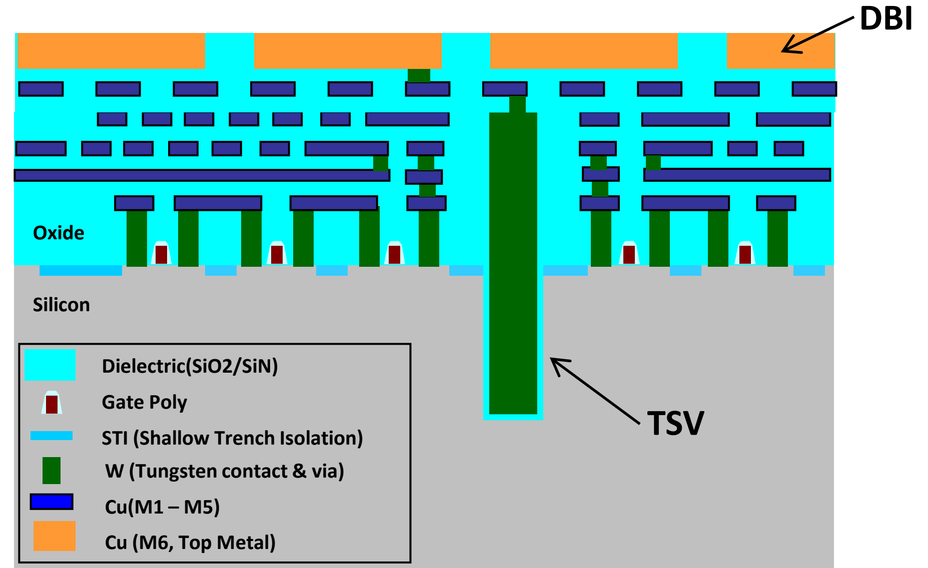
1- Standard CMOS process stopped at MET4



2- Deep etching (DRIE)



3- Dielectric isolation and TSV formation



4- Continue BEOL with Via4 / M5 / Via5 / M6

New Tezzaron Process Flow using "Near End of Line" TSV

DBIs continuing the stacking

Bond pad for wire bonding or bump, flip-chip …

"Near End of Line" versus "Via Middle"

Advantages of "Near End of Line" :

- The process can be done on any wafer from any foundry, provided that BEOL is stopped at Metal 4. The post-process for TSV and DBI is independent from the foundry.
- As a consequence, it allows mixing different process nodes 130nm / 65nm from different foundries, or any combination like assembling SiGe BiCMOS and CMOS.

Disadvantage of "Near End of Line" :

- The access to the TSV is only possible with a Via from Metal5. That makes long paths and serial resistances through the 5 Vias from the MOS to the TSV.

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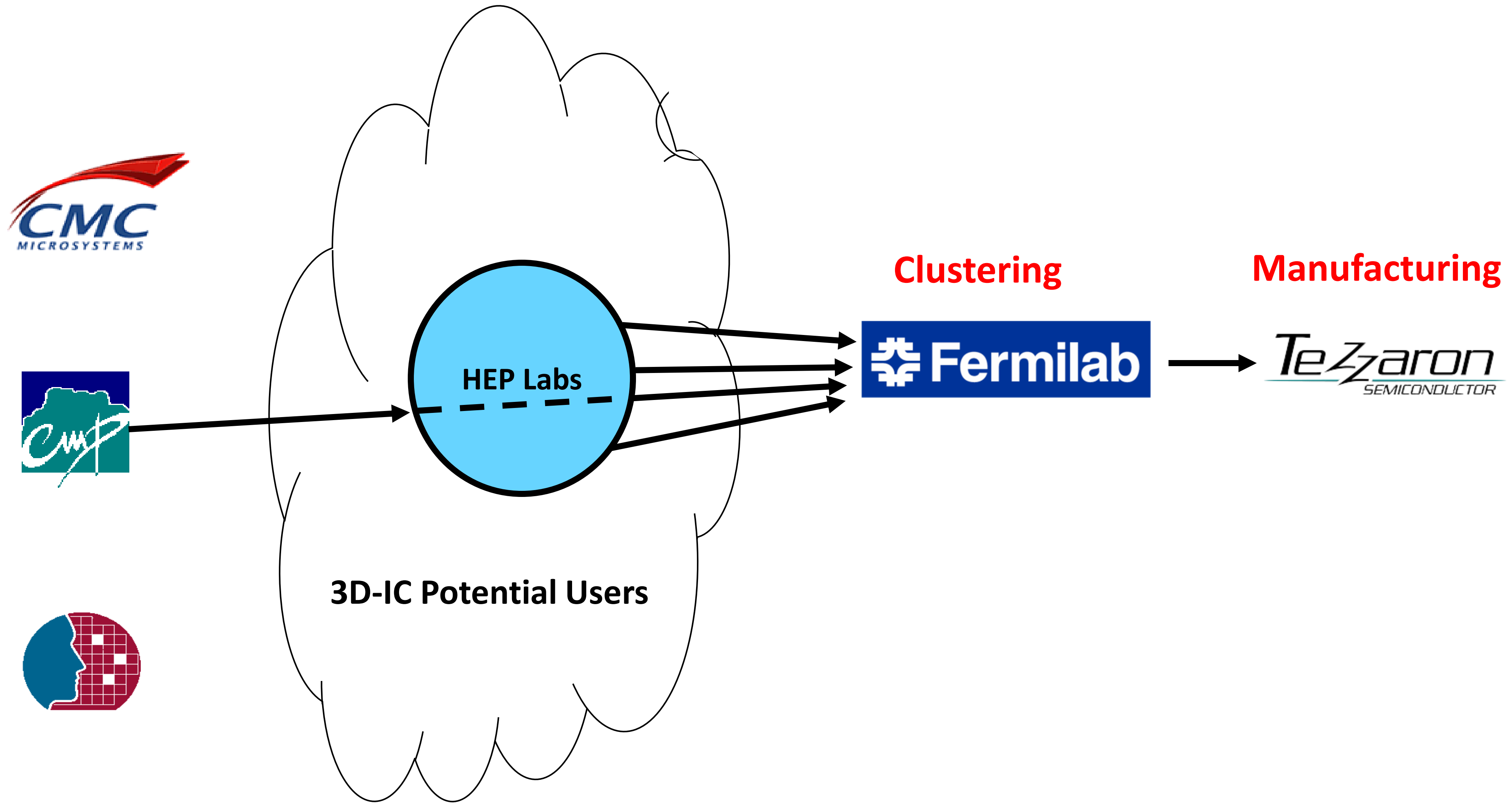
3D-IC MPW Initial Infrastructure

First MPW Run organized by FermiLab using an Industrial Process



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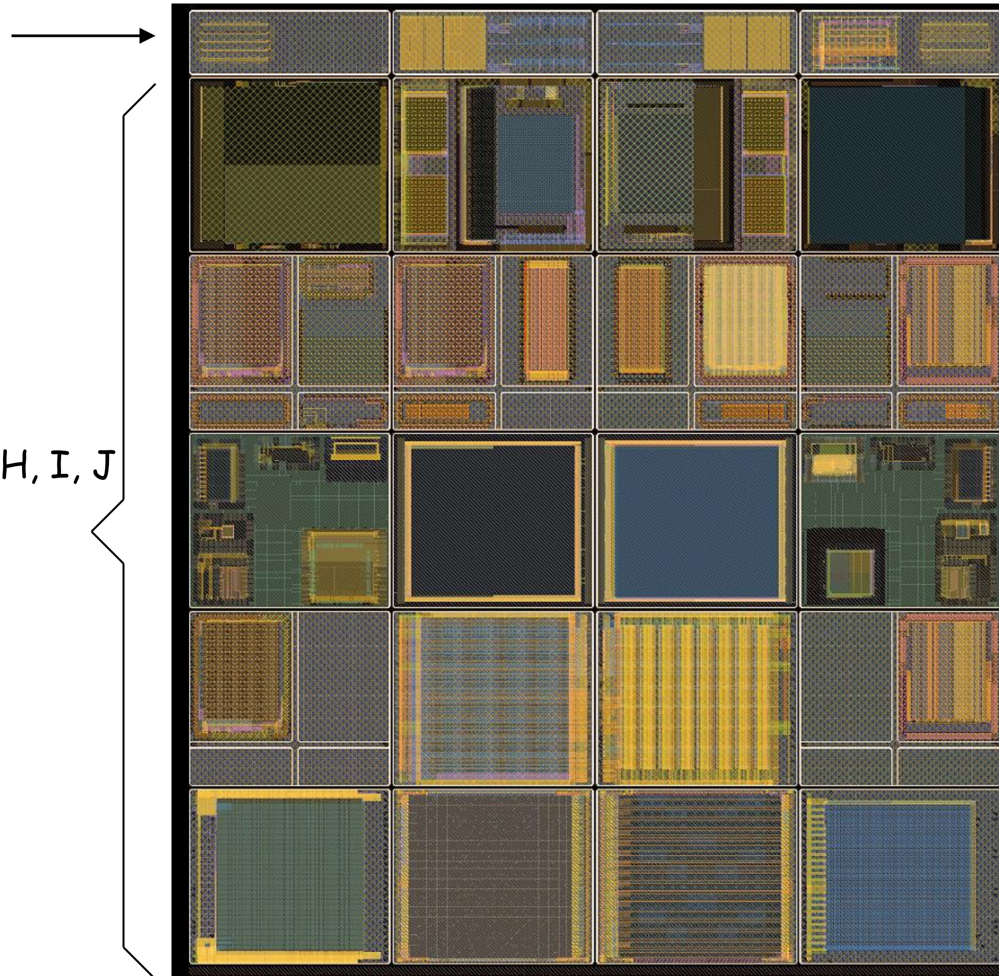
MPW Full Frame

Test chips:
TX, TY
2.0 x 6.3 mm

Subreticules:
A, B, C, D, E, F, G, H, I, J
5.5 x 6.3 mm

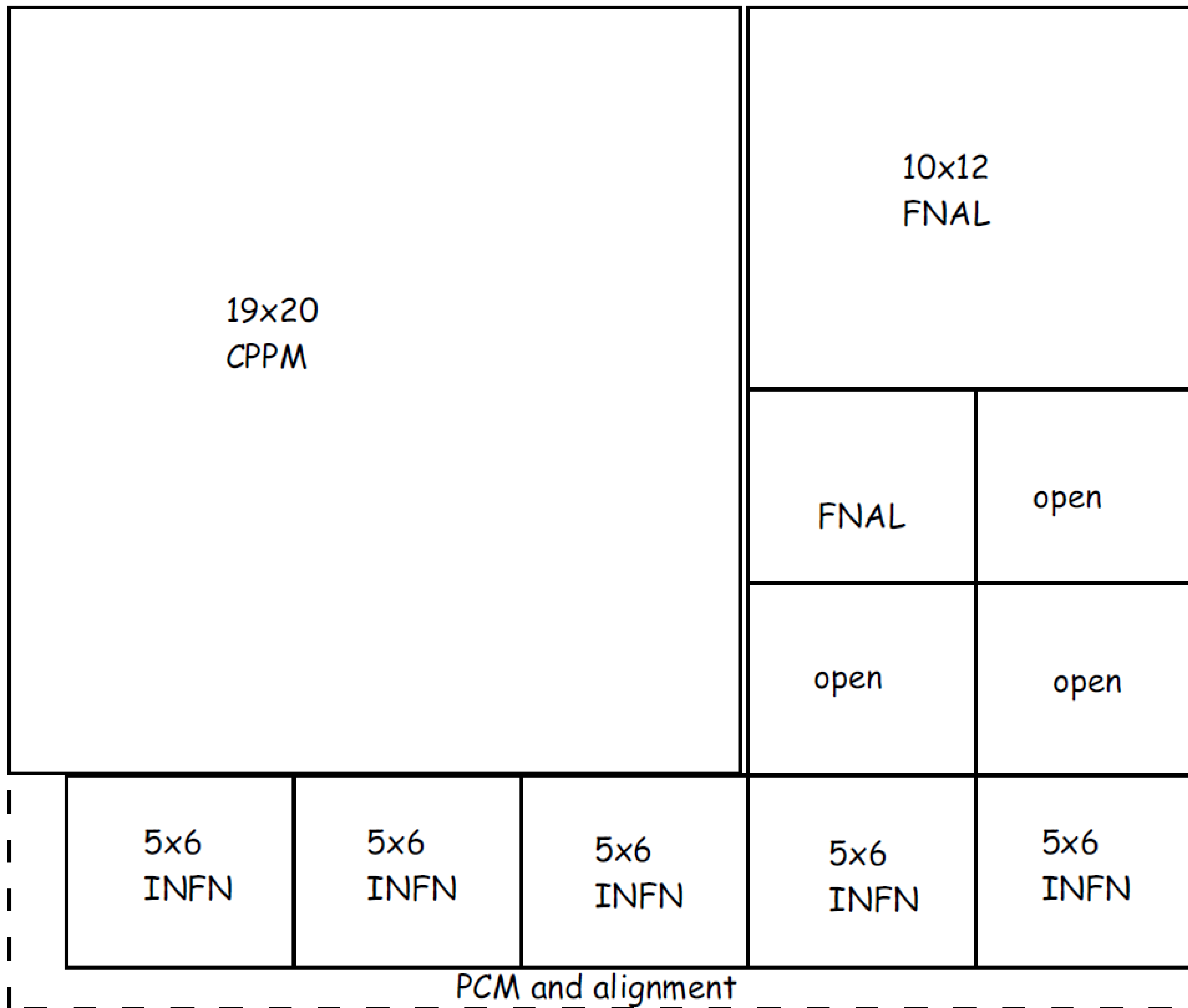


Notice Symmetry about vertical center line

Top tiers — Bottom Tiers

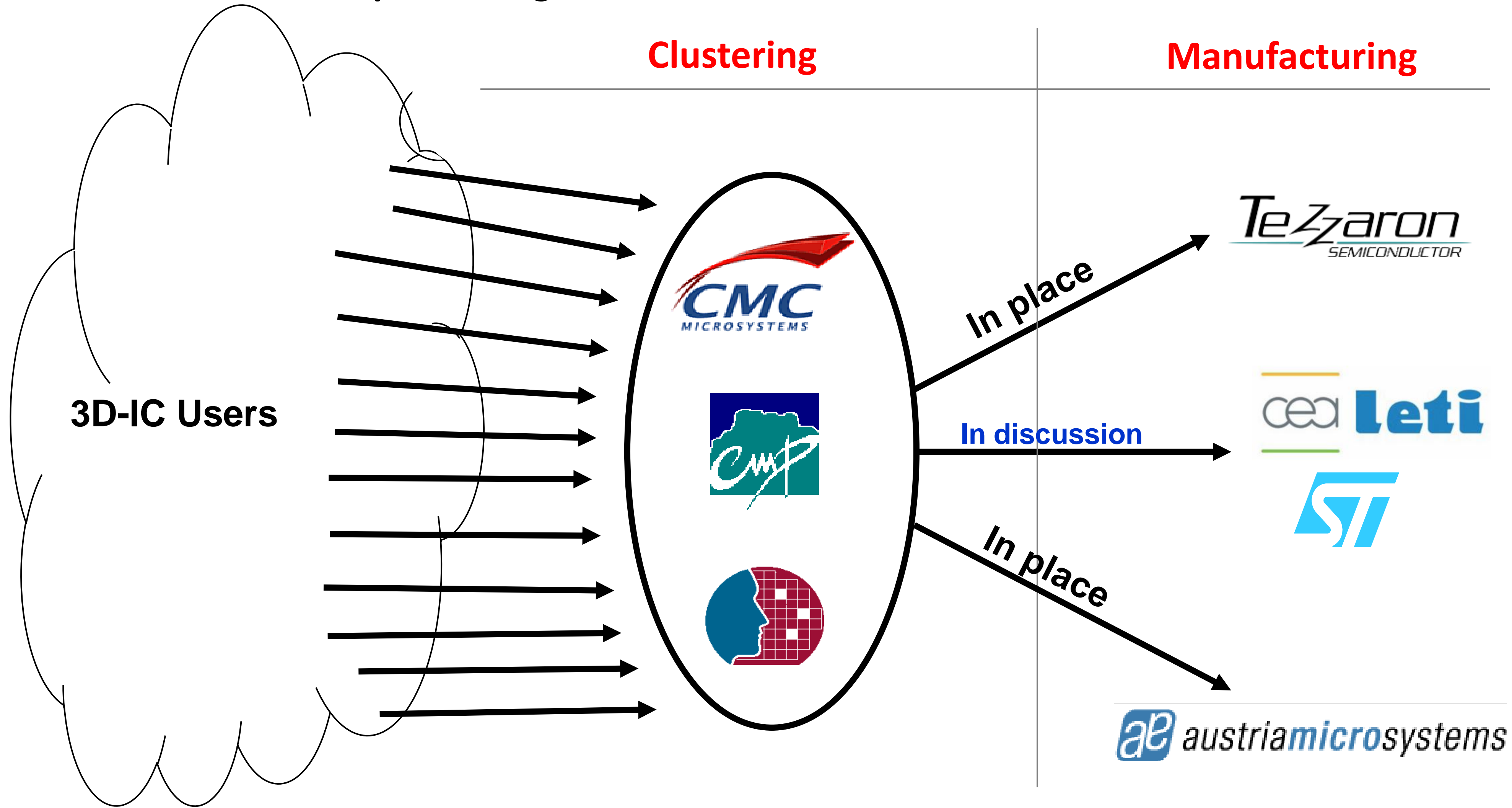
Source FermiLab (3D Consortium Meeting)

3D Consortium : 2nd MPW run Planned for March 2011



3D-IC MPW Infrastructure

CMC-CMP-MOSIS partnering to offer 3D-IC MPW runs



Critical mass will allow frequent MPW runs and low pricing

CMC-CMP-MOSIS : 1st MPW run Planned March 2011

Tezzaron Targets

Block 1 = 12.69 x 15.19 mm^2
Block 2 = 12.69 x 15.19 mm^2
Block 3 = 12.69 x 15.19 mm^2
Block 4 = 12.69 x 15.19 mm^2

0,0 is lower left corner for all blocks

All outer scribe lanes are 80um wide

Block 1

Block 2

Block 3

Block 4

160um

160um

Available for Chartered

Available for Chartered

Available for Chartered

30.86mm

25.70mm

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Chartered / Tezzaron Design Platform

- Making a common root installation for the different parts of the Design Platform

  - PDK
  - Libraries
  - Memory compilers
  - Utilities
  - Tutorials

- Defining a unique variable for the root installation.

All the modules inside refer to this unique variable.

Making the Design Platform portable to any site without configuration scripting.
The user need just to define the path to this variable.

Chartered / Tezzaron Design Platform (continued)

- The PDK has been revisited organizing its content.
  - Organize the different modules by tools
  - Redefine the Cadence IC configuration files to include missing features
  - Correcting some definitions (libInit.il)
  - Reorganize the utilities
  - Choice between different layers palettes.

- Unify the cellviews inside a single database (CDB format)

(can be done the same way when the OpenAcess data format will be available)

- Define setup files pointing to the libraries :
  - For Cadence DFII + Mentor/Calibre
  - For Synopsys Design Compiler
  - For Encounter Place & Route tools.

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Chartered / Tezzaron Design Platform (continued)

TDP_2010q2v1 : Tezzaron Design Platform

CSM013LP_LVT_SC_2007q2v1 : Chartered LP LVT Core cells
CSM013LP_SC_2005q1v1 : Chartered LP standard VT Core cells
CSM013_IO_GP_IL_2005q3v2 : Chartered In Line IO cells
CSM013_IO_GP_ST_2005q2v1 : Chartered In Line IO cells
CSM013_MEM_COMPILERS : Chartered Memory compilers
MMI_PDK_I : MicroMagic PDK part I
MMI_PDK_II : MicroMagic PDK part II
README_NCSU
UTILITIES_2010q2v1 : Utilities provided by the community
chrt13lprf_DK009_Rev_1C_TSC_1C : Chartered/Tezzaron PDK
Doc : Documentation
Install : Installation utilities and setup environments
tutorials : Here comes the different design-flows tutorials

PDK (Process Design-Kit) structure

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chrt13lprf_DK009_Rev_1C_TSC_1C : Chartered PDK including Tezarron layers

Chartered.013lp.ReleaseNotes
Chartered.013rf.ReleaseNotes
MapTables : layers map tables : Encounter / ARM libs
assura : QRC extraction / Dummies filling program
Calibre : 3DDRC / 3DLVS / Dummies filling
chrt013lp : Technology library + devices (active & passive)
chrt013rf : Complementary library with RF devices
doc : Documentations : Design-rules / design guides (Chrtrd + Tezzaron)
eldo : Model files for Eldo
hspice : Model files for Hspice
skill : Skill routines for 3D LVS
spectre : Model file for Spectre
src : C program fro NCSU preprocessing for 3D LVS.

Libraries structure

Each Library of standard-cells or IO pads is organized as follows :

README.copyright
README.csm013lp-lvt_sc-x2_2007q2v1
README.fe_license
apollo : Synopsys backend views for P&R
cds_cdb : Cadence database with all cellviews
cds_oa : Cadence OpenAcess format with all cellviews
cell_list
doc : Documentation
edif : Edif format for symbols
gds2 : Physical layouts in GDSII format
lef : LEF format for P&R
lvs_netlist : CDL netlists for LVS
primetime : Perl script backannotation for Primetime
synopsys : Frontend and Backend libraries for Synopsys Digital Flow
verilog : Verilog libraries
vhdl : VHDL libraries

Developments & Contributions to the Design Platform

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HEP contributing Programs, Libraries, and Utilities have been included in the Design Platform

DBI (direct bonding interface) cells library. (provided by FermiLab)

3DPad template compatible with the ARM IO lib. (provided by IPHC)

Preprocessor for 3D LVS / Calibre (provided by NCSU)

Skill program to generate an array of labels (provided by IPHC)

Calibre 3D DRC (provided by Univ. of Bonn)

Dummies filling generator under Assura (provided by CMP)

Basic logic cells and IO pads (provided by FermiLab)

Floor-planning / automatic Place & Route using DBIs, and TSVs (provided by CMP)

Skill program generating automatically sealrings and scribes (provided by FermiLab)

MicroMagic PDK (provided by Tezzaron/NCSU)

Virtuoso Layout Editor with 3D layers and verification

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TSV

Back Metal

Back Pad

DBI

NO_FILL drw
TSCSuperCnt drw
TSCBackMet0 drw
TSCBackMet0 lbl
TSCBackMet1 drw
TSCBackMet1 lbl
TSCBPad drw
SRAM_TSC drw
PR_BNDRY drw
NWELL drw
DNWELL drw
LDMOS_XTOR mar
COMP drw
POLY2 drw
POLY2 lbl
PPLUS drw
NPLUS drw
CNT drw
MET1 drw
MET1 lbl
VIA1 drw
MET2 drw
MET2 lbl
VIA2 drw
MET3 drw
MET3 lbl
VIA3 drw
MET4 drw
MET4 lbl
VIA4 drw
MET5 drw
MET5 lbl
VIATOP drw
METTOP drw

X: 12.500 Y: -4.115 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 2

Tools Design Window Create Edit Verify Connectivity Options Routing Assura Calibre Help

Calibre Integration

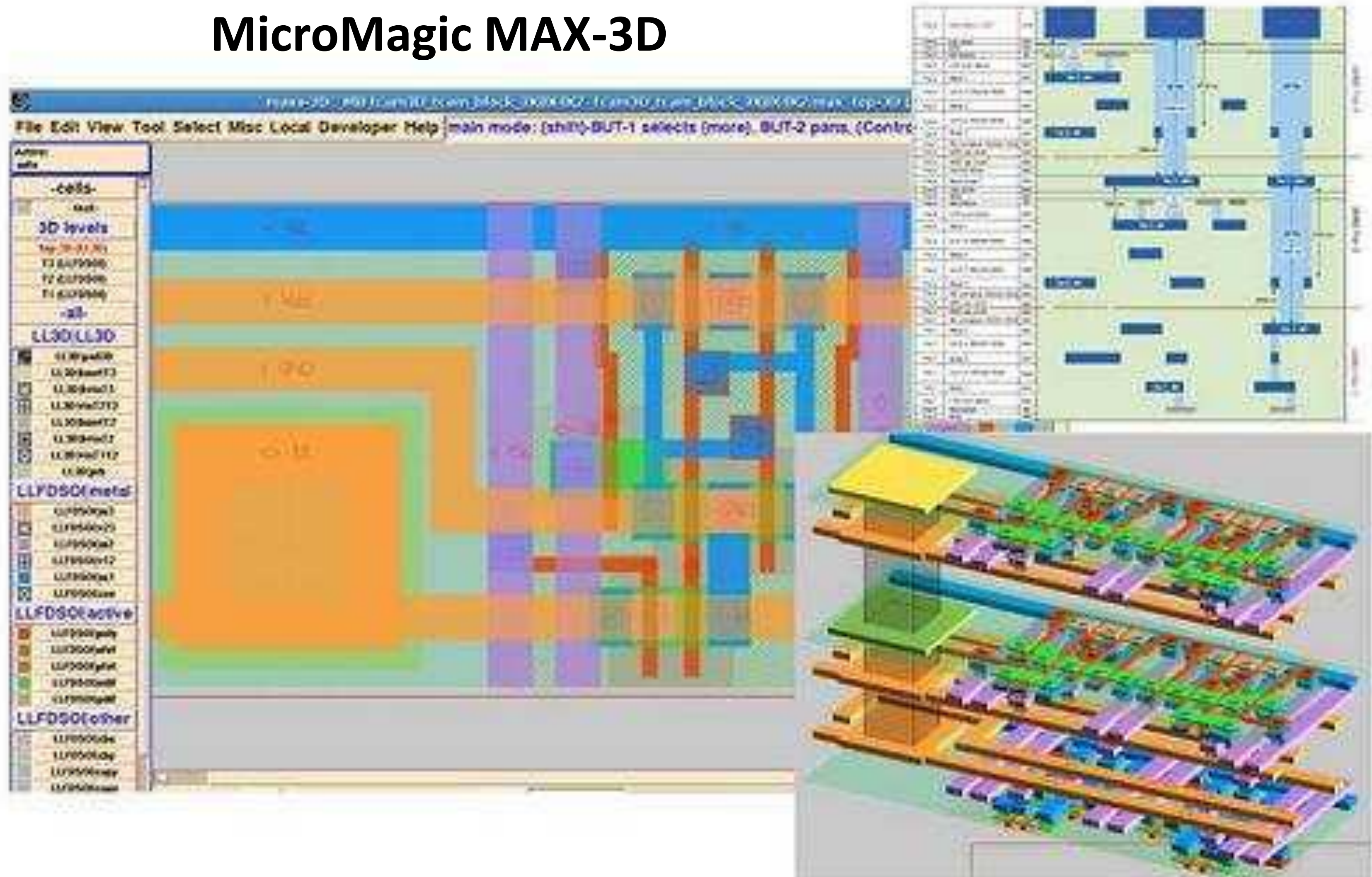
Assura

mouse L: mouseSingleSelectPt M: leHiMousePopUp() R:hiZoomAbsoluteScale(hiGetCurrentWi

True 3D Mask Layout Editor

Technology Files fully supported by Tezzaron

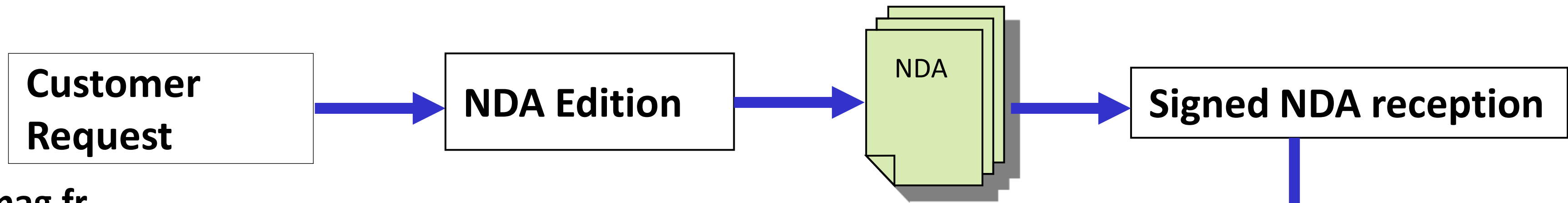
MicroMagic MAX-3D



Generate Animated 3D Layouts From Virtuoso

Should we develop an interface to generate VRML descriptions from Virtuoso Layout ?

Access to the Design-Rules and the Design Platform



http://cmp.imag.fr

Request to access from CMP Web page or by E-mail to :

cmp@imag.fr

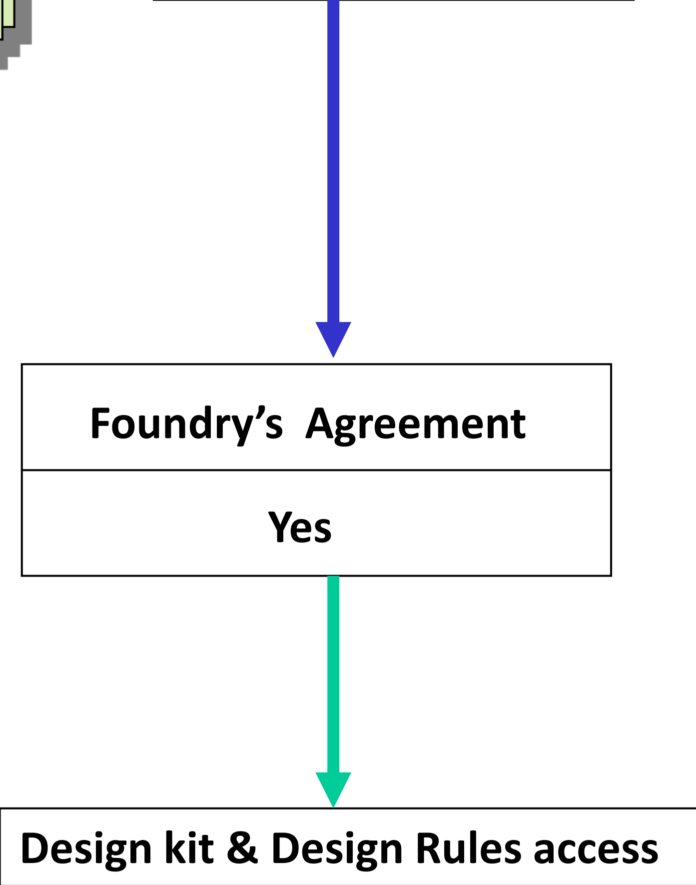
The user receive by E-mail the NDA + ARM lirary Addendum.

The user sign and return by post 2 original signed copies

CMP forward to Tezzaron the NDAs.

When Tezzaron is OK, they counter-sign and return one copy to CMP.

CMP return the copy to the user and give the access to the DRM and Design-Platform.



Users having access to the Design Platform

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CPPM, Marseille
IPHC, Strasbourg
LAL, Orsay
LPNHE, Paris
IRFU, CEA Saclay
LAPP, Annecy-Le-Vieux *
ENSTA PARISTECH, Paris *

France

INFN, Roma
INFN, Pavia
INFN, Pisa
University of Bologna *
University of Perugia

Italy

University of Bonn, Germany

University of Barcelona, Spain
IMSE-CNM-CSIC, Sevilla, Spain

University of Turku, Finland

Acreo AB, Norrköping, Sweden

Norwegian University, Trondheim, Norway

Monash University, Clayton, Australia

New Users

19 Users in Europe

Tezzaron Semiconductor, USA

FermiLab, USA

North Carolina State University, USA

MOSIS, USA
CMC Microsystems, Canada

University of Sherbrooke, Canada

+ Other centers supported by MOSIS and CMC
Not listed here.

Agenda

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- Introduction
- Motivations for 3D-IC Integration
- CMC-CMP-MOSIS partnering on 3D-IC
- Process Overview
- MPW runs
- Design Platform features for 3D-IC
- **3D-IC automatic Place & Route**
- Conclusion

Automatic P&R with DBI and TSV

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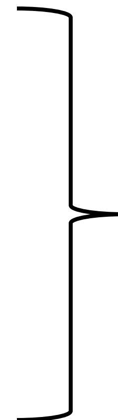
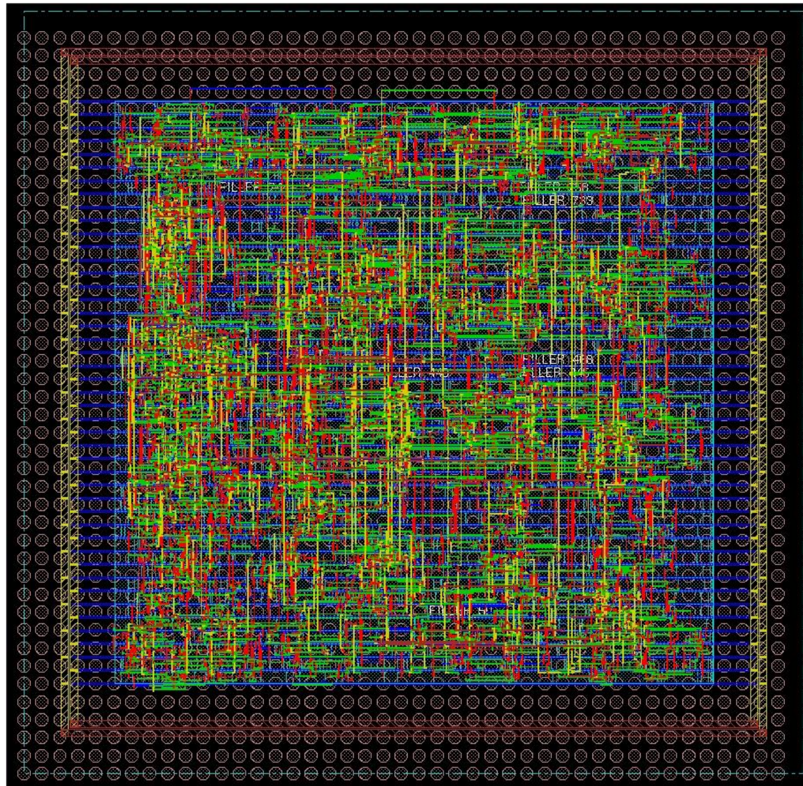
Step	Description
System Level Partitioning	Design exploration at system level
3D Floor-Planning DBI, TSV, IO placement	Design exploration at the physical level DBI, TSV, and IO placement & optimization
Automatic Place & Route	Cells and blocks place & route can be done tier by tier
Extraction, Timing Analysis	To be done for each tier, then combined for backannotation to the 3D top level system
Physical verification 3D DRC, 3D LVS	
Dummies Filling	
Final 3D DRC	



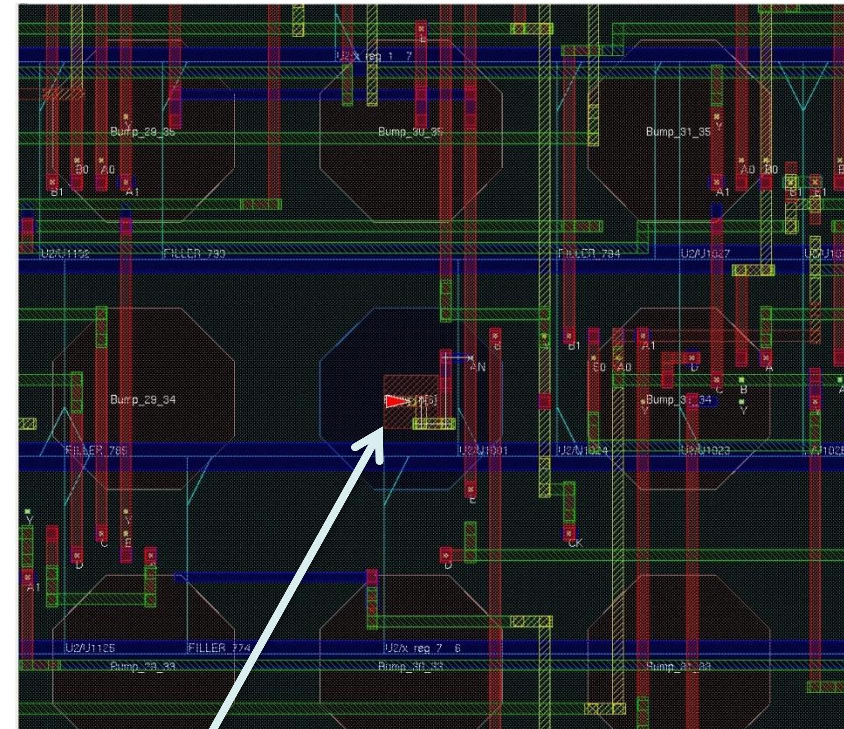
Similar to the full-custom design flow

Using Cadence / Encounter for automatic P&R with Direct Bond Interface

- Encounter natively refuses to make the routing for pins on DBIs.
- A custom script solved the problem. It's a workaround.
- The resulting layout is compliant to the Tezzaron DRC, LVS etc …



DBI array generation + P&R

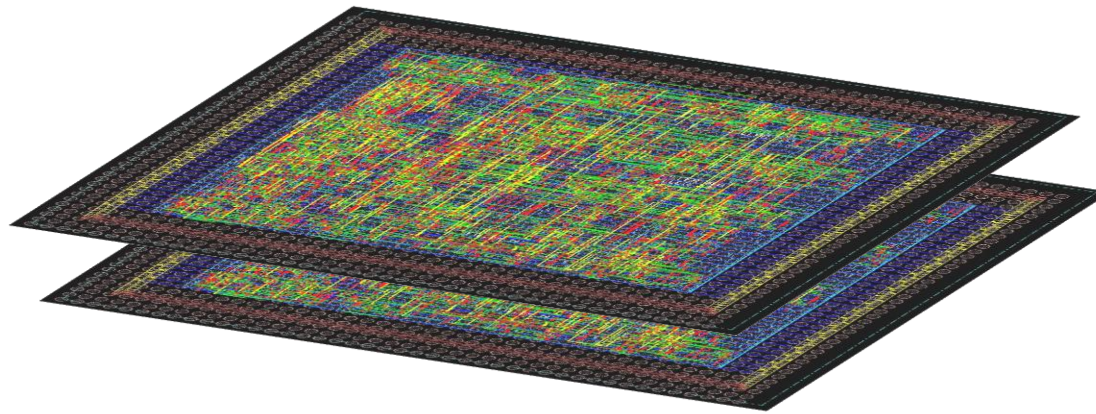


DBI completely routed through the lower metal layers

Using Cadence / Encounter for automatic P&R with Bond Interface

Saving the floor plan for the bottom tier, and apply it for top tier so the automatic Place & Route run the placement and routing taking into account the DBI locations.

The place & route for both tiers is optimal for timing, buffer sizing and power performance.



This should result in a "correct by construction" design.

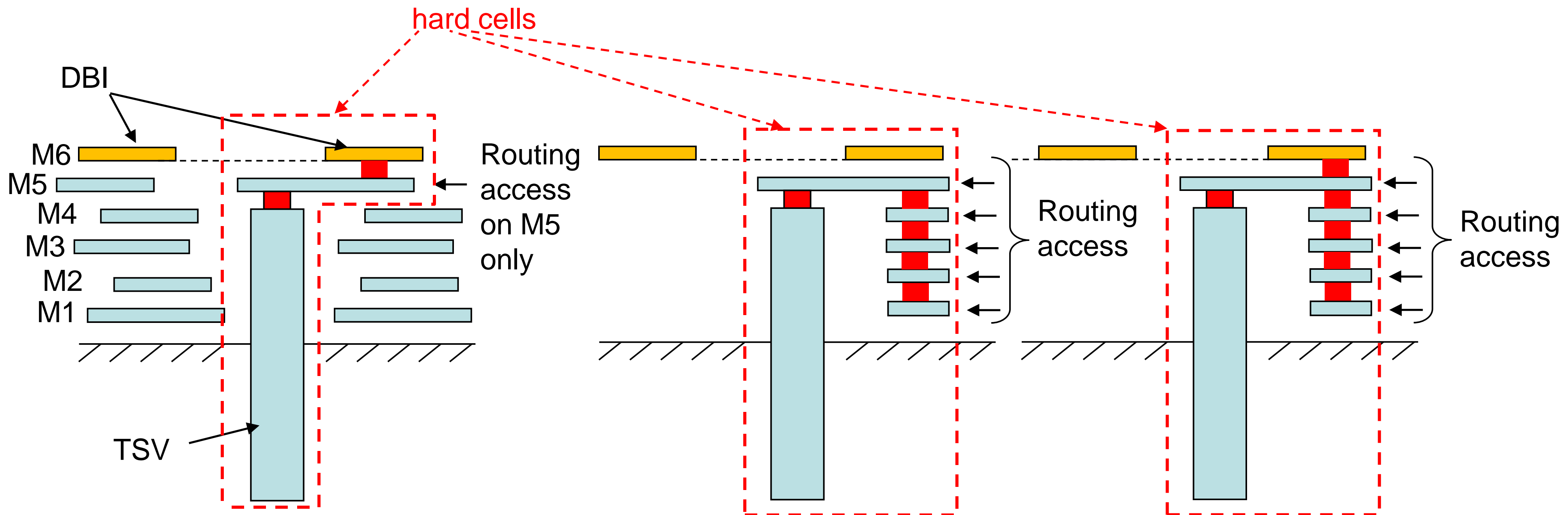
Using Cadence / Encounter for automatic P&R with TSV

3 ways investigated and solved for P&R using TSV :

1) Using a combined TSV / DBI cell allowing a straight vertical routing across the tiers.
Scripting allowing the automatic placement, then P&R is done automatically.
Access is available on M5. The router decides how to make the wiring to the pin. (RDL routing)

2) Using a separated TSV, allowing the router to connect to any of the metal layers (except M6).

3) Using a combined TSV / DBI cell with pins for routing on all metal layers (except M6)

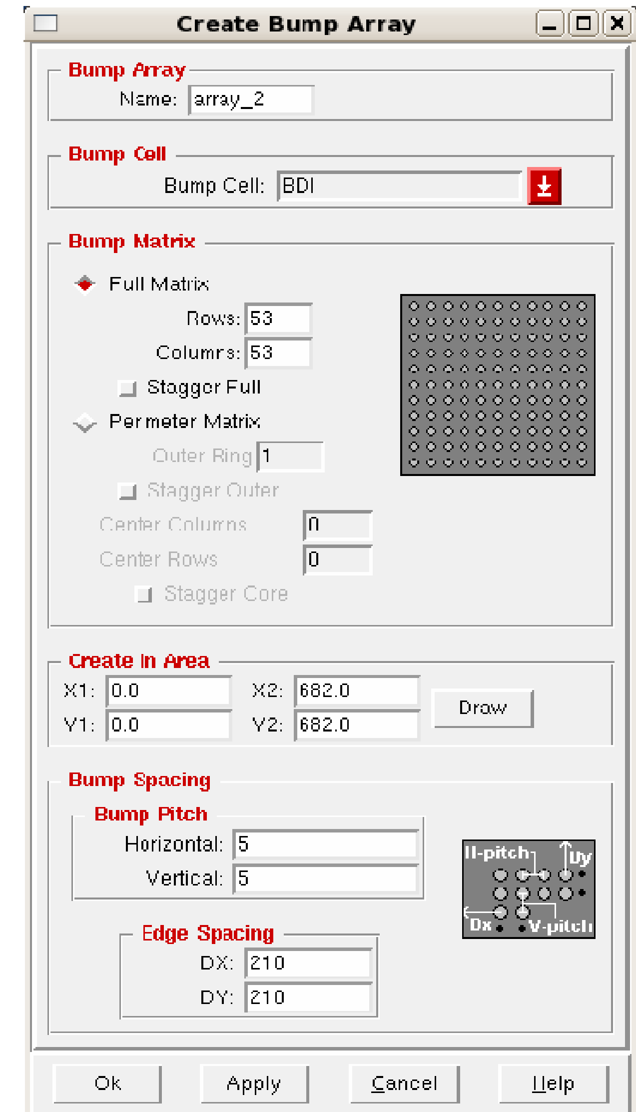


➢ Create Bump Array

Floorplan > Flip Chip > Create bump Array…

Specify the array Name, number of bumps, pitch, …
Then click OK.

To save an IO file with this bump array choose the following menu:
Design > Save > I/O File…



Cadence / Encounter v 8.1 Signal Bumps Assignment

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Floorplan > Flip Chip > Assign Signal…

1. Select the IO signal in the list
2. Select the bump to be assigned
3. Click "Assign". The selected bump become blue.

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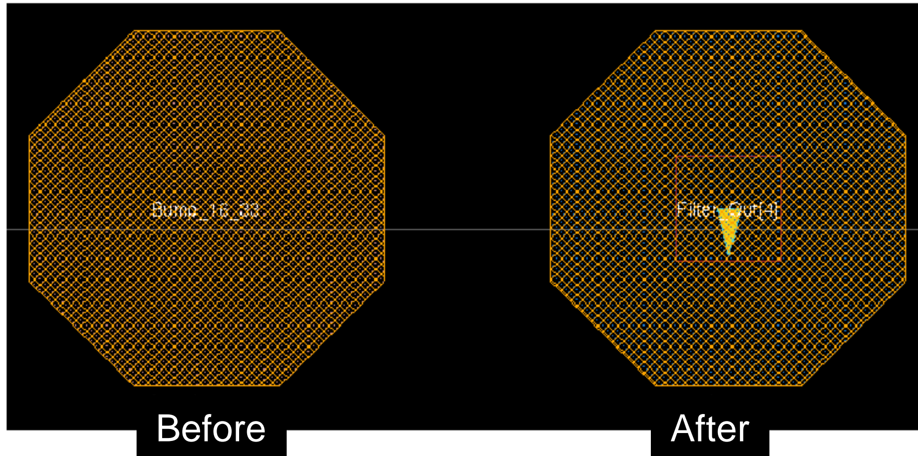
Custom Scripts Enabling Routing on DBIs

Create pins under bumps:

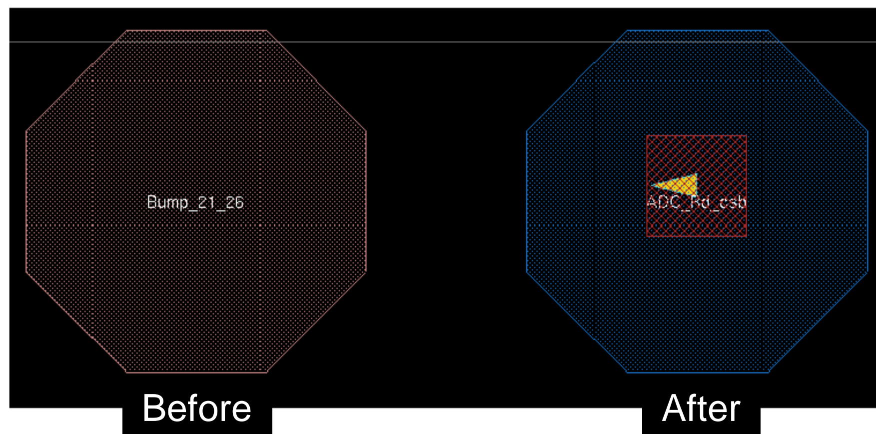
```
exec ../ScriptsBDI/makePhysical_Pins.sed Design_pins_bumps.io makePhyPins.do
```



Placing logical pins on bumps (DBIs), and extract their location.

Generating physical pins under bumps:

source makePhyPins.do
setBumpFixed –allBumps



Generating Physical pins from these locations.
They can now be used as terminals for routing.

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Automatic P & R Design Flow (From Floor-Plan to Routed Design)

- DBIs Placement
- TSVs Placement
- Obstructions on TSVs

- Std cells Placement
- Clock Tree Synthesis

Filler Cells Placement

- Clock routing
- Final routing

Clock and all nets routing is enabled on M1-M5

⚠ **The M6 layer must not be used during routing. This layer is reserved for DBI.**

➢ Routing Clock Nets

Route > NanoRoute > Route…

Switch **Selected Nets Only** in the *Routing Control* panel.

In the **Attribute** Menu, select :
Net Type : **Clock Nets**
Avoid Detour: **True**
(this allows to route the clock nets as straight as possible)

Use the "Mode setup" panel to switch the different options (for example, define the bottom/top routing layer).
Click OK to run Nanoroute.

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Conclusion

CMC, CMP, MOSIS already cooperating since several years offering commonly some processes, and sharing the manufacturing prices. They are engaged this time with the 3D-IC process offer.

A very collaborative work has been achieved and still ongoing between the parties CMC, CMP, MOSIS, FermiLab, Tezzaron, HEP Labs, NCSU.

A Unique and Unprecedented Design Platform resulted from the collaboration. (Industrial CAD vendors just starting addressing the features)

First CMC/CMP/MOSIS MPW run planned for March 2011.

Other 3D-IC processes are explored :

- **CMP is in discussion with Austriamicrosystems for a TSV process for System-in-Package (SiP) applications.**
- **CMP is in discussion with LETI / ST for the access to a 3D-IC process using Cu TSV.**