A Tezzaron-Chartered 3D-IC electronic for SLHC/ATLAS hybrid pixels detectors

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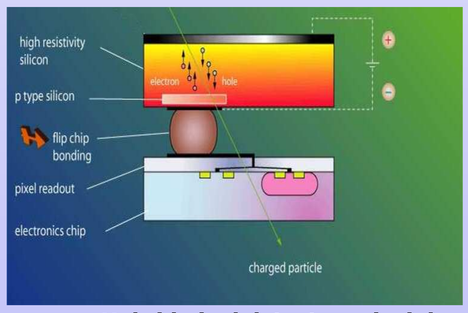
HYBRID PIXEL DETECTORS

Hybrid silicon pixels detectors featuring high spatial resolution, very good signal to noise ratio and true two-dimensional information are currently used as vertex detectors in High Energy Physic experiments and specially in ATLAS and CMS detectors at the Large Hadron Collider (LHC).

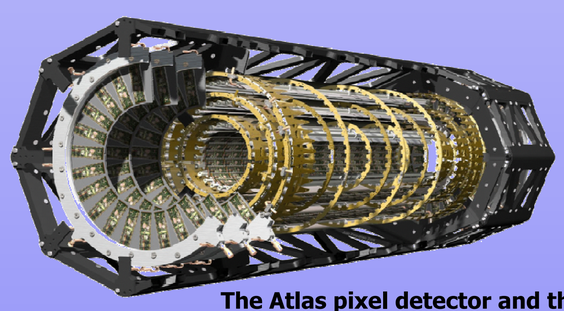


Hybrid pixel detector principle

As they consist in sensors connected by bump-bonding to CMOS read-out circuits, they can be considered already as "3D devices". Thanks to this modularity, the choice of the sensor material (Silicon, 3D Silicon, Diamond, CdTe..) could be driven only by application needs (efficiency, radiation hardness..).

THE ATLAS PIXEL DETECTOR

86 millions of hybrid pixels around the LHC beam pipe, organized in 3 cylindrical layers and 6 disks (end-caps). Pixel dimensions are of 50*400 µm in IBM 0.25 µm technology. If the pixel width is driven by physic requirements, pixel length is mainly imposed by technology limitations



The Atlas pixel detector and the pixel cell

The ATLAS 3D project steps

FEI4_P1 design : IBM 130nm, 8 metals
- 14x61 "analogue" pixel matrix
- Pixel size : 50x166µm
- Rad-hard and SEU tolerance

FEC4_P1 circuit : 2D Chartered, 8 metals
- Pixel structure : identical to FEI4_P1 (due to schedule no optimization has been done)
- Objectives : test Chartered technology (functionalities, performances, radiation…)

FETC4_P1 circuits : 3D first prototype, 5 metals

FEC4_P2 circuit : 2D Chartered, 8 metals
- Based on FEC4_P1 circuit, plus :
- Optimization of transistors
- New latches for irradiation tests
- New PadRing strategy and ground/substrate separation

FEC4_P3 : 2D Chartered, 8 metals but only 5 are used)
- Smaller pixel size : 50µm x 125µm
- Design of new sub-circuits and functionalities :
  - Analogue multiplexor
  - Triple redundancy

Submission / Test :

March 08 / Summer 08

February 09 / April 09

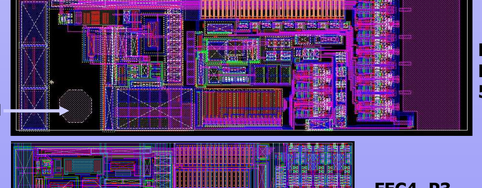
Main results are equivalent to IBM ones
Threshold min around 1100 e-
Un-tuned threshold dispersion 200 e-
Noise lower than 80 e-
Problem discovered after 160 MRad on latches which output tends to be blocked in "1" state

July 09 / expect fall 10

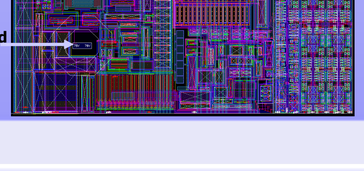
November 09 / January 10

Main results are equivalent to FEC4_P1 ones the chip has received up to 200Mrad eq ne without latch output stacked to "1"

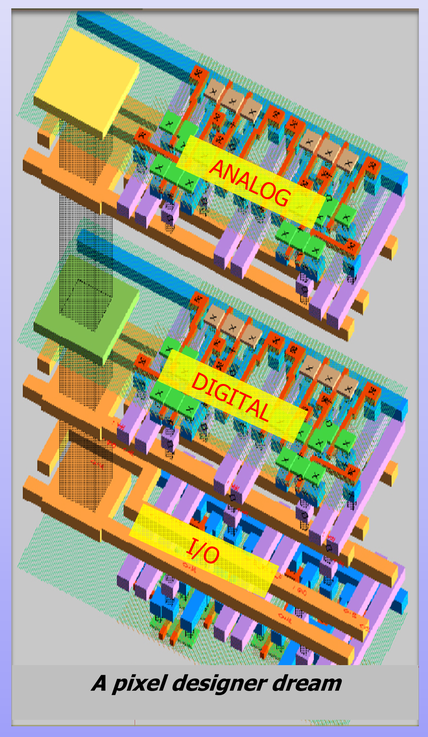
September 10 / End of 10



FEC4_P1 (Chartered technology)
From the FEI4_P1 (IBM technology)
50µm x 166µm



FEC4_P3
Size optimization
From the FEC4_P1 and P2
50µm x 125µm



A pixel designer dream

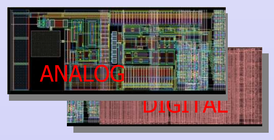
3D ELECTRONICS

Future requirements of post LHC accelerators are, as usual, one step beyond the actual ones in terms of speed, spatial resolution, material budget, radiation hardness and cost.

Facing some of these challenges might be addressed by diminution of the electronic feature minimal size. However, emerging 3D technologies could offer an alternative way with the advantages of technology mixing and cost effectiveness.

As it is the case today for the sensor, analog and digital part of the pixel will be designed choosing the best available technology for each part rather than trying to choose the best compromise between opposite requirements.

3D-IC electronic for SLHC/ATLAS hybrid pixels detectors

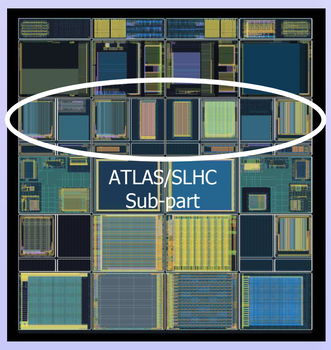


Design a 3-D pixel based on the FE-I4 pixel by splitting its functionalities into two parts :

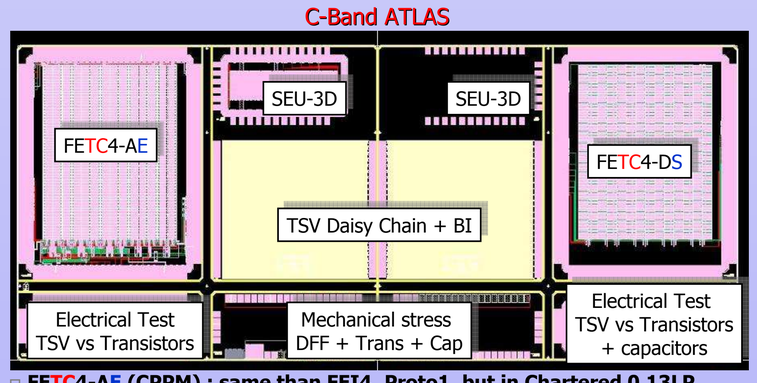
- one for the analogue functions,
- one for the digital parts.

2009 : First 3D MPW run for High Energy Physics organized by FNAL with a consortium of 15 institutes (France, Germany, Italy, Poland and United-States)

The proposed 3-D process combines :
- CHARTERED 130nm Low Power technology
- TEZZARON 3D technology

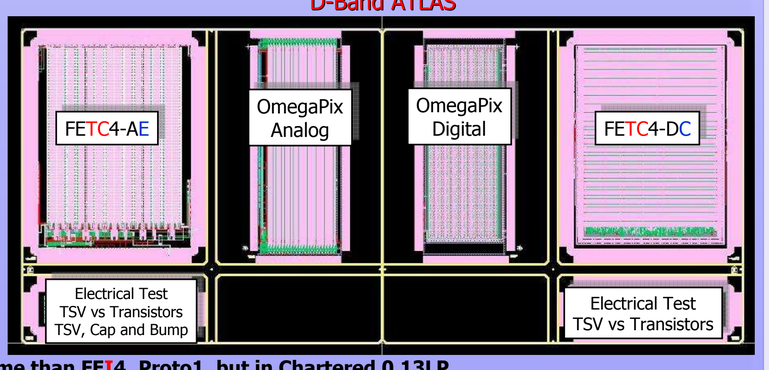


C-Band ATLAS



- **FETC4-AE (CPPM) : same than FEI4_Proto1, but in Chartered 0.13LP**
- **FETC4-DS (CPPM) : Shift Register + counter + readout data and "Drum registers"**
- **SEU-3D (CPPM) : SEUless memories blocks**
- **General test structures (CPPM) : TSV + BI Daisy chain (electrical parameters) ; TSV capacitors value with and without BackMetal and BI ; Transistors (Linear and ELT) closed to TSV ; Mechanical stress effects of devices (Trans, Cap, Res, DFF)**

D-Band ATLAS



- **FETC4-AE (CPPM) : same than FEI4_Proto1, but in Chartered 0.13LP**
- **FETC4-DC (Bonn-CPPM) : Digital pixels Read-out "à la FEI4"**
- **OmegaPix (LAL)**
- **General test structures (CPPM) : TSV + BI Daisy chain (electrical parameters) ; TSV capacitors value with and without BackMetal and BI ; Transistors (Linear and ELT) closed to TSV ; Mechanical stress effects of devices (Trans, Cap, Res, DFF)**

THE FIRST 3D HYBRID PIXEL READ-OUT CHIP FOR SLHC/ATLAS

Reducing pixel size needs very small connexion vias and pitches in order to fit the overall pixel dimension (about 150 µm) without wasting too much space. A post-process (via-last) 3D staking seems actually inappropriate to fulfill pixel design requirements. On the other hand , access to via-first process which provide the smallest possible wafer interconnexions reduce drastically the amount of commercially available technologies. In a first step, we choose to use a Tezzaron/Chartered technology which could be accessed in few MPW runs.

In this technology, based in 0.13 µm Chartered process, vias can be as small as 1.2 µm diameter with 2.5 µm pitch. Through Silicon Vias are formed before the BEOL of Chartered process and they are of about 12 µm depth.

ATLAS pixels collaboration has submitted in 2009 a prototype of a pixel Read-out chip based on a "translation" of the 2D, IBM 0.13 µm chip. In this latter prototype, pixel dimension are of 50*250 µm. Two tiers, face to face option has been chosen for this first run and the pixel length will be scaled down to 125 µm.

In the same time, some 2D prototypes have been developed and tested, to prepare the full scale FETC4_A for next year. The FETC4 chip is a FEI4 blocks reuse, compatibility with FEI4 chip (the next generation FE for upgraded ATLAS pixel detector in traditional 2D technology) for sensors, bump bonding , module/stave integration, testing tools, software, mechanics.

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