Signal processing for High Granularity Calorimeter: Amplification, Filtering, Memorization and Digitalization

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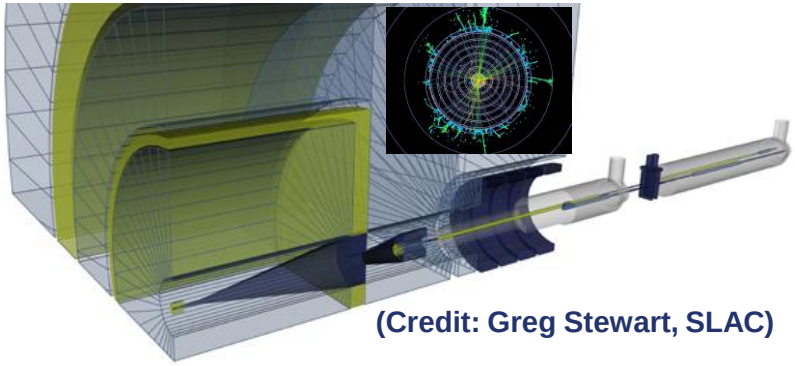
LPC Clermont-Ferrand

International Linear Collider

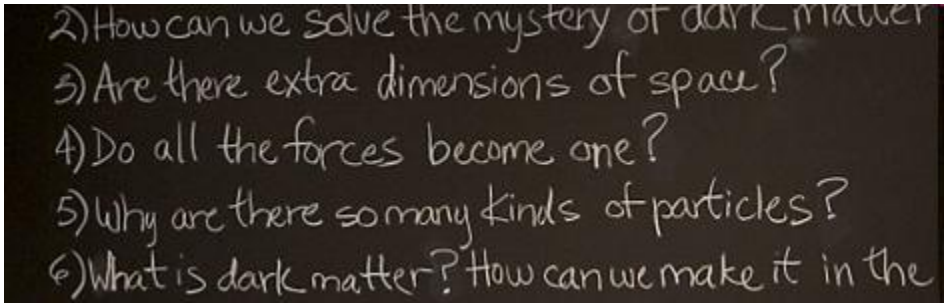
ILC "could be the next big adventure in particle physics"

[http://www.linearcollider.org/]



(Credit: Greg Stewart, SLAC)

The possible discoveries scientists could make with the ILC



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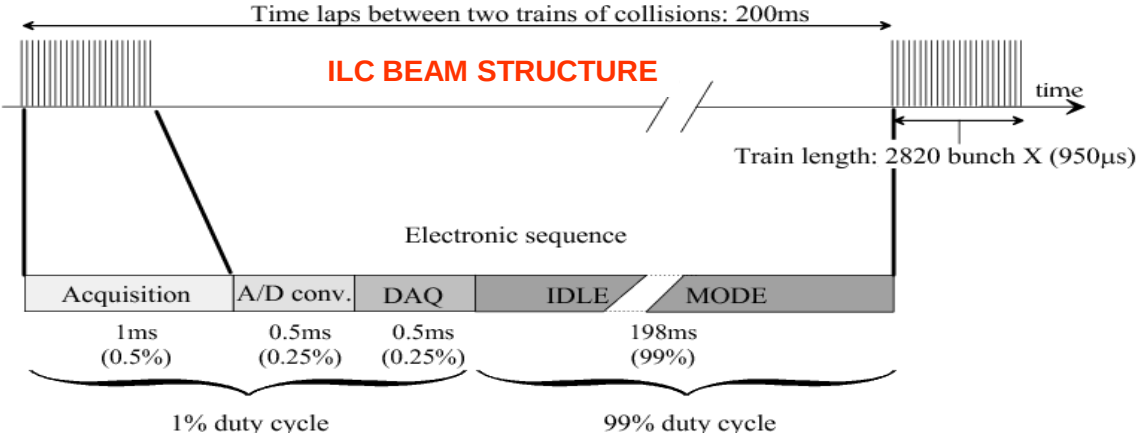


ILC BEAM STRUCTURE:

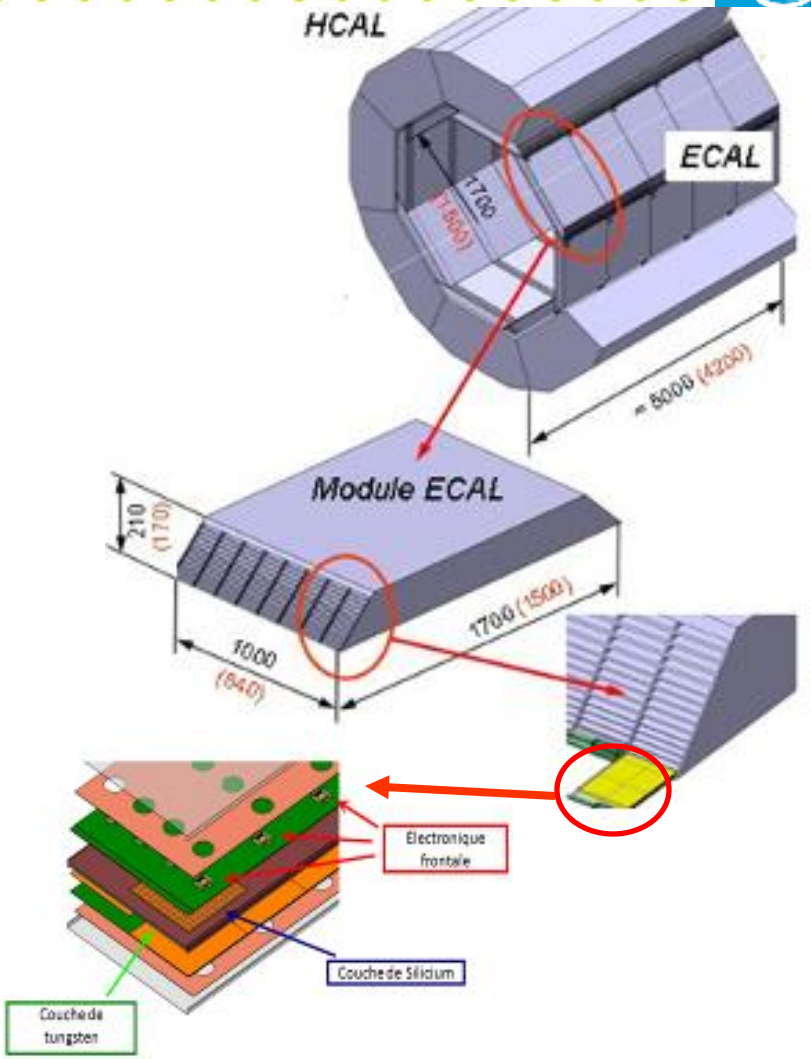
- about 300ns between collisions
- duration of train of collisions: 1ms
- no beam during 199 ms
- with 1ms to convert signals and output data → 99% of the time with no activity for electronics on detectors

Challenges for next generation of Ecal

- ✓ Sandwich structure of: thin wafers of silicon diodes & tungsten layers
  - ➢ Embedded Very Front End (VFE) electronics
    - ➢ Deeply integrated electronics
- ✓ High granularity : diode pad size of 5x5 mm^2
- ✓ High segmentation : ~30 layers
- ✓ Large dynamic range of the input signal (15 bits)
  - ✓ **0.1 MIP (noise level) -> ~3 000 MIPs**
- ✓ Minimal cooling available and > 100.10^6 channels
  - ➢ Ultra-low power : 25 µW per VFE channel

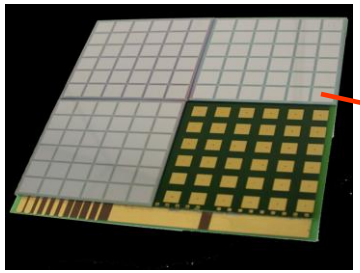
⇒ power pulsing required (1% duty cycle)

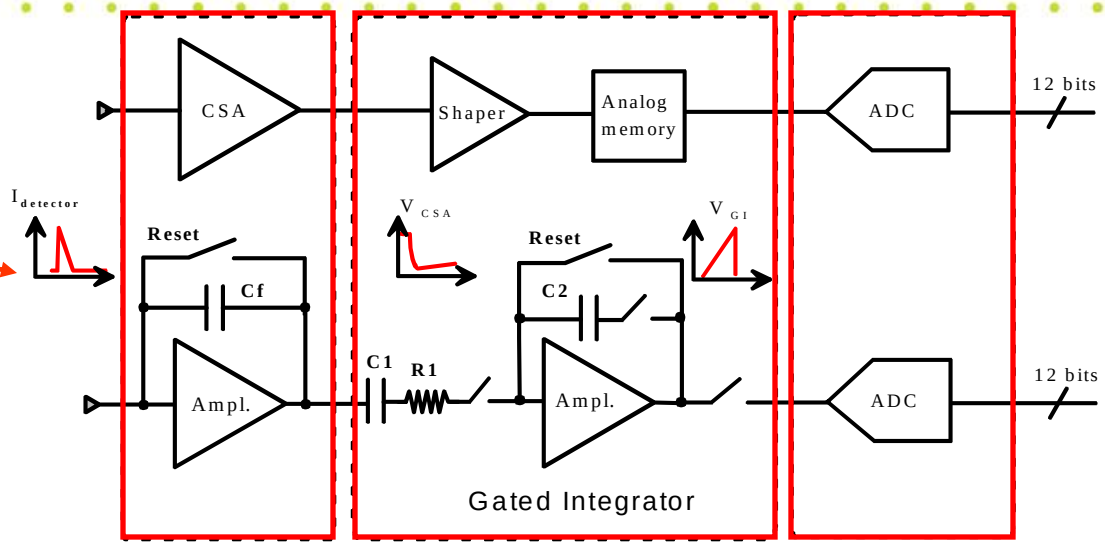
« Tracker electronics with calorimetric performance »



Analog electronics busy	A/D conv.	DAQ	IDLE MODE
1ms (.5%)	.5ms (.25%)	.5ms (.25%)	198ms (99%)

Architecture of the VFE designed





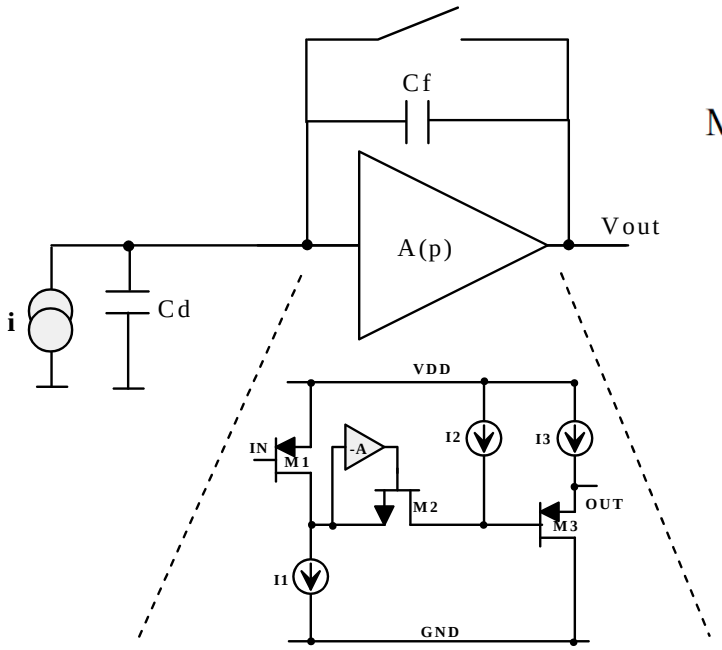
- ✓ **Charge Preamplifier**
  - The amplification of the charge delivered by the detector is performed with a low-noise Charge Sensitive Amplifier (CSA)
- ✓ **Shaper and Analog Memory**
  - The bandpass filter is based on a gated integrator which includes an intrinsic analog memory thanks to the integration capacitor
- ✓ **Analog to Digital Converter**
  - The converter is a customized low power 12-bit cyclic ADC
- ✓ **External digital block to control the G.I. and the ADC (in a FPGA)**
- ✓ **Technology: AMS CMOS 0.35µm**

The Charge Sensitive Amplifier (CSA)

- The amplifier is based on a boosted folded cascode, followed by a source follower
  - **Boosted Cascode : High gain performance**
  - **Source follower : Low output impedance**

$$V_{out} \approx -Q/C_f$$

Q, the charge delivered by the detector.
***Cf,* the feedback capacitor.**



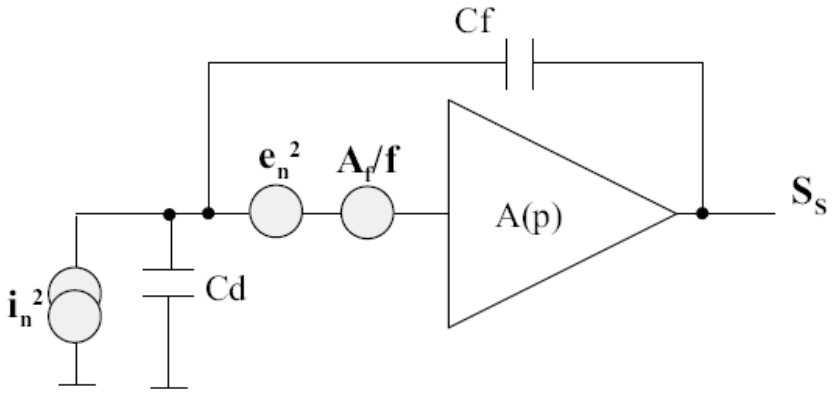
MAIN CHARACTERISTICS OF THE CSA (SIMULATED RESULTS).

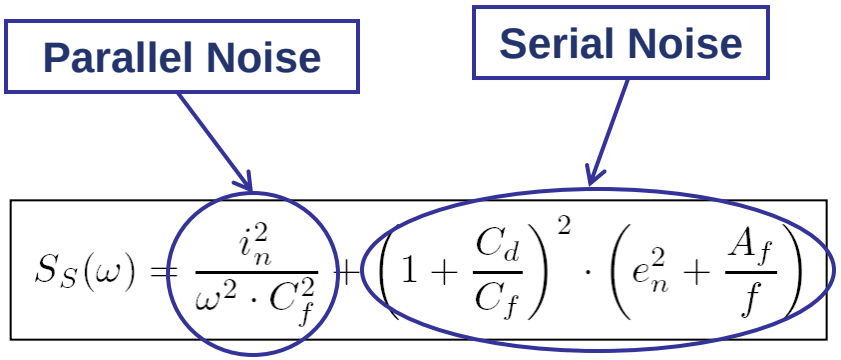
Power supply	3.3 V
Consumption	3.54 m
$C_{Detector}$	
$C_{Feedback}$	
Transconductance gm_1	/ mS
Open Loop Gain G_{OL}	83 dB
Gain-Band Width	105 MHz
Output swing	1.0 V
ENC (with a 200 ns CCRC shaper)	0.24 fC
Dynamic range	92 dB

50% for masters of the current sources
→ can be shared by several channels

The charge preamplifier

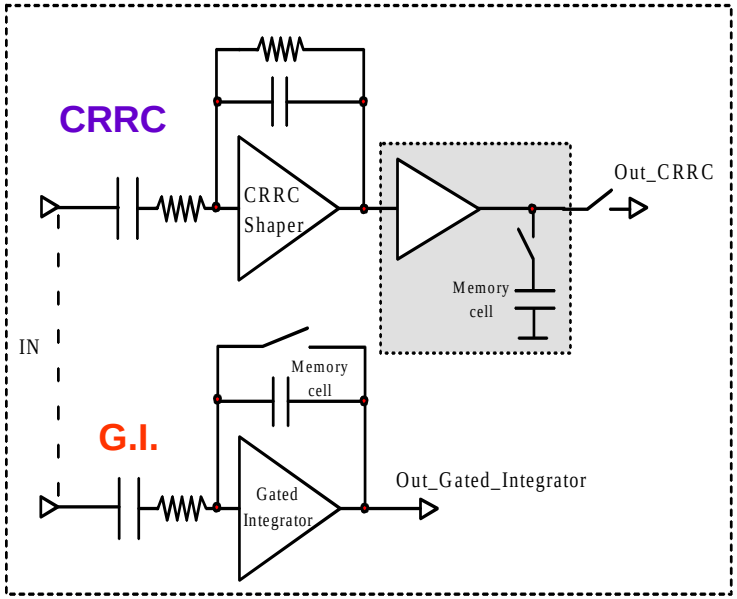
- The spectral density of the noise at the output of the CSA is mainly composed of two terms: parallel and serial noises

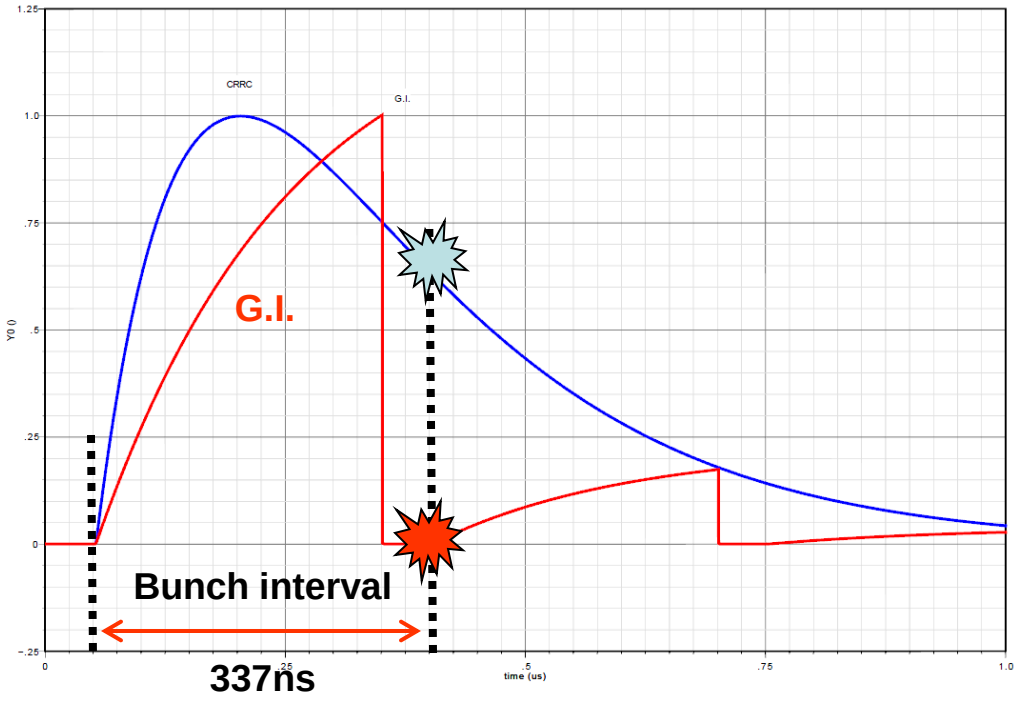




- **i_n corresponds to the gate leakage current of the detector and the current noise contribution of R_f**
- **e_n is the thermal noise introduced by the input transistor**
- **A_f is the process dependant flicker noise parameter**

CRRC Shaper vs Gated Integrator (GI)





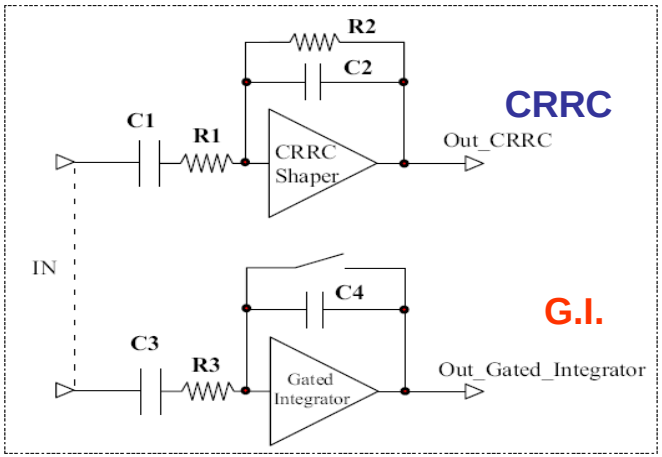
- **The integration capacitor of the G.I. can be used as an analog memory cell (switch opened at the end of the integration)**
  - no extra analog-memory stage required
- **The fast switched reset of the capacitor of the G.I. allows a time of integration near to the bunch interval**
  - no pile up
  - improved noise filtering (see next slides)

Comparative noise filtering performances of Gated Integrator and CRRC filtering

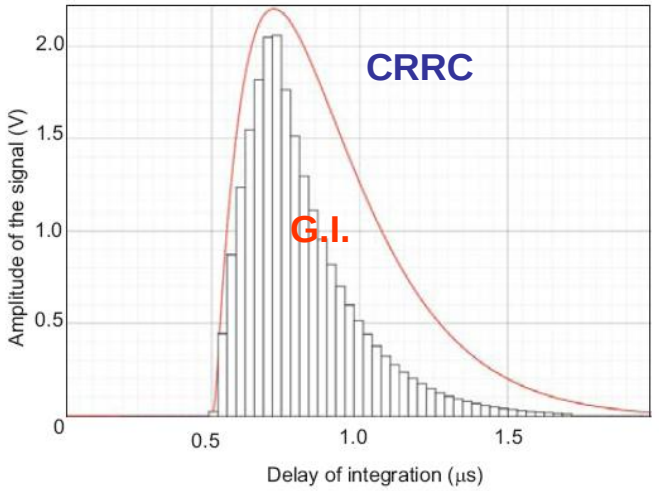
- CRRC shaper is time invariant filter
- Gated integrator is time variant filter

  - **To compare performances, weighting functions R(t) in time domain MUST BE USED (see publications of V.Radeka & Goulding)**

- *The weighting function is the measurement of influence of a noise step generated before the measuring time on the amplitude at the measuring time*



Obtained by simulation with Virtuoso from Cadence



Comparative performances of Gated Integrator and CRRC filtering

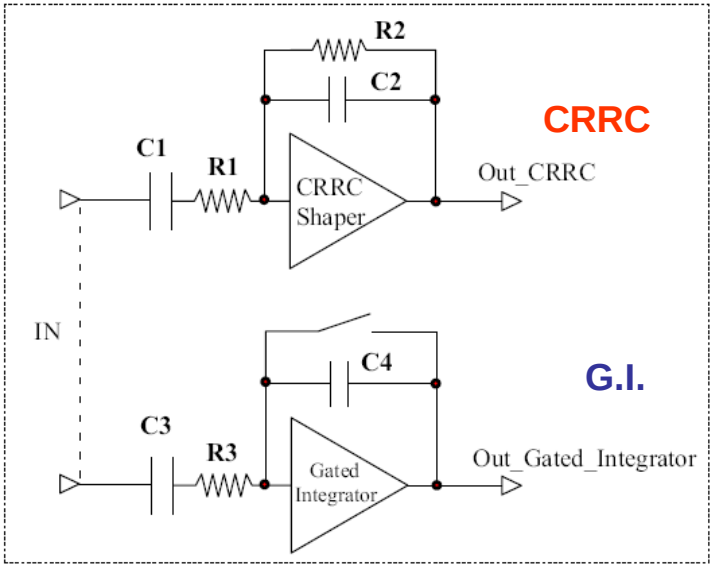
- R(t) is used to calculate noise indexes:
  - ***Parallel Noise index***

$$< N_S^2 >= \frac{1}{A^2} \int_0^\infty [R(t)]^2 \, dt$$

  - ***Serial Noise index***

$$< N_\Delta^2 >= \frac{1}{A^2} \int_0^\infty [R'(t)]^2 \, dt$$

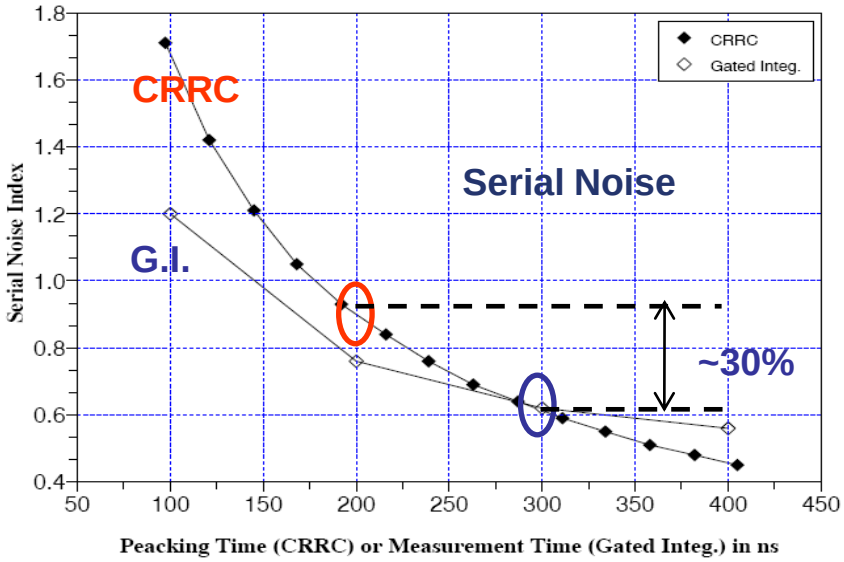
A: gain of the system

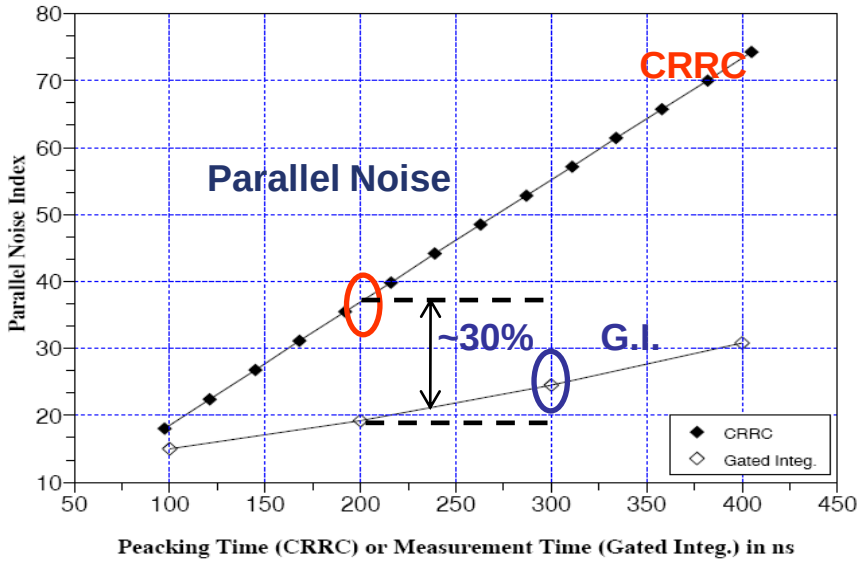


- *The parallel and serial noises can be evaluated for any case of shaper to compare filtering performance*

Comparative performances of Gated Integrator and CRRC filtering

- **Noise indices have been simulated with Analog Artist (Cadence) Software for several peaking times (CRRC) and durations of integration (G.I.)**

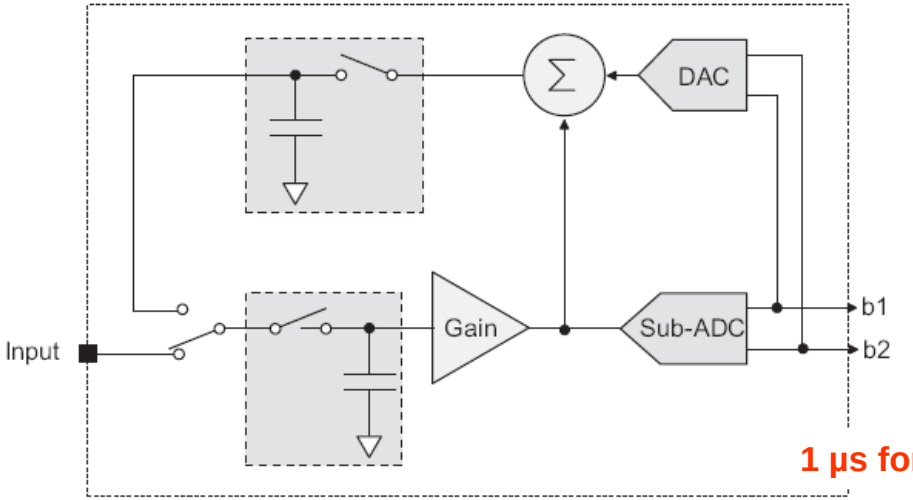




- **The peaking time of the CRRC shaper is limited due to pile-up consideration**
  - → **200ns with a bunch crossing of 337ns (ILC).**
- **For the Gated Integrator, fast reset of integration capacitor allows duration of integration near to the bunch crossing interval**
  - → **300ns with bunch crossing of 337ns**

→ both serial and parallel noise indexes can be reduced by about 30% with the G.I. filtering.

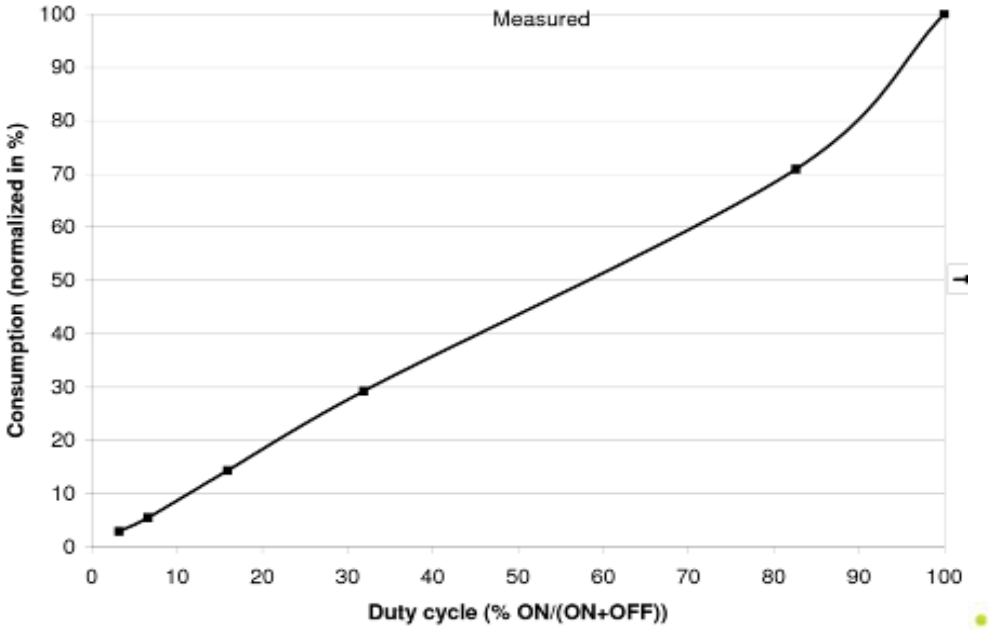
Architecture of the 12 bits cyclic ADC



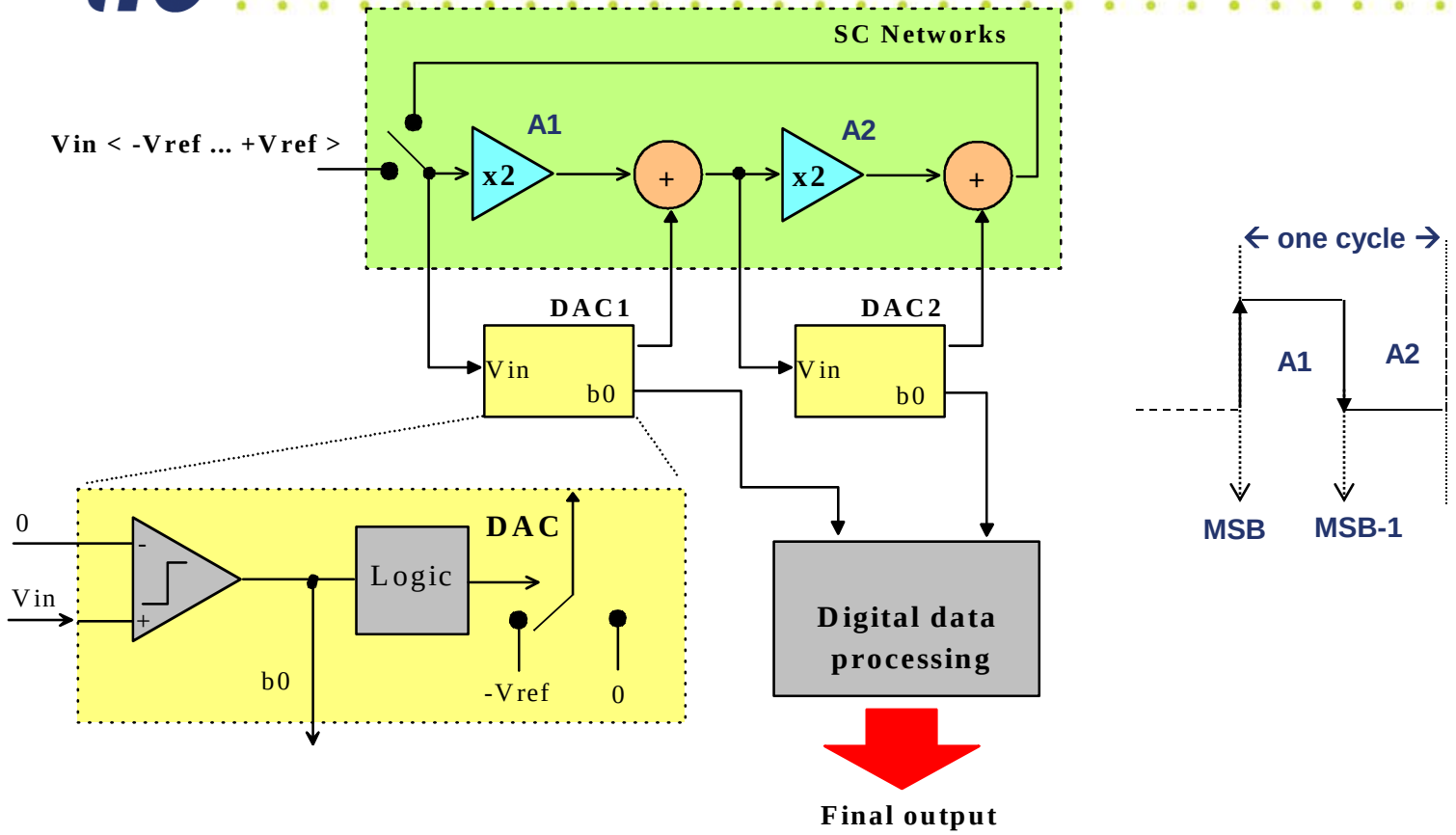
Architecture	1.5-bit/stage
Area	0.12 mm^2
Supply Voltage	3.0 V
Resolution	12 bits
Dynamique range	2.0 V differential
Time of conversion	6.8 μs
Consumption	1.5 mW
INL	3 LSB
RMS Noise	0.3 LSB

1 µs for recovery time included after power ON

- **The cyclic architecture is well adapted to compact-low-power converter**
  - **1.5 bit per stage architecture**
  - **Clock frequency: 1MHz**
  - **Power pulsed**



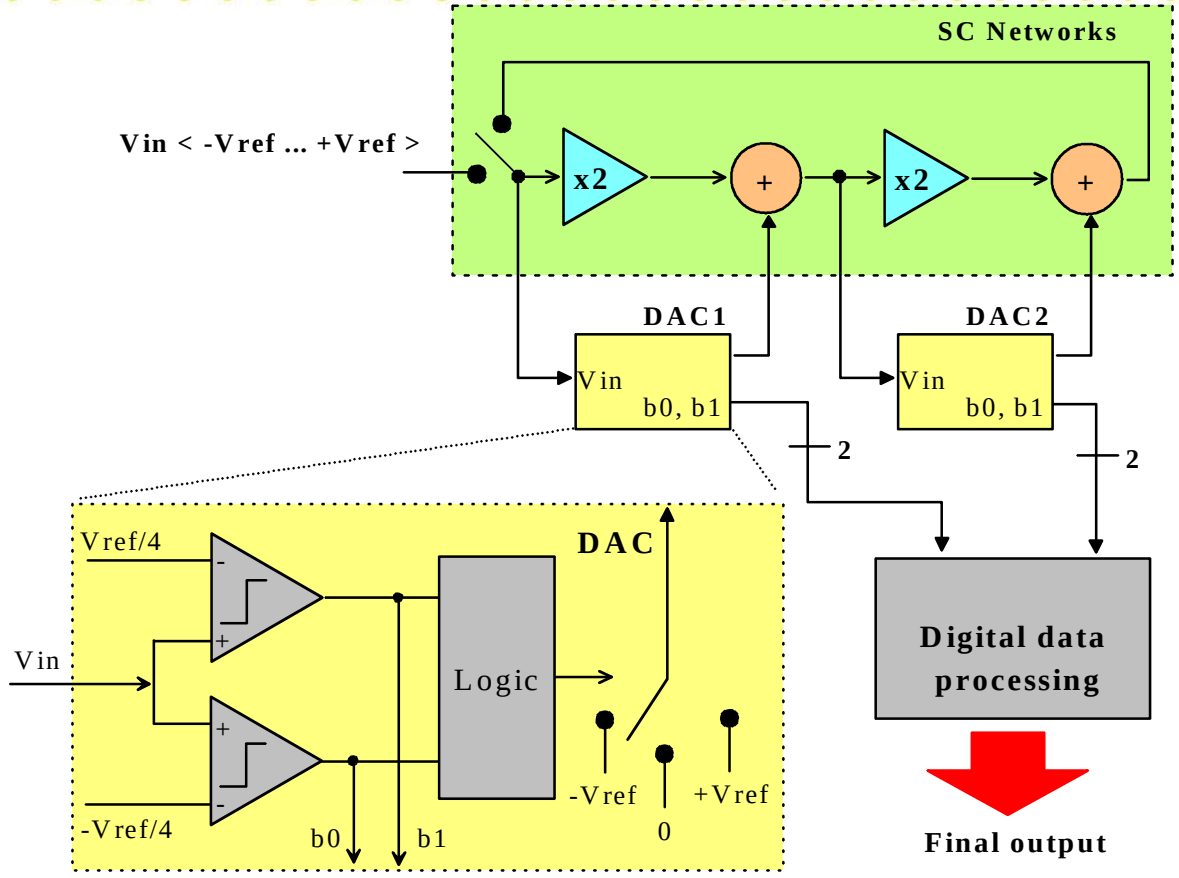
Conventional 2-stage Cyclic architecture



- ✓ One cycle = two phases of amplification and sampling
- ✓ At each cycle (one clock period), 2 bits are delivered → MSB then MSB-1, …..until LSB
- ✓ For an n-bit ADC, n/2 cycles are required
- ✓ The key block: gain-2 amplifier (switched capacitors amplifier)

→ The precision of the gain-2 amplification gives the precision of the ADC

1,5 bit/stage Cyclic architecture

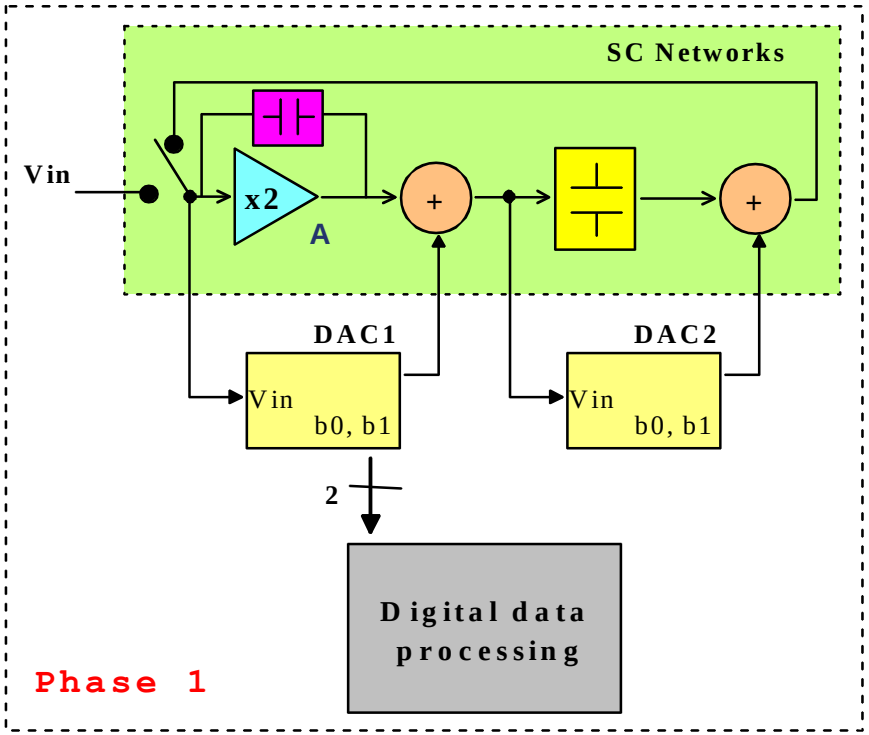


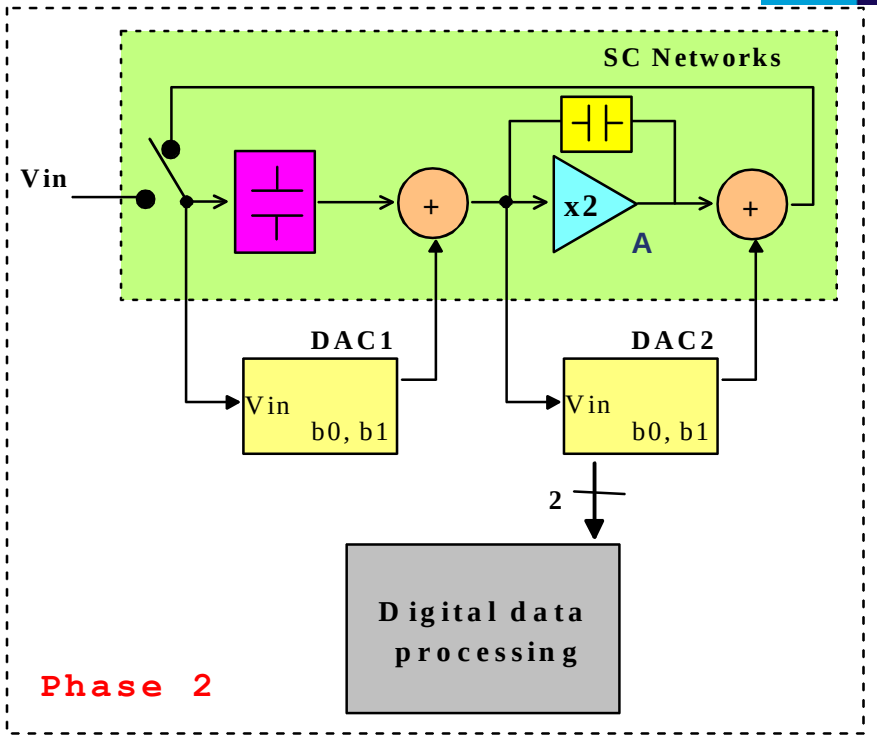
✓+ 1 redundant bit at each cycle

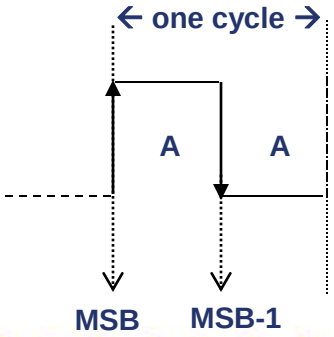
→ **Precision of the ADC becomes insensitive to the offset of the comparators up to ± 1/8 of the dynamic range (± 125mV for 2 V)**

✓ Number of comparators is doubled

Enhanced architecture: "Flip-around amplifier "

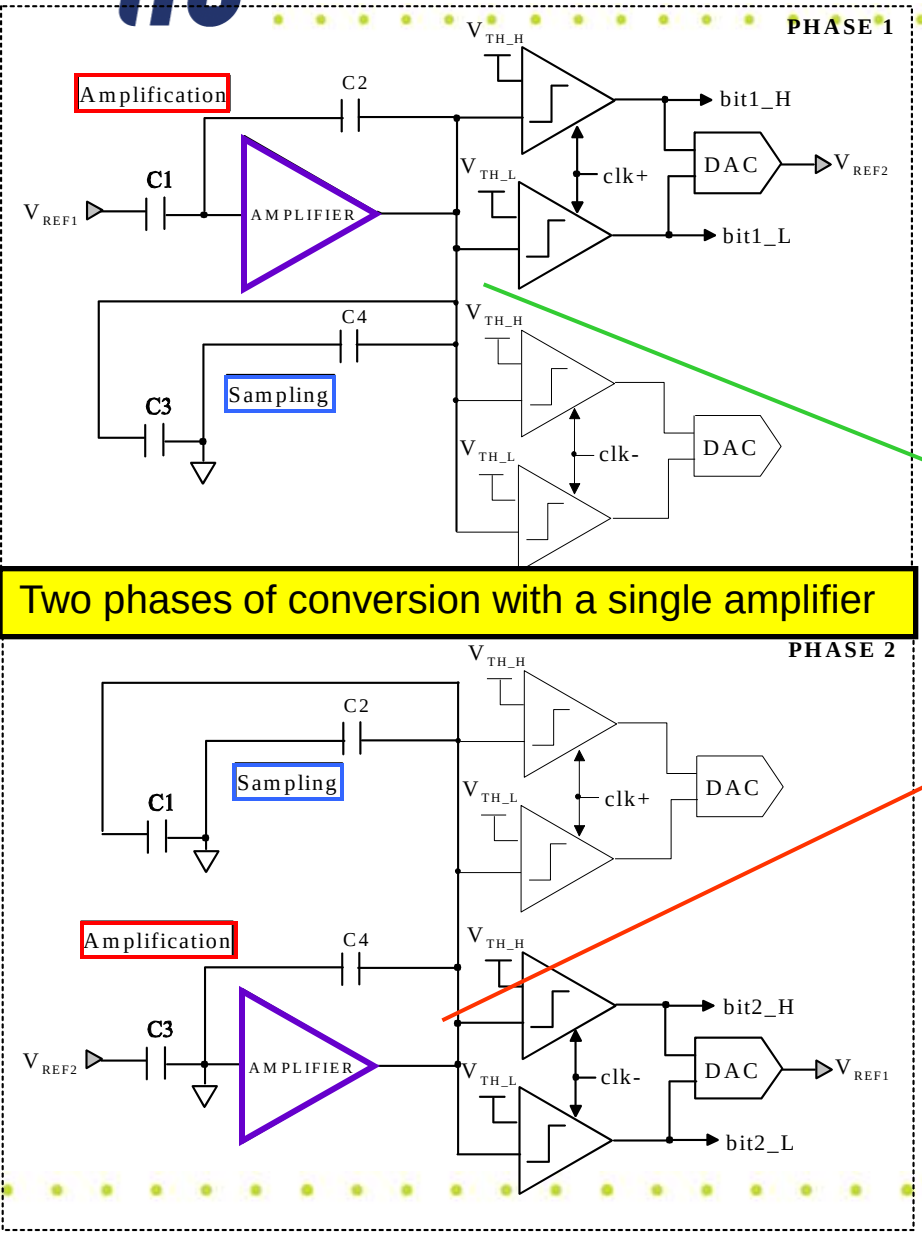




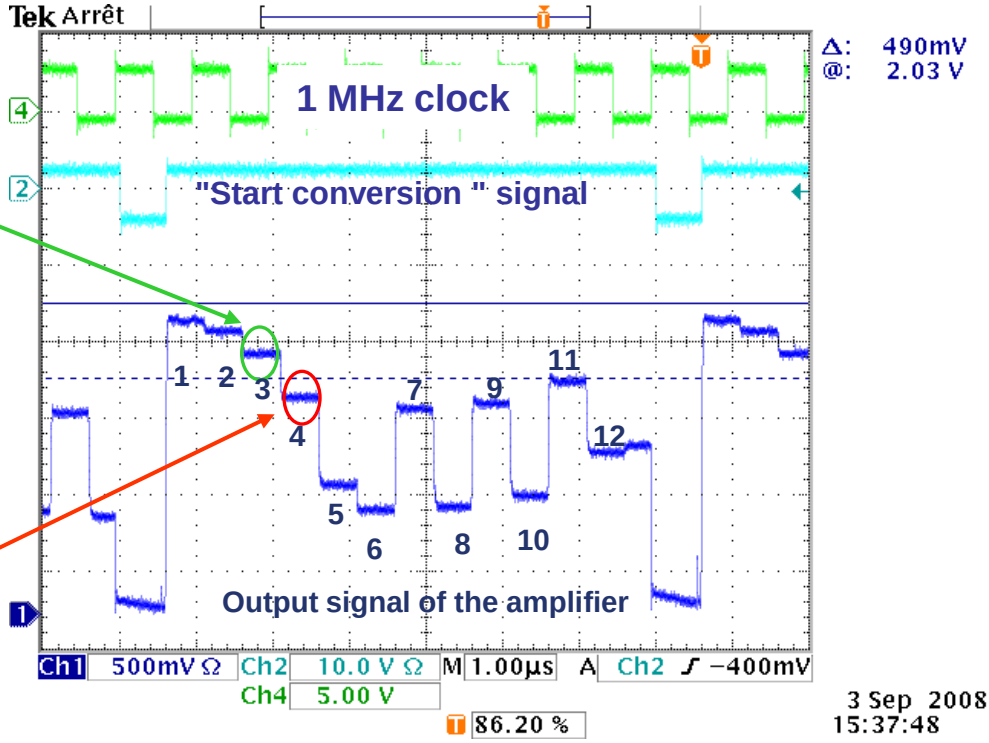


- ✓ A single amplifier shared by the two stages
- ✓ As main of the power is consumed by amplifier
  → reduction of power up to 40%

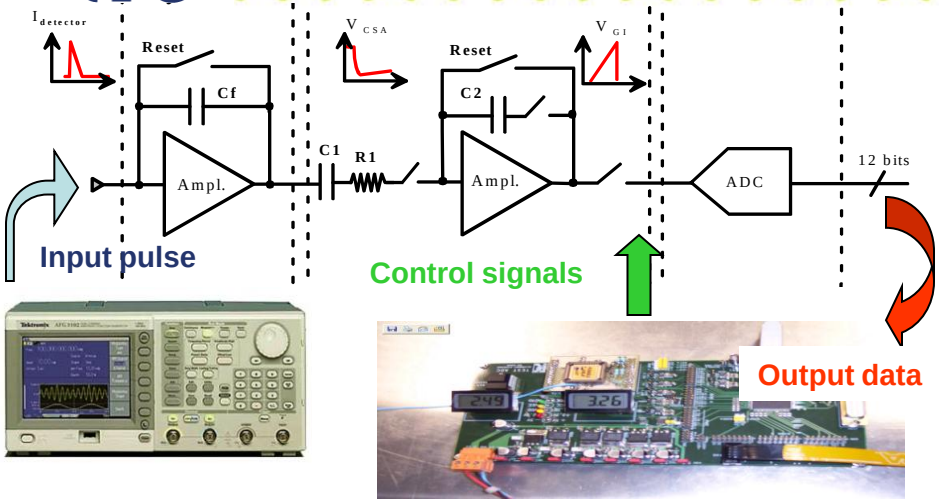
Enhanced architecture: "Flip-around amplifier "

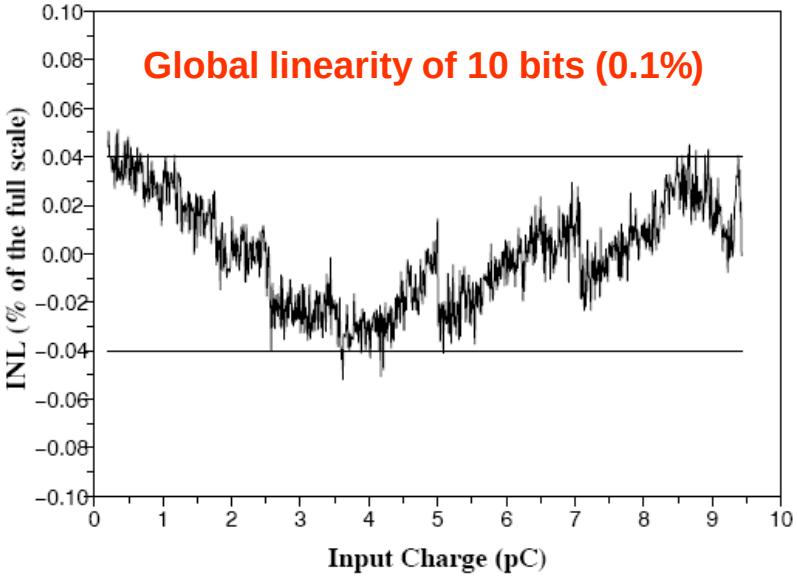


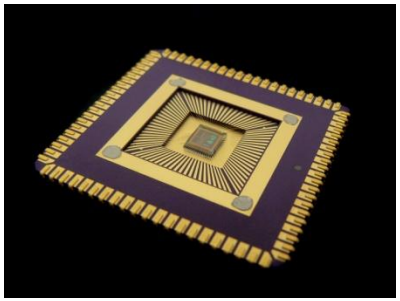
Two phases of conversion with a single amplifier



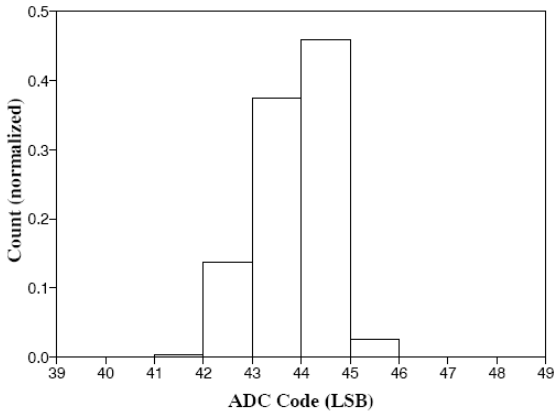
Results of measurements of the VFE (1)







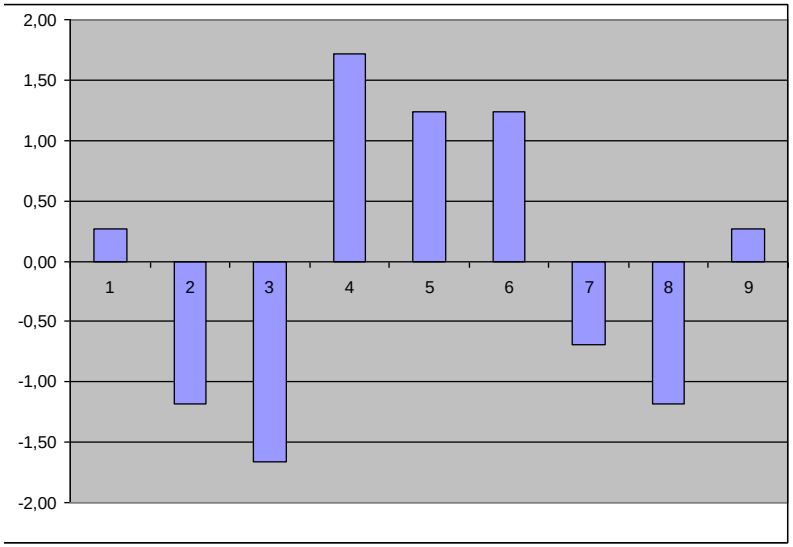
The standard deviation of the noise at the output of the channel is *0.76 LSB (370 µV rms).*
The Equivalent Noise Charge (ENC) at the input of the channel is then lower to 2 fC.

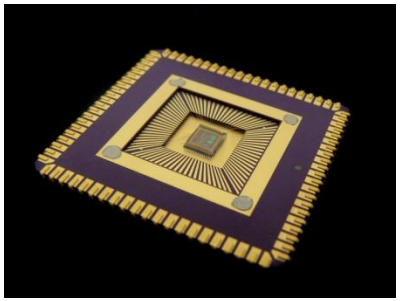


The power consumption of the channel is 6.5mW, estimated to 25µW with duty cycle of each block.

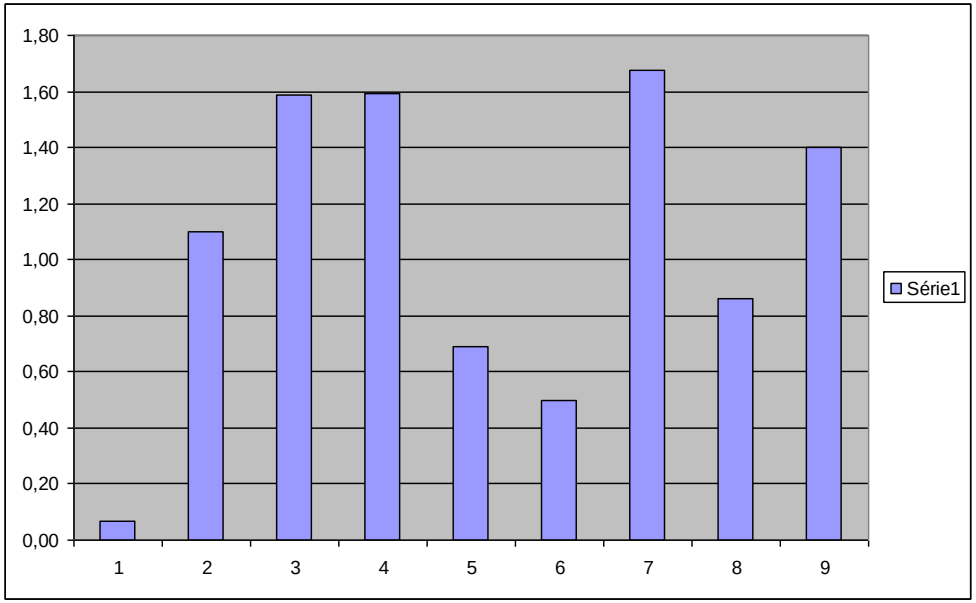
Results of measurements of the VFE (2)

Dispersion of the gain of the 9 chips (in %)



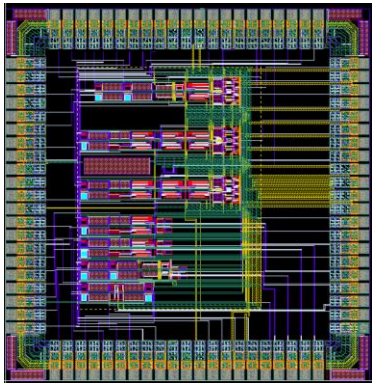


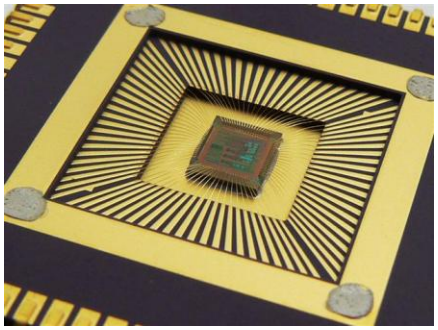
Dispersion of the offset of the 9 chips (in mV)



Summary

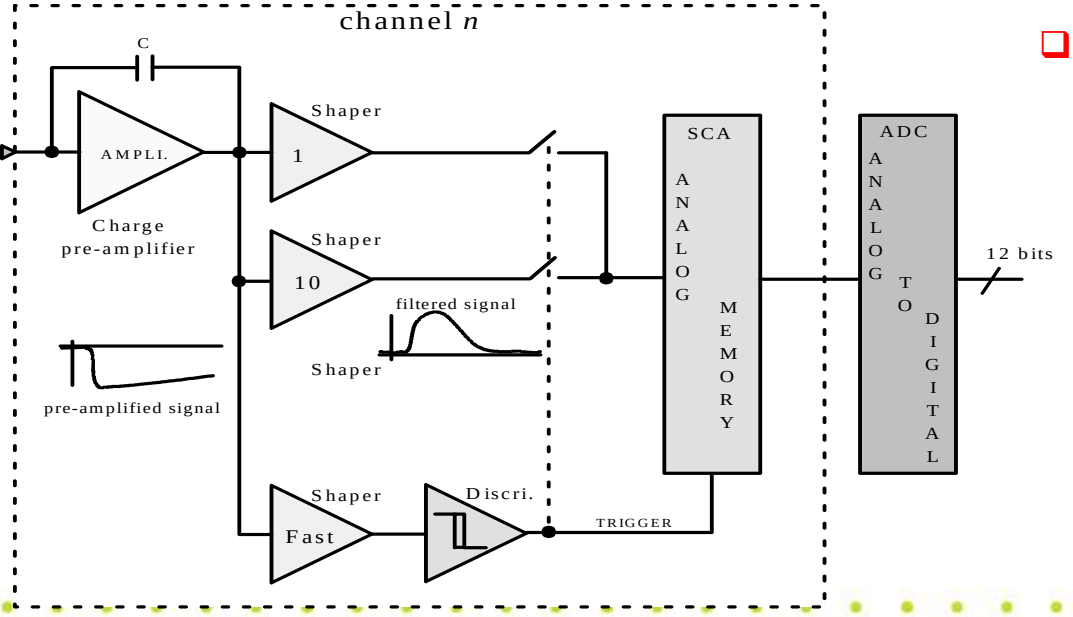
- A VFE channel performing the amplification, the filtering, the memorization and the digitalization of the charge from Si detector has been designed and tested.
  - **Global Linearity better than 0.1 % (10 bits) up to 9.5 pC (2375 MIP).**
  - **ENC = 1.8 fC (0.5 MIP)** with a single gain stage
  - **Power consumption with power pulsing (ILC timing) estimated to 25µW**





Present road map

- **Next step 1: improved and more complete channel**
  - **Improvement of the dynamic range**
    - **Reduction of the output noise of the amplifier of the Gated Integrator**
    - **Bi-Gain shaping**
  - **Fast shaping channel for auto-trigger**
  - **Integration of the digital block, of the bandgap (ADC references)**
  - **Implementation of the power pulsing**



- **Next step 2: multi-channels chip**
  - **pin compatible with SKIROC chip from LAL with same DAQ**
  - **comparative performances (synchro or asynchronous filtering, pure CMOS or SiGe techno., common or multi ADC, …)**

The workshop is devoted to the design of GHz microelectronic components for signal processing in high energy physics, astronomy and astroparticle physics, spatial and medical applications, as well as high rate networks.
It will be held October 28th to October 29th, 2010 at Laboratoire de Physique Corpusculaire (LPC) de Clermont Ferrand (FRANCE). It aims to review the state of the art of the technique and to bring together in an informal way design experts and potential users.
Workshop topics :

- **Needs and requirements in high energy physics, astrophysics, nuclear medical imaging,..**
- **Performance and limitations of the VLSI (Very Large Scale Integration) Technologies**
- **Wide Band Analogue Front End Electronics**
- **High rate SCA (Switched Capacitor Array)**
- **High rate ADC (Analog to Digital Converter)**
- **High rate networks**

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http://clrwww.in2p3.fr/www2008/giga/