TWEPP-10

SPIROC : second generation of Silicon PM Readout ASIC

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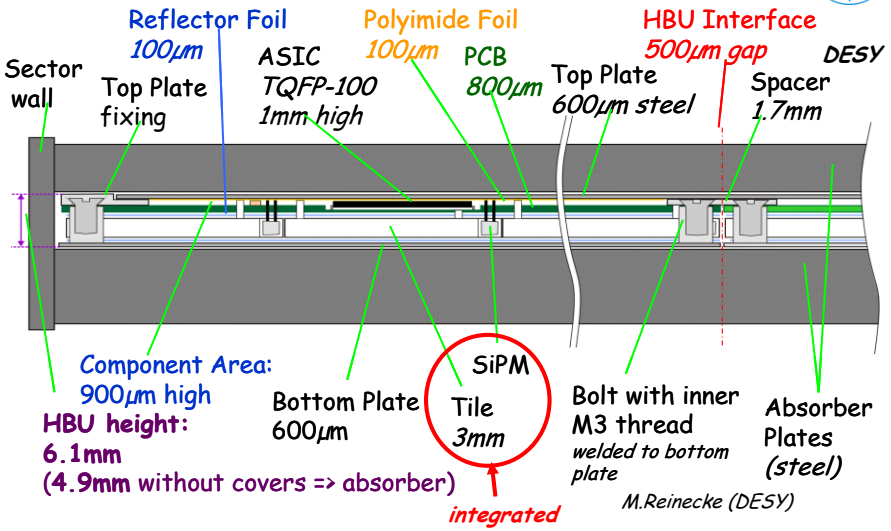
Orsay MicroElectronics Group Associated

Contents

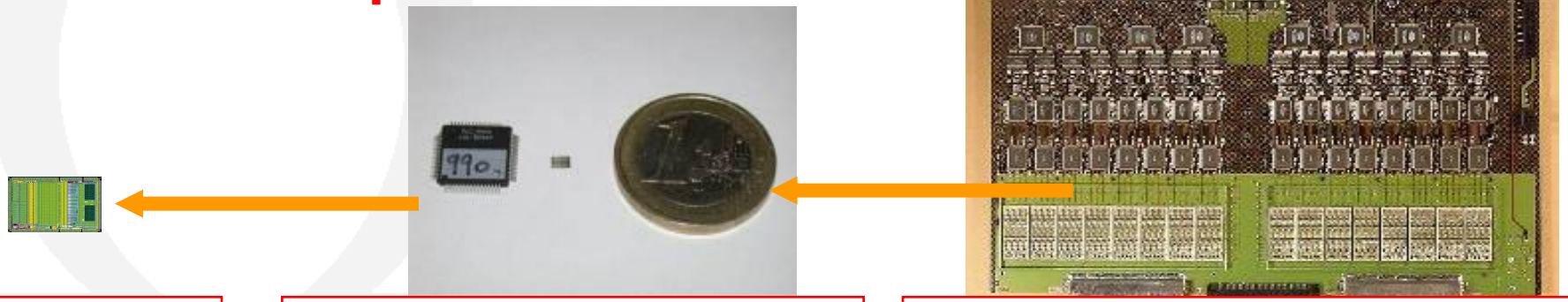
- **SPIROC : an ILC dedicated Chip**
  - ILC calorimetry electronics requirements
- **SPIROC, the second generation chip for SiPM readout:**
  - SPIROC Description
- **Chip measurements**
- **Summary and perspectives**

ILC Challenges for electronics

- **Requirements for ILC calorimetry electronics**
  - Large dynamic range (15 bits)
  - Auto-trigger on 1/3 MIP
  - On chip zero suppress
  - 10^8 channels
  - Front-end embedded in detector
  - Compactness
  - « Ultra-low power » : (25µW/channel)



- **« Tracker electronics with calorimetric performance »**



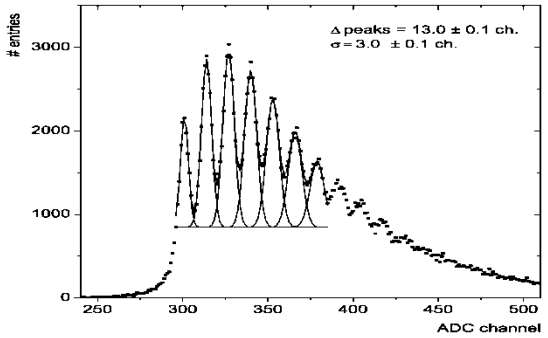
ILC **25µW/ch**

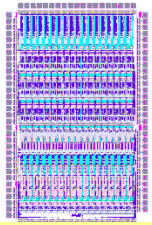
FLC_PHY3 18ch 10x10mm **5mW/ch**

ATLAS LAr FEB 128ch 400x500mm : **1 W/ch**

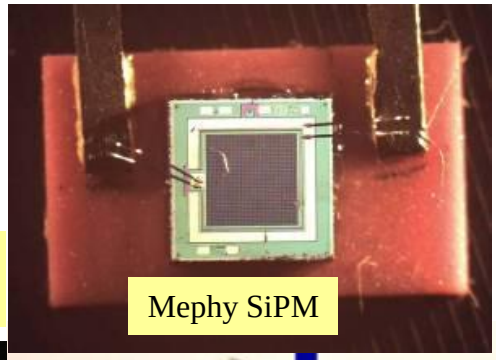
CALICE AHCAL testbeam physics prototype

- **SPIROC** is the second generation for SiPM readout
- The first generation **FLC_SiPM** was designed to equip the Analog H-Cal physics prototype for the ILC: 1 cubic meter, 38 layers, 2cm steel plates
- **8000 tiles with SiPM** fabricated by MePHY group

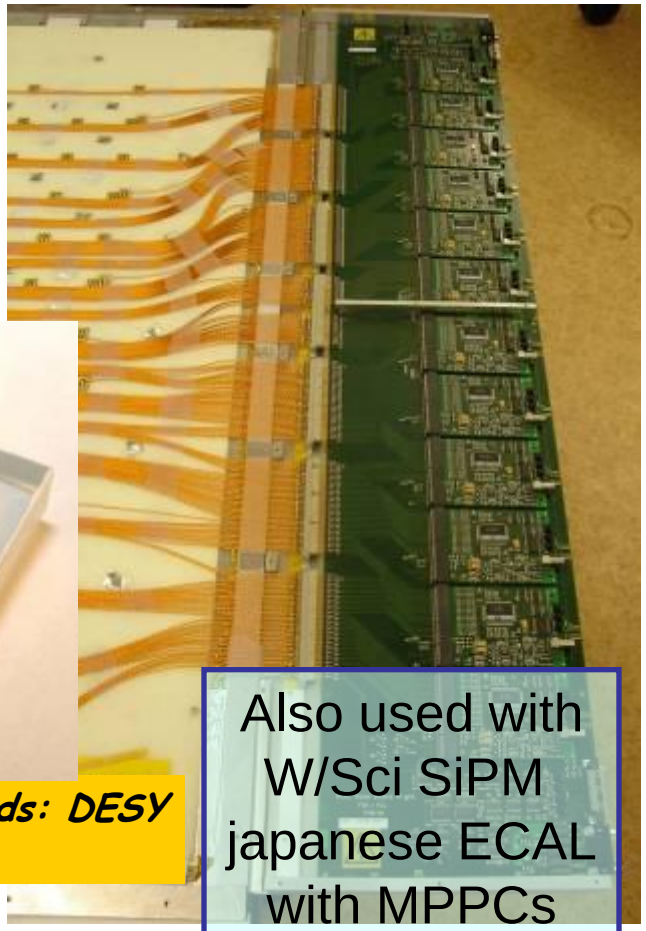


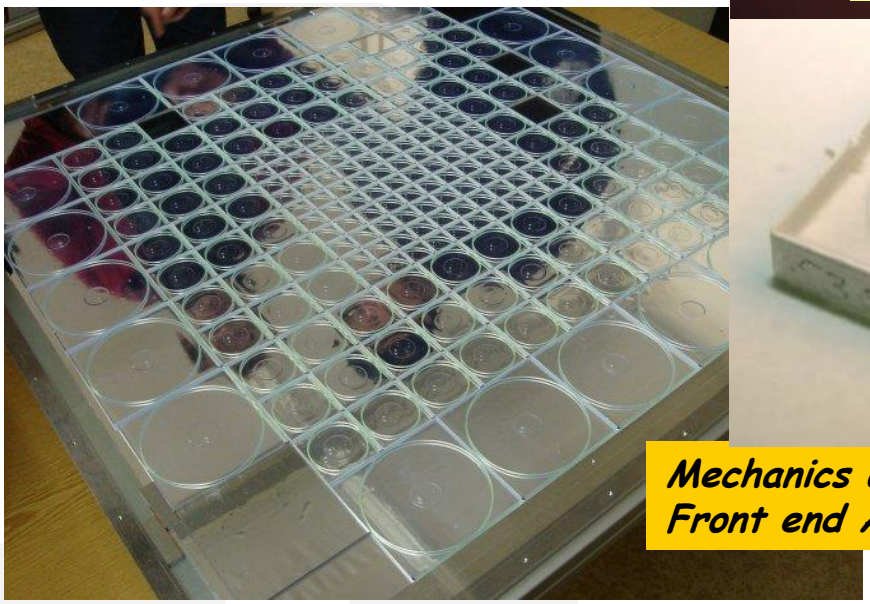


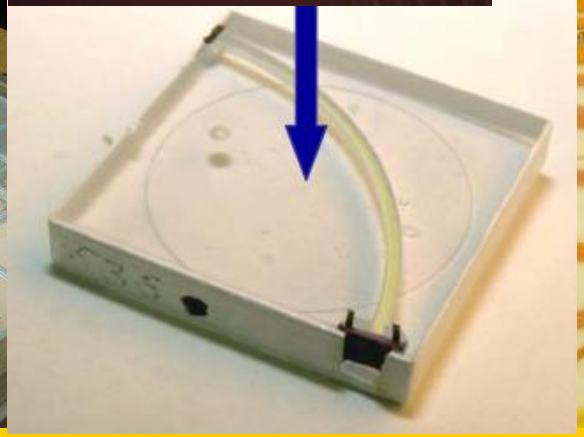
FLC_SiPM ASIC



Mephy SiPM





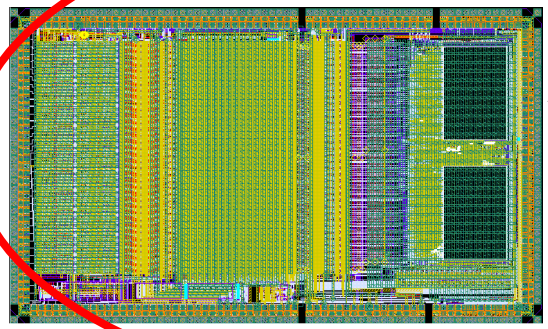


Mechanics and front end boards: DESY
Front end ASICs: LAL

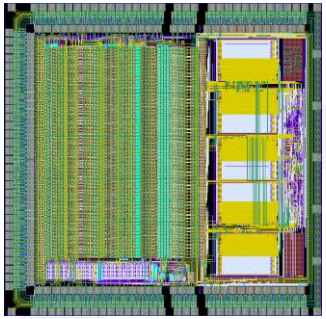
Also used with W/Sci SiPM japanese ECAL with MPPCs

The front-end ASICs : the ROC family chips

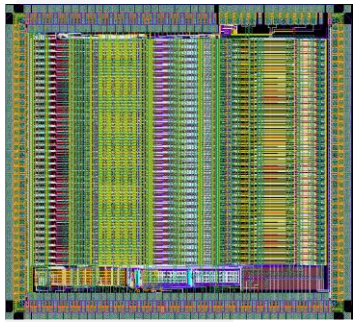
- **Technological prototypes : full scale modules (~2m)**
- **ASIC designed within the CALICE collaboration and EUDET (EU funding 2006-2010)**
- **ECAL, AHCAL, DHCAL**



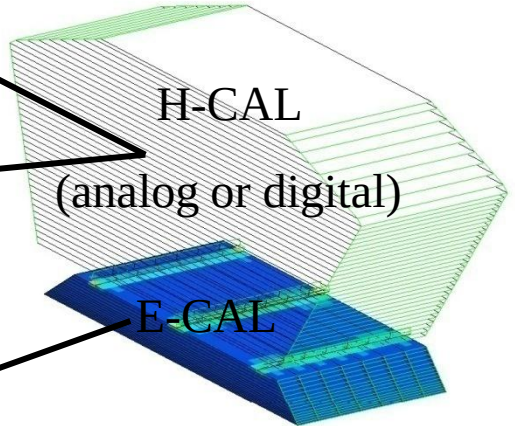
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²

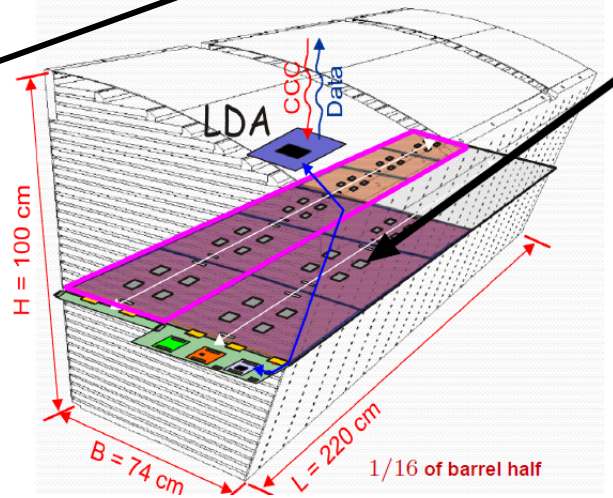


HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²



SKIROC
ECAL
(Si PIN diode)
64 ch. 60mm²

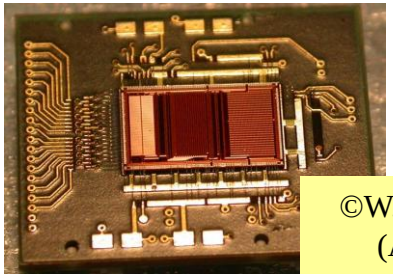




SPIROC chip:
handles signal from 36 SiPM

SPIROC saga….

- **200 chips SPIROC 1 produced in Nov 2007**
  - Package PQFP240
  - Good analog performance
  - Bug in ADC ramp : no digital data out



©W. Karpinski (Aachen)

- **50 chips SPIROC 2 produced in June 2008 to equip AHCAL and ECAL EUDET modules**
  - **EUDET milestone**
  - Package TQFP208
  - Difficult slow control loading

PEBS experiment Aachen University

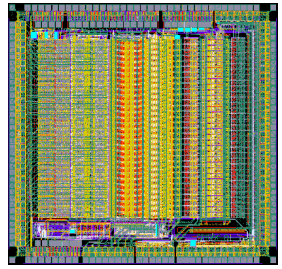
- **Full CALICE production run : April 2010 (Chip delivery Sept. 2010)**
  - **SPIROC 2a** (1200 chips) : conservative prototype in which the major bugs of SPIROC 2 are fixed
  - **SPIROC 2b** (1200 chips) : more agressive prototype in which the major bugs of SPIROC 2 are also fixed and some interesting improvements are added (in particular the independent gain adjustment channel by channel)
  - **SPIROC A** (3600 chips) : "light" analog version of SPIROC users who don't need the digital core.

MU-RAY project INFN Napoli

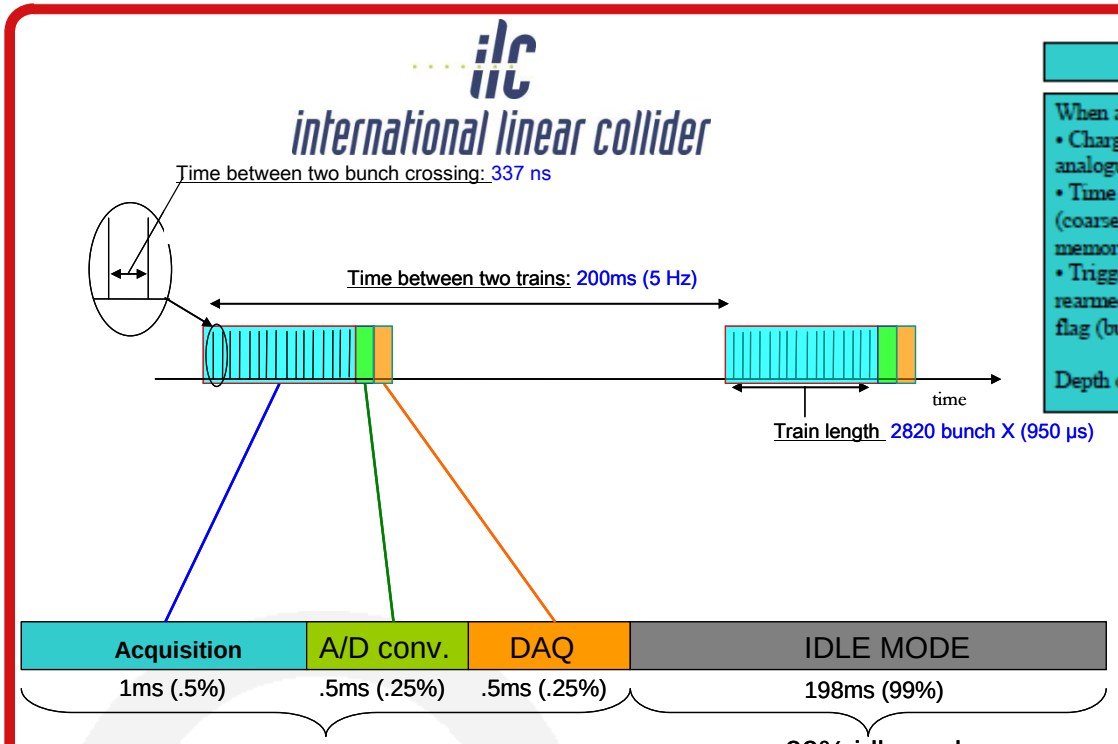
- **Others applications using SPIROC chips**
  - astrophysics PEBS experiment (Aachen University),
  - medical imaging (Roma, Pisa, INMC Orsay, Valencia, etc.)
  - Nuclear physics (IPNO, KEK)
  - Vulcanology: Muon radiography of geological structures (INFN Napoli)

SPIROC A

Fabricated in SiGe AMS 0.35 µm
Submitted in September 2009
Delivered in December 2009
Chip area: 17 mm² (4.2 mm × 4.1 mm)

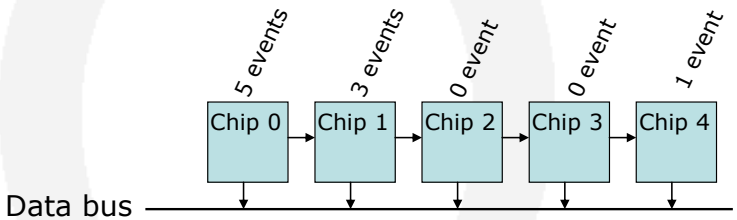


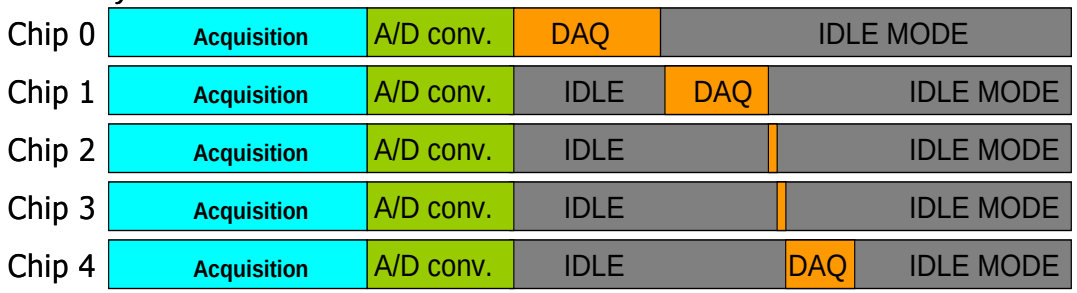
ILC beam structure and SPIROC running modes



Acquisition	A/D conversion	DAQ
When an event occurs : • Charge is stored in analogue memory • Time is stored in digital (coarse) and analogue (fine) memory • Trigger is automatically rearmed at next coarse time flag (bunch crossing ID) Depth of memory is 16	The data (charge and time) stored in the analogue memory are sequentially converted into digital data and stored in a SRAM.	The events stored in the RAM are readout through a serial link when the chip gets the token allowing the data transmission. When the transmission is done, the token is transferred to the next chip. 256 chips can be read out through one serial link

- **Readout based on token ring mechanism initiated by DAQ**
- **One data line activated by each chip sequentially**
- **Readout rate few MHz to minimize power dissipation**

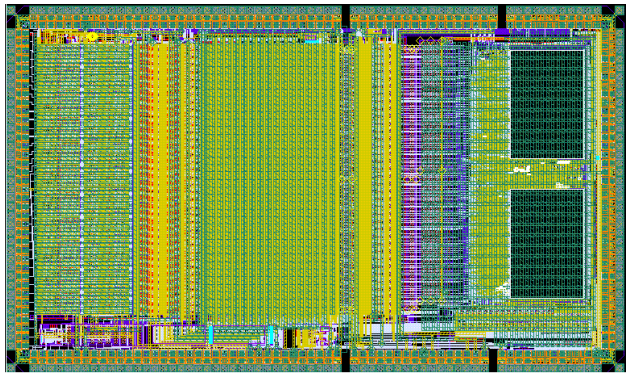




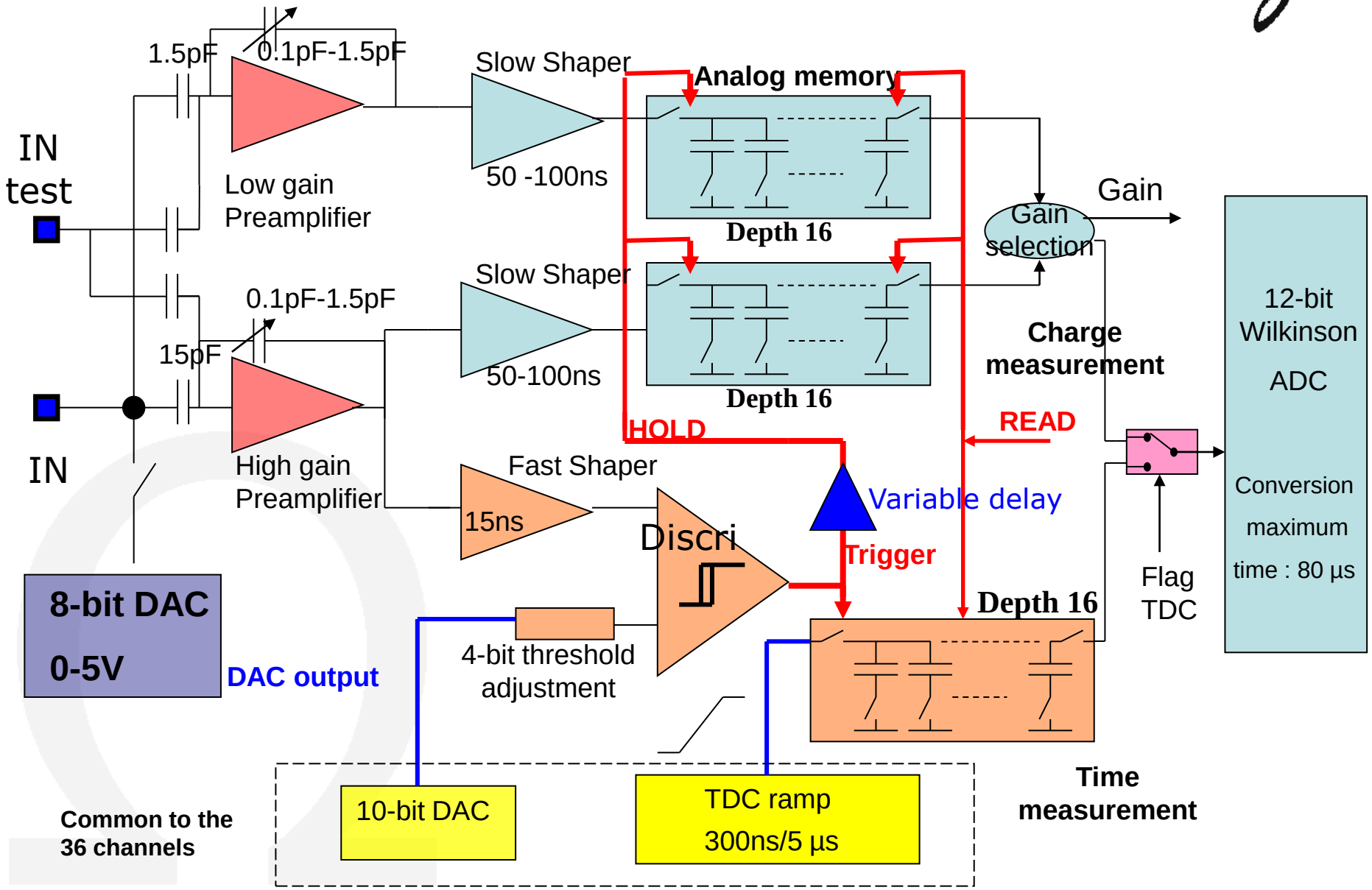
Two orders of magnitude saved on the consumption by using the ILC beam structure and the power pulsing

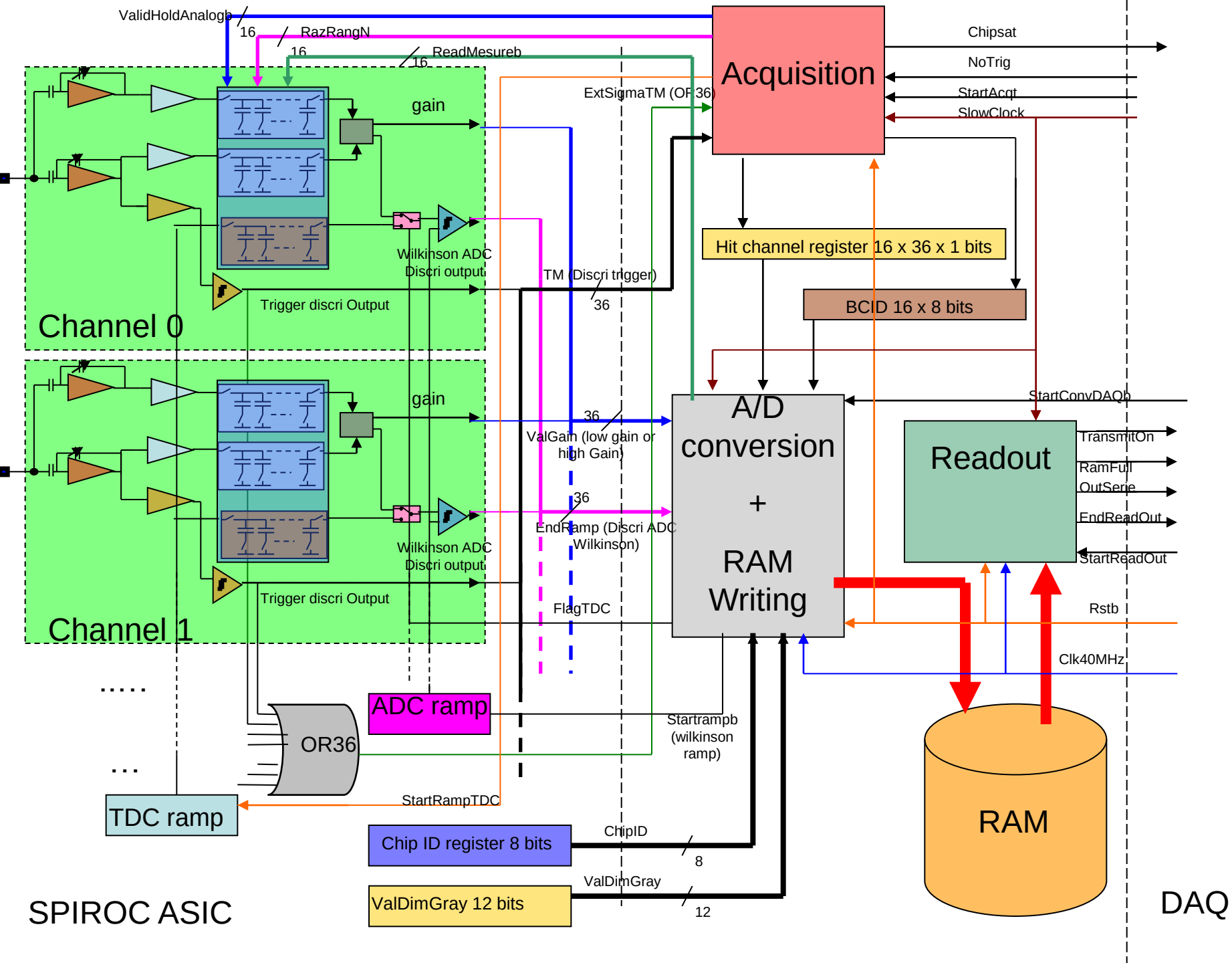
SPIROC main features

- **36-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits**
  - 2 gains (1-10) + 12 bit ADC : 1 pe → 2000 pe
  - Variable shaping time from 25 ns to 175 ns
  - pe/noise ratio : ~11
- **Auto-trigger on MIP or on single photo-electron**
  - pe/noise ratio on trigger channel : ~24
  - Fast shaper : ~10 ns
  - Auto-Trigger on 1/3 pe (50fC)
- **Time measurement :**
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step~1 ns TDC->TAC (fine time)
- **Other features:**
  - Analog memory for time and charge measurement : depth = 16
  - Low consumption : ~25 µW per channel (in power pulsing mode)
  - Individually addressable calibration injection capacitance
  - Embedded features (bandgap, 10-bit DAC, etc.)
  - Multiplexed analog output for physics prototype DAQ
  - 4kbytes internal memory and daisy chain readout

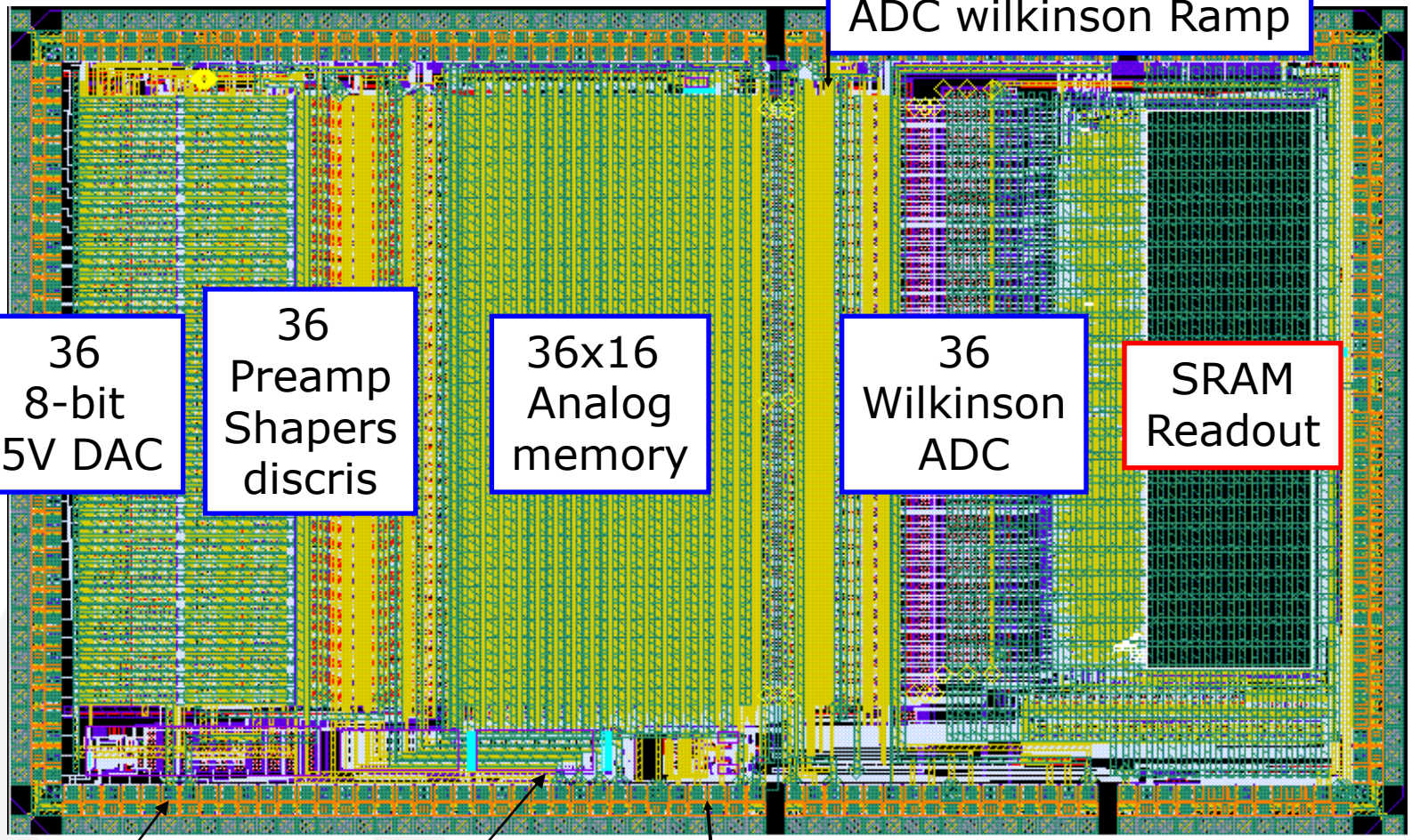


SPIROC : One channel schematic




ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
A/D conversion + RAM Writing
StartConvDAQb
Readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray 12 bits
ValDimGray
12
RAM
SPIROC ASIC
DAQ

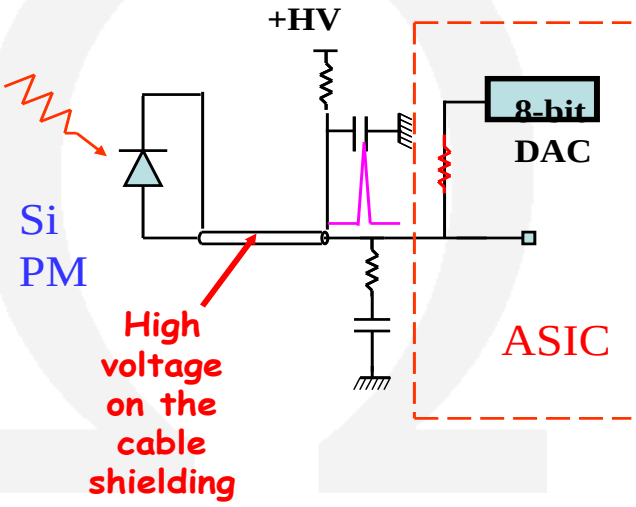
SPIROC layout

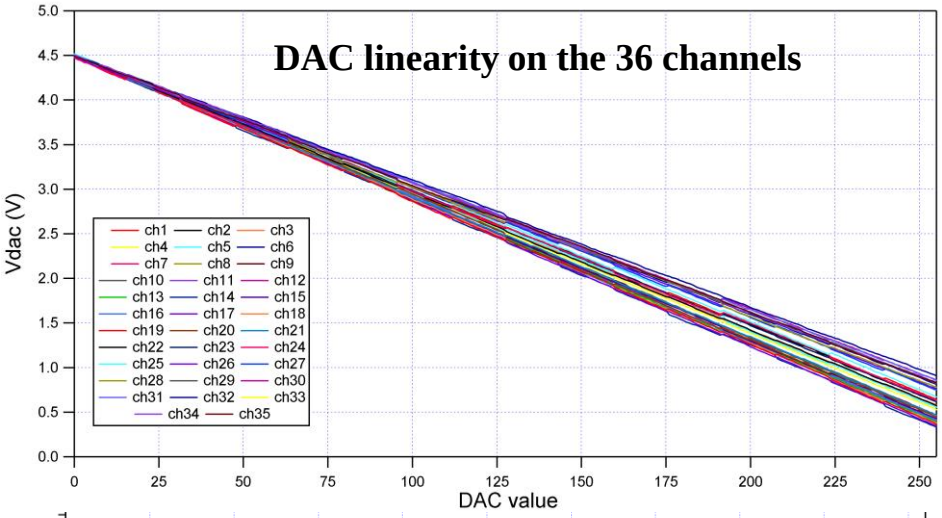


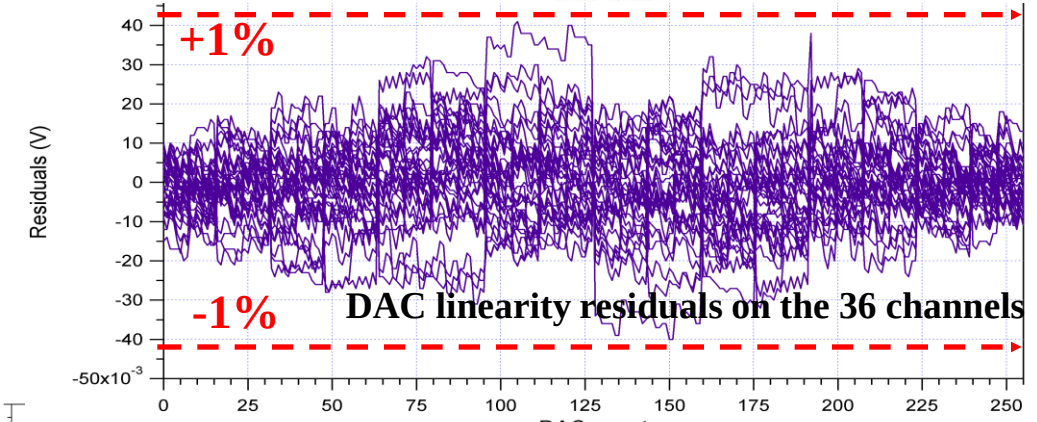
Fabricated in SiGe AMS 0.35 µm
Submitted in june 2007
Chip area : 32 mm² (4.2mm 7.2mm)

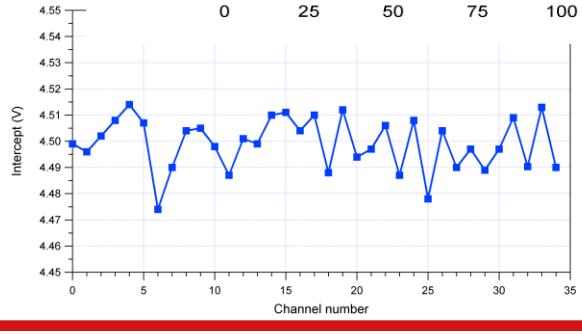
SPIROC Input DAC

- Input DAC to optimize SiPM bias voltage
- 8-bit DAC, 5V range
- LSB=20mV
- 36 DAC (one per channel)
- Ultra low power (<1µW) : no power pulsing
- Can sink 10 µA leakage current
- Linearity : ± 1%
- DAC uniformity between the 36 channels : ~3%



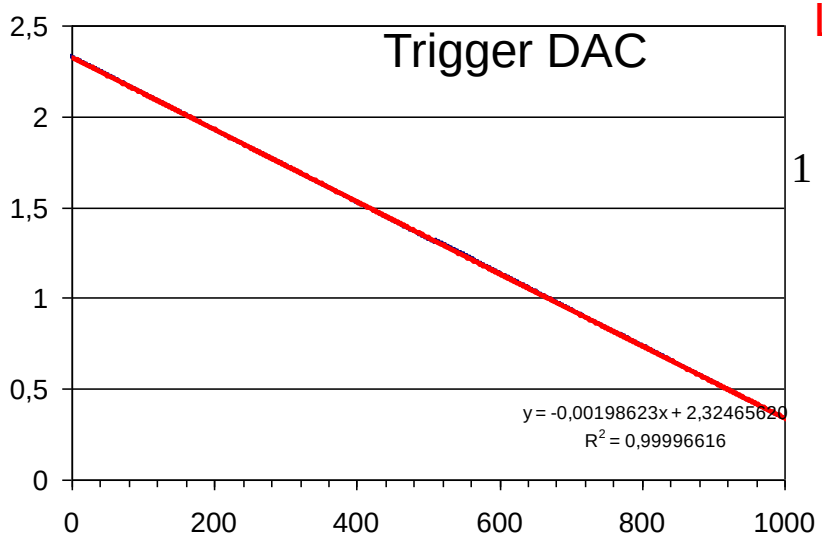






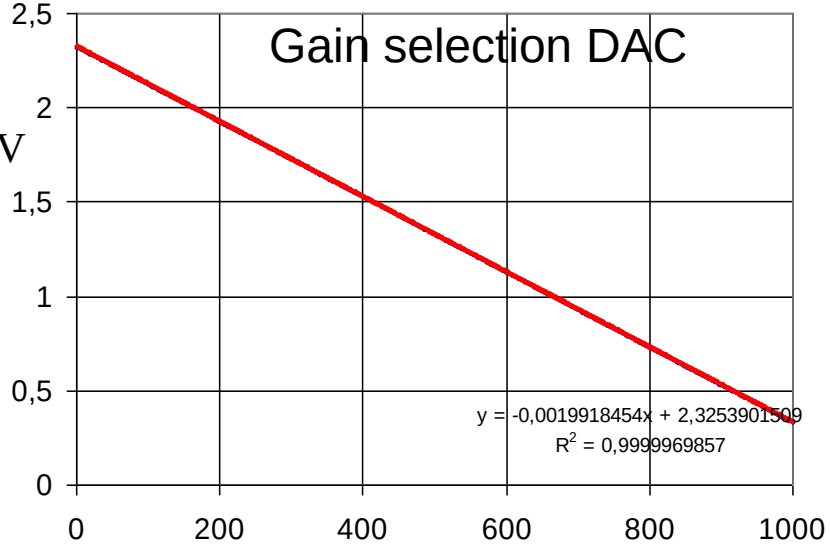
Trigger and gain selection DAC measurements

- Threshold 10-bit DAC linearity : typical ±0.2%

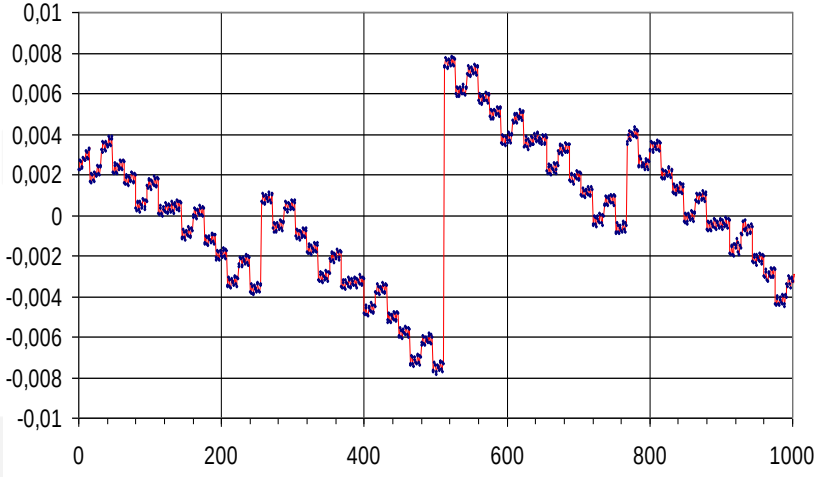


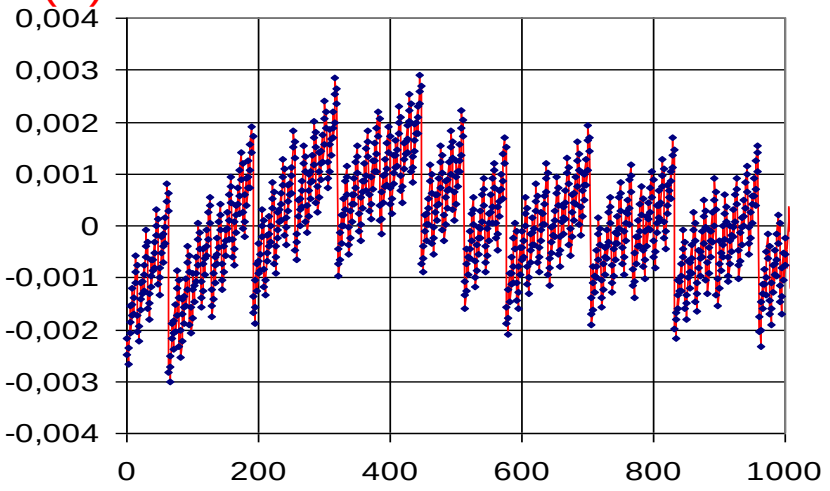
Linearity

1 LSB = 2 mV



Residuals (V)

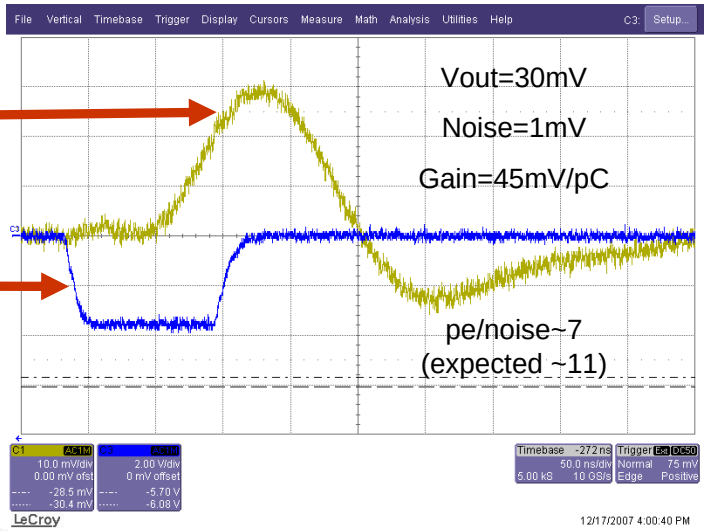




SPIROC charge measurement

High gain channel output

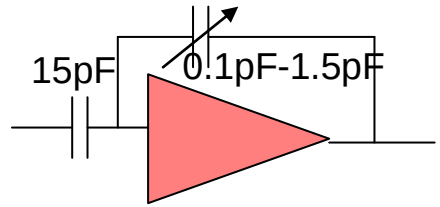
680fC (~4 pe @SiPM gain=10^6) in SPIROC



Set up:

Cf=400fF

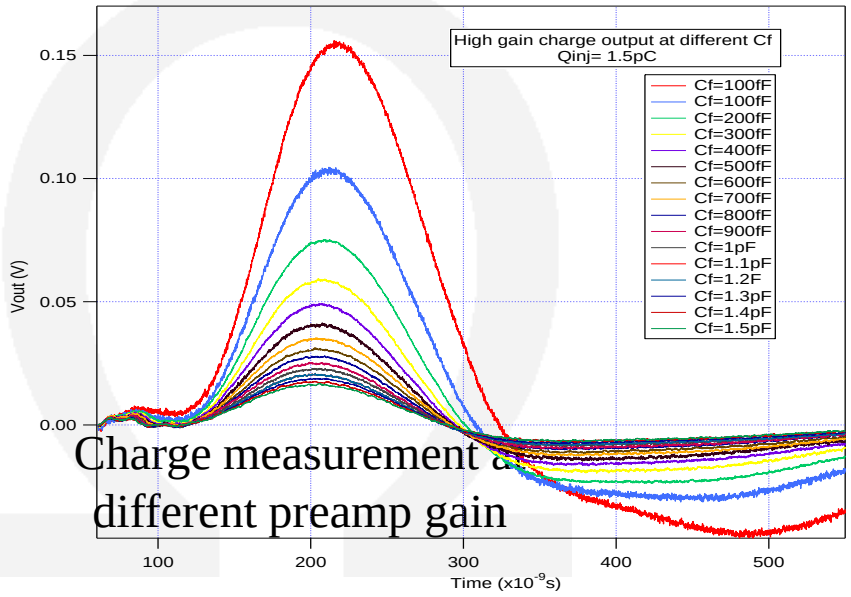
Tau=50ns



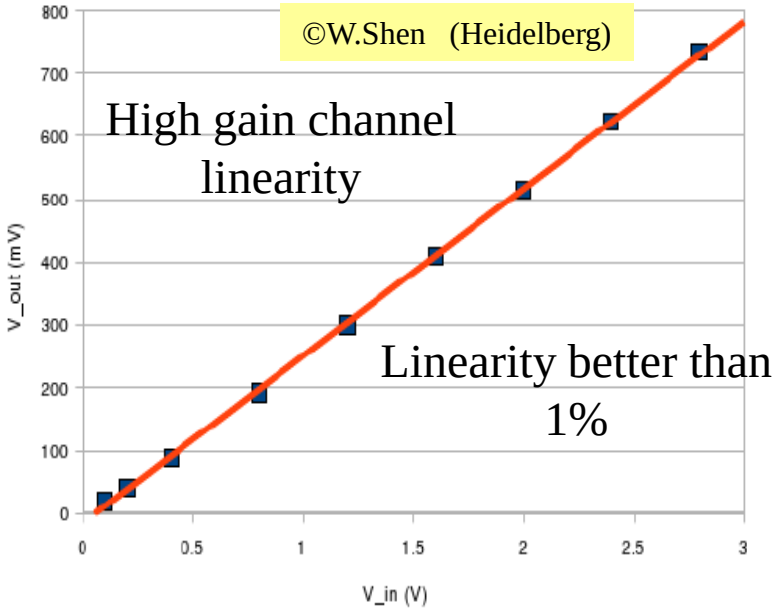
Low noise charge preamplifier capacitively coupled = voltage preamplifier

Preamp noise : 1.4 nV/sqrt(Hz)

Power : 2 mW (unpulsed)

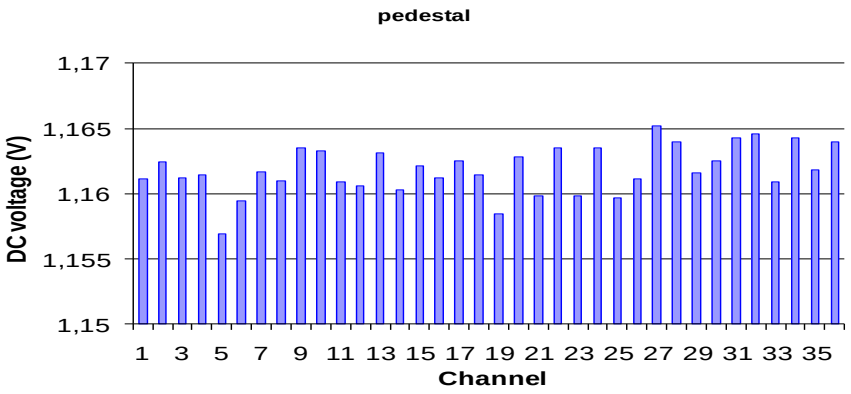


Cf = 700fF ,Tau=50ns Cc-100pF, 20dB

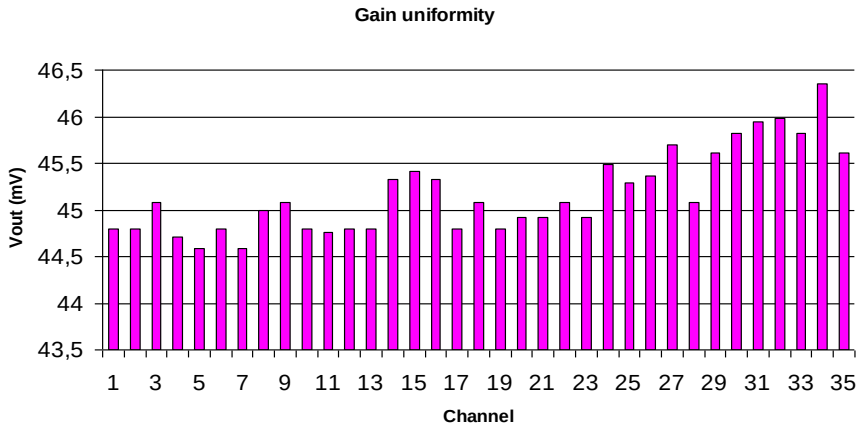


Other measurements

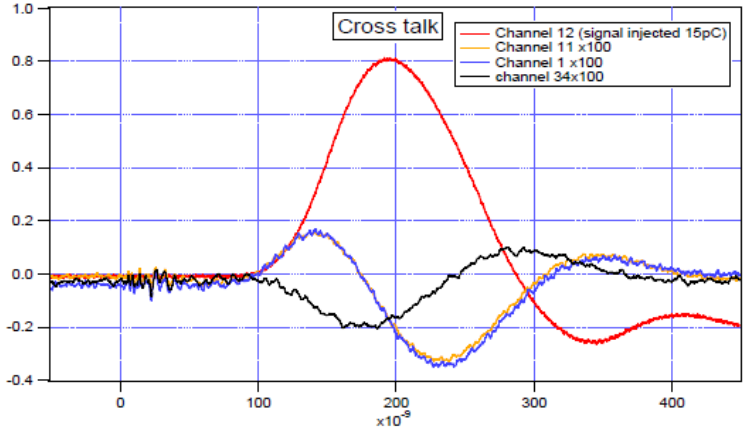
- **Pedestal uniformity**
  - **Mean= 1.16V; RMS = 1.8 mV**

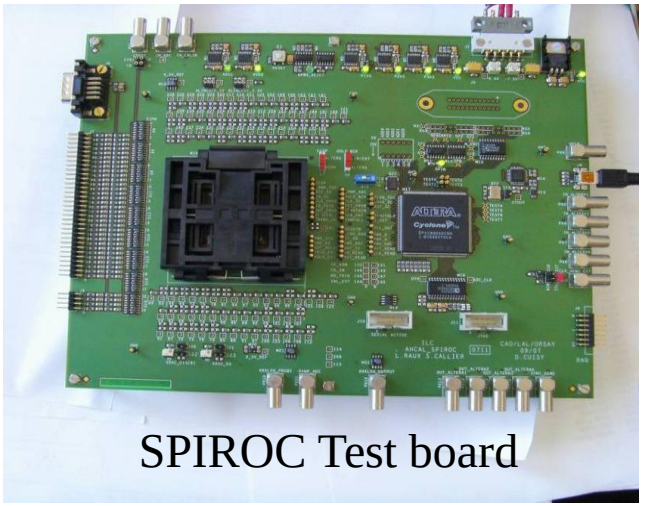


- **Gain uniformity**
  - **RMS 1%; 45 mV/pC (C_f=0.2pF, τ=50ns)**



- **Very low electronic cross-talk :** 0.3% (long distance cross talk due to slow shaper voltage reference: If this voltage decoupled with 100µF, it becomes negligible ~0.04%)





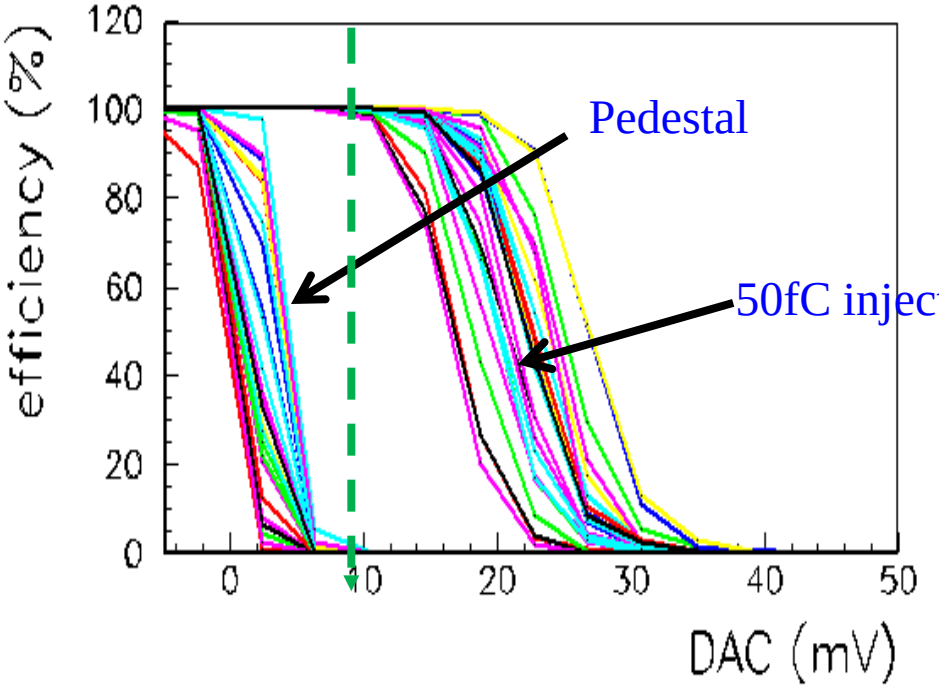
SPIROC Test board

Trigger efficiency

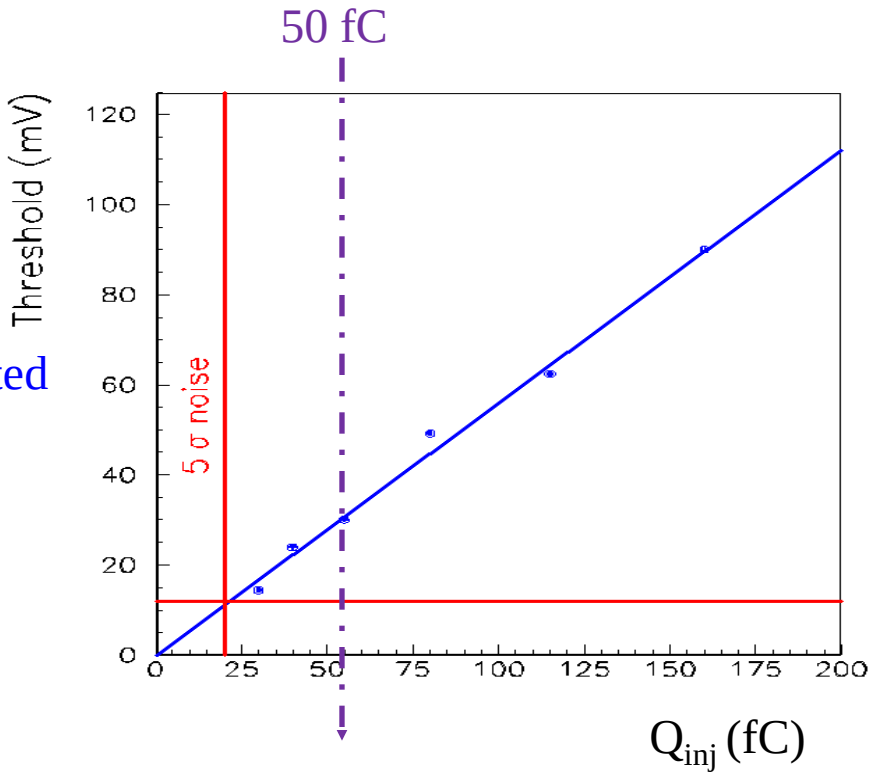
- S-curves : Trigger efficiency versus Threshold (1 LSB = 2 mV)
  - Good uniformity between channels

- Trigger at 50fC matched (1/3 photon-electron at 10^6)

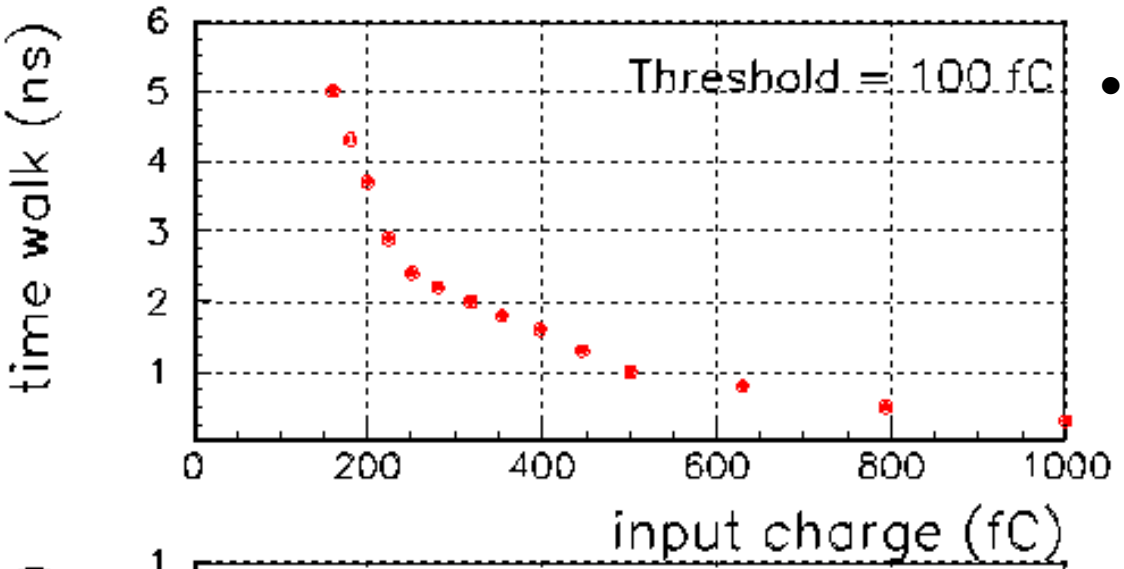
36-channel S-curves

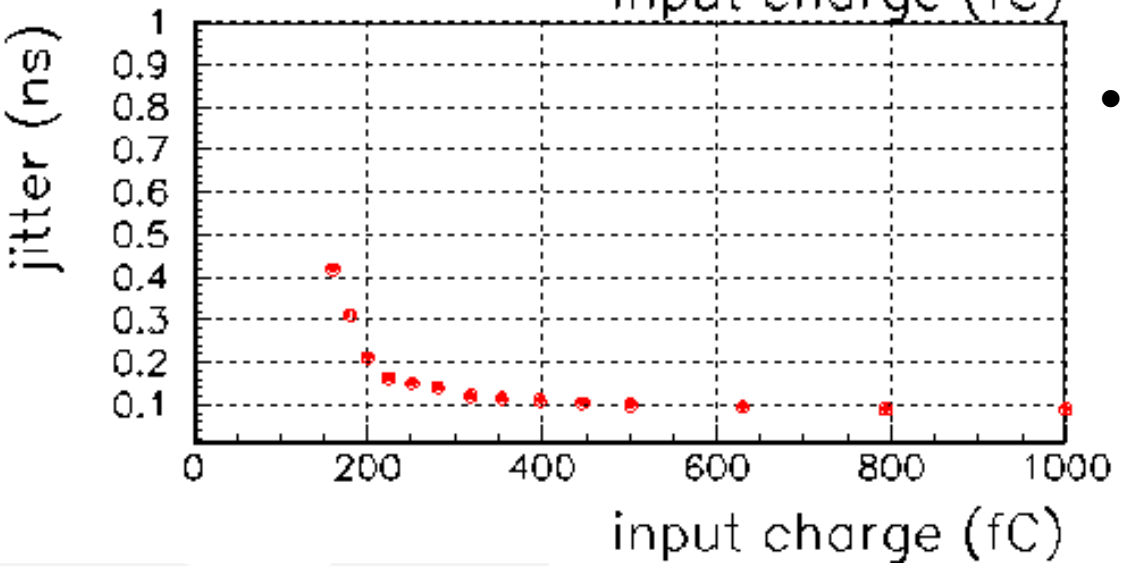


50 % Trigger efficiency point vs Q_{inj}



Time considerations : Trigger jitter and trigger time-walk

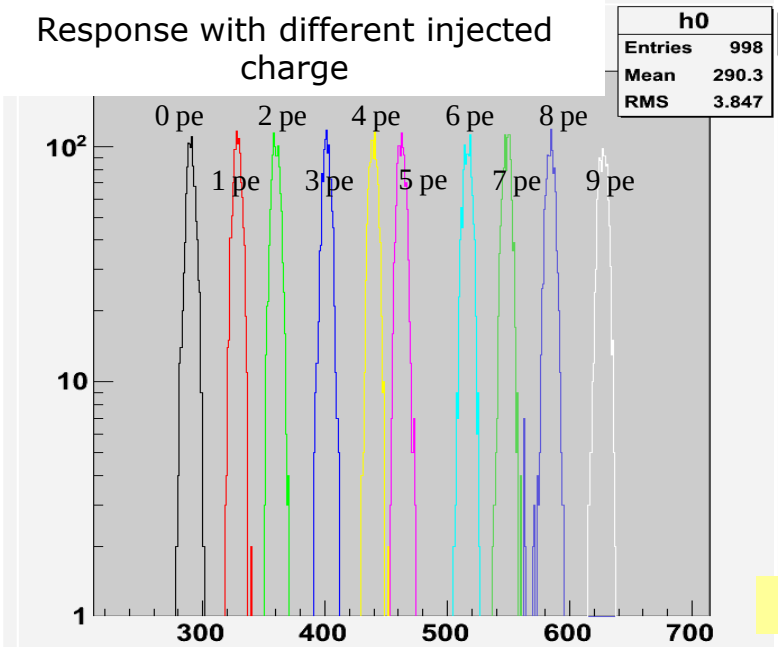


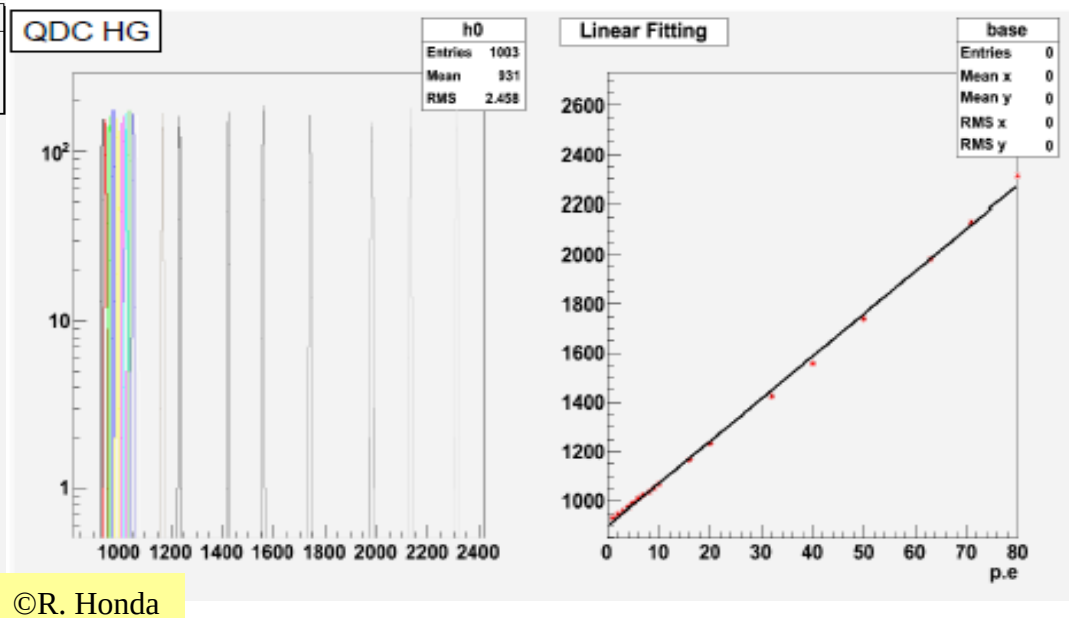


- Time walk: ~10ns
- Trigger jitter: ~100ps

Single photoelectron spectrum

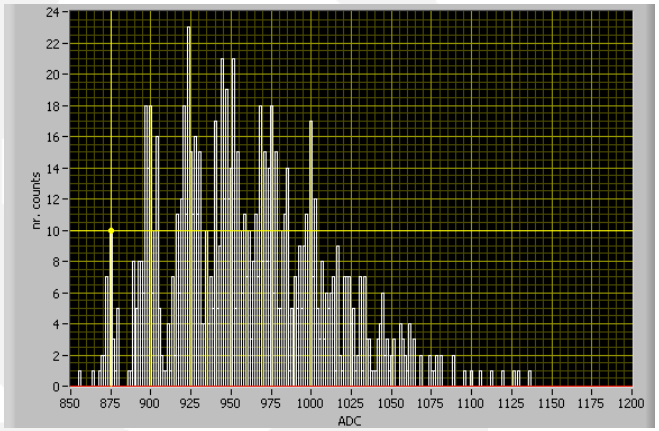
Response with different injected charge

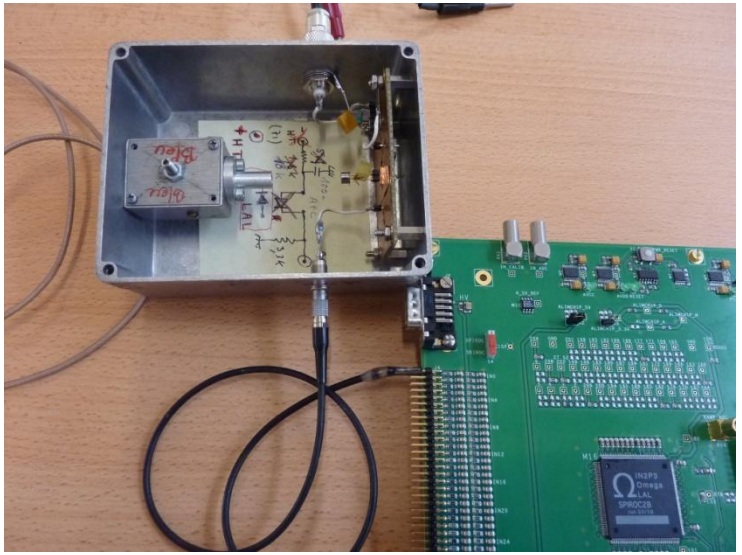




©R. Honda

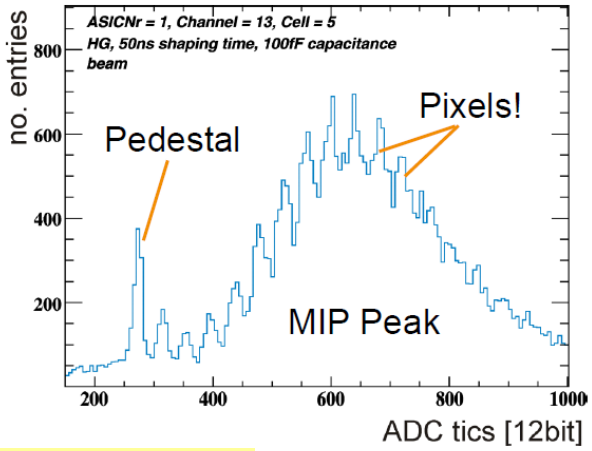
Setup: Autotrigger mode and internal ADC



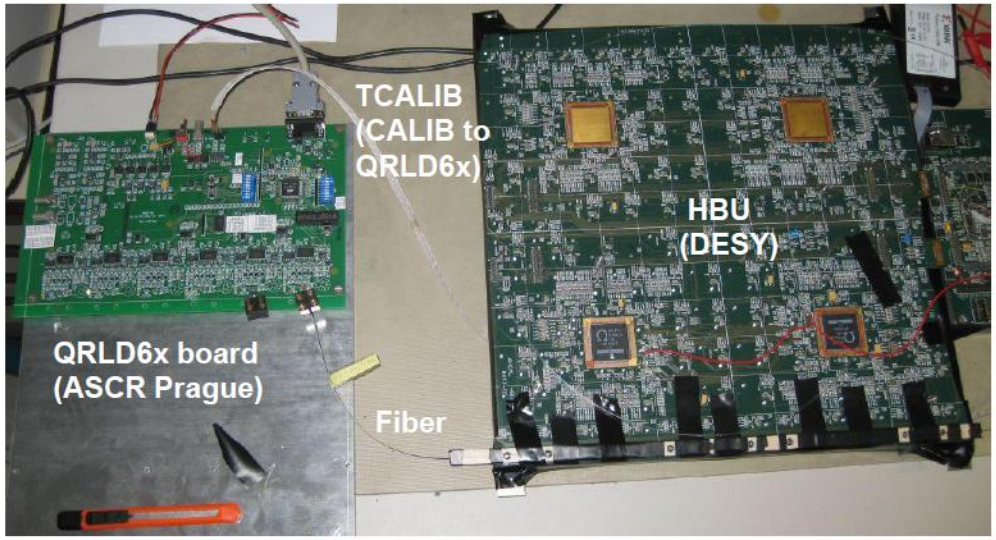


MIP response

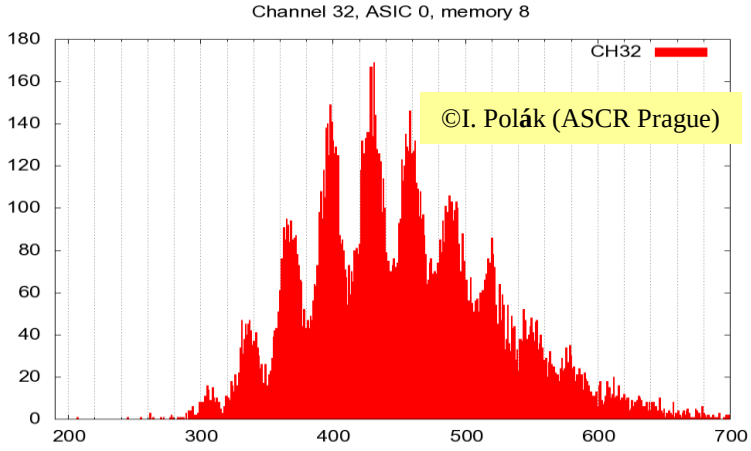
MIP response in DESY 6 GeV electron testbeam



©M. Reinecke (DESY)



Spectrum obtained with the LED calibration system



©I. Polák (ASCR Prague)

Summary and perspectives

- SPIROC is a versatile readout chip for SiPM photo detectors
- Laboratory tests have shown nice global functioning, especially on the charge measurement and auto triggering features.
- Some more tests have to be performed (time measurement, etc.)
- SPIROC 2 is produced in large scale in 2010 for the EUDET AHCAL module -> 1200 chips
- Development on SPIROC chip are on-going for ILC and also for other external requests (nuclear experiments, medical imaging, vulcanology, etc.)
  - More informations on Omega web site: http://omega.in2p3.fr

raux@lal.in2p3.fr

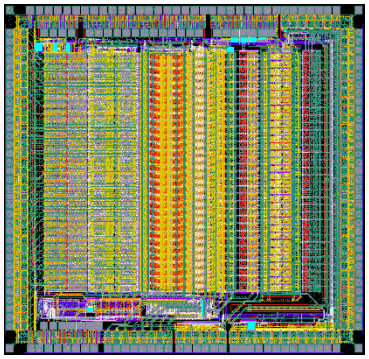
Thank you for your attention !!!

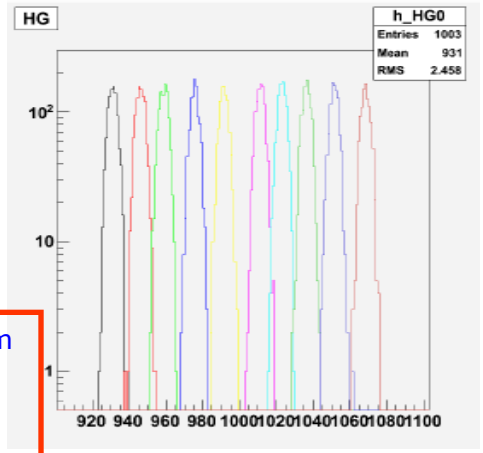
If you have questions or comments…

Backup slides

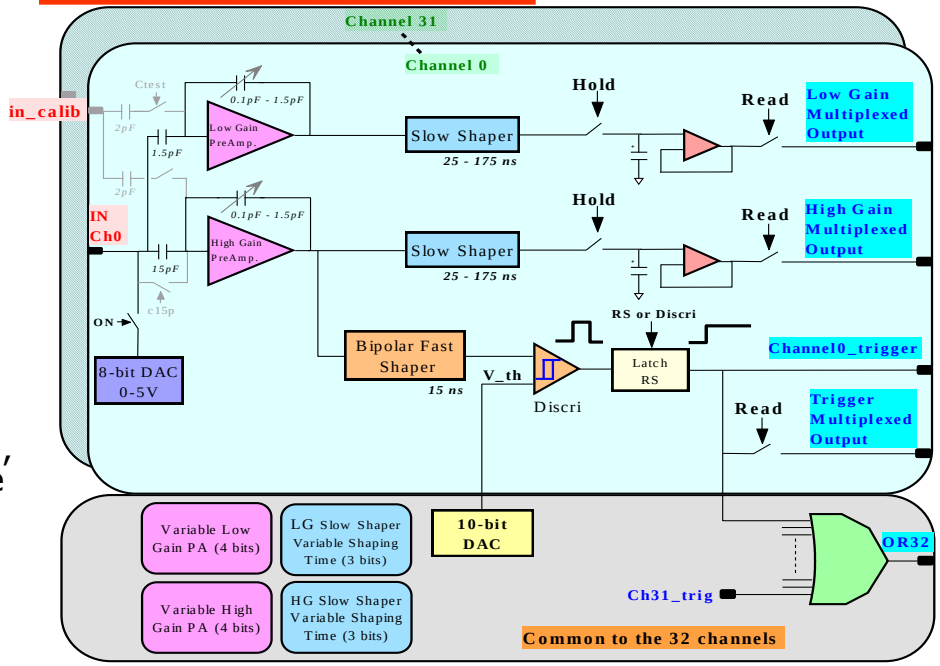
SPIROC A main features

- **Spiroc 0 motivations :**« light » analog version for users who don't need the digital core
- **32-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits**
  - 2 gains (1-10) 1 pe → 2000 pe
  - Variable shaping time from 25ns to 175ns
  - pe/noise ratio : 11
  - 2 Multiplexed outputs for low gain and high gain
- **Trigger output**
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Trigger on 1/3 pe (50fC)
  - 32 trigger outputs
  - OR 32 output
  - Trigger latch for each channel and multiplexed output
- Individually addressable calibration injection capacitance
- **Embedded features** (power pulsing, new bandgap, 10-bit DAC, possibility to disable each stage to save power when unused, high impedance outputs when inactive)





Fabricated in SiGe AMS 0.35 µm
Submitted in September 2009
Delivered in December 2009
Chip area: 17 mm² (4.2 mm 4.1 mm)



Engineering run

- **Reticle size : 18x25 mm2**
  - 50-55 reticles/Wafer
  - 25 wafers needed
- **Final arrangement:**
  - **« Calice » chips produced:**
    - 7 Hardroc 2b => ~9000 chips
    - **1 Spiroc 2a** => ~1200 chips
    - **1 Spiroc 2b** => ~1200 chips
    - 1 Skiroc 2 => ~1200 chips
  - **Additionnal chips produced:**
    - 1 Spaciroc : JEM EUSO experiement => ~1200 chips
    - 1 Maroc 3 : for PMT readout => ~1200 chips
    - **3 Spiroc 0** => ~3600 chips
- **Production run launched in April 2010**
- **Delivery in September 2010**