# Developments for the upgrade of the CMS HCAL front-end electronics

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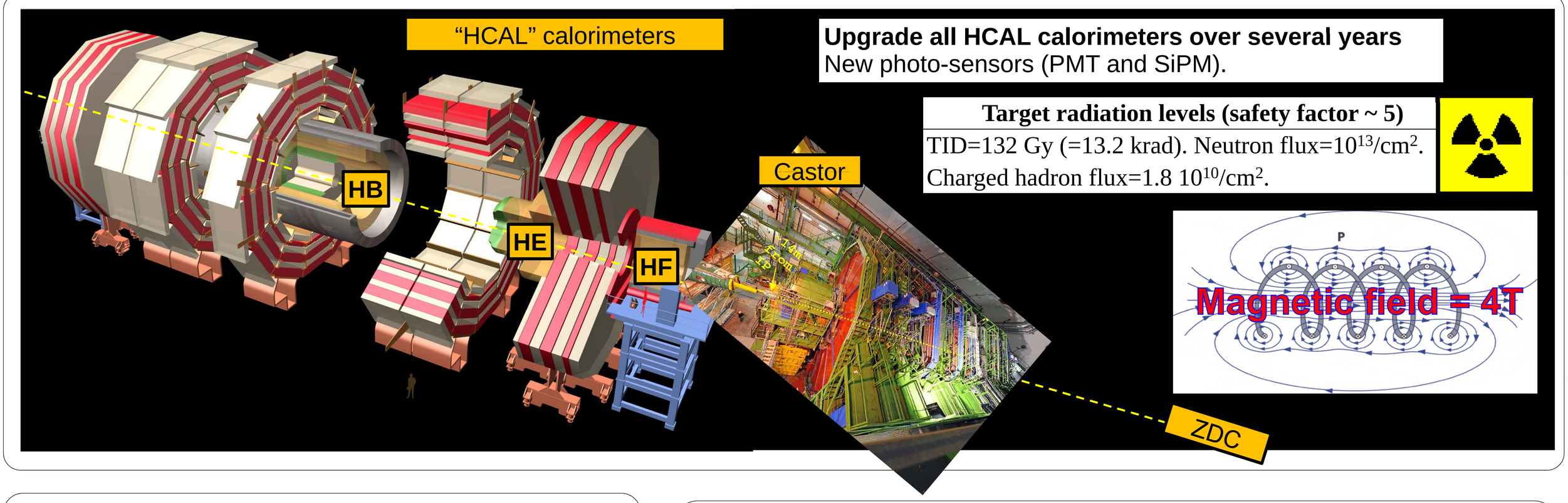
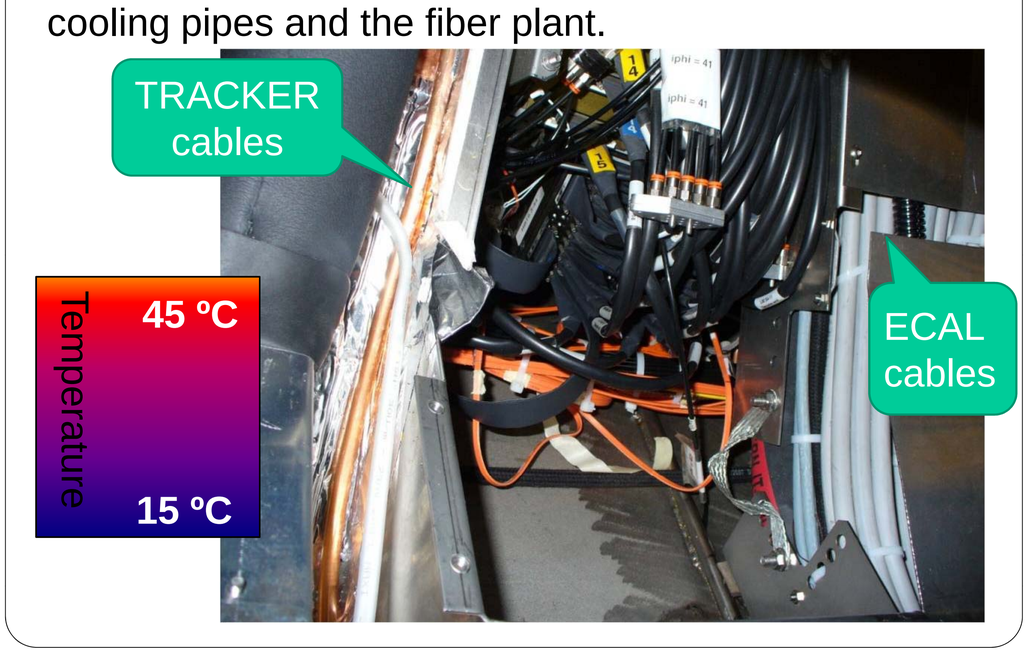
***Abstract:*** We present a scheme to upgrade the CMS HCAL front-end electronics in 2015. The HCAL upgrade is required to handle a major luminosity increase of LHC which is expected for 2016. We describe the requirements for the new electronics and on the proposed solutions. The requirements include increased channel count, additional timing capabilities, and additional redundancy in a harsh environment which is constrained by the existing system. The proposed solutions span from chip level to system level. They include the development of a new ADC ASIC, the evaluation and use of circuits from other developments, evaluation of commercial FPGAs, better thermal design and improvements in the overall architecture.

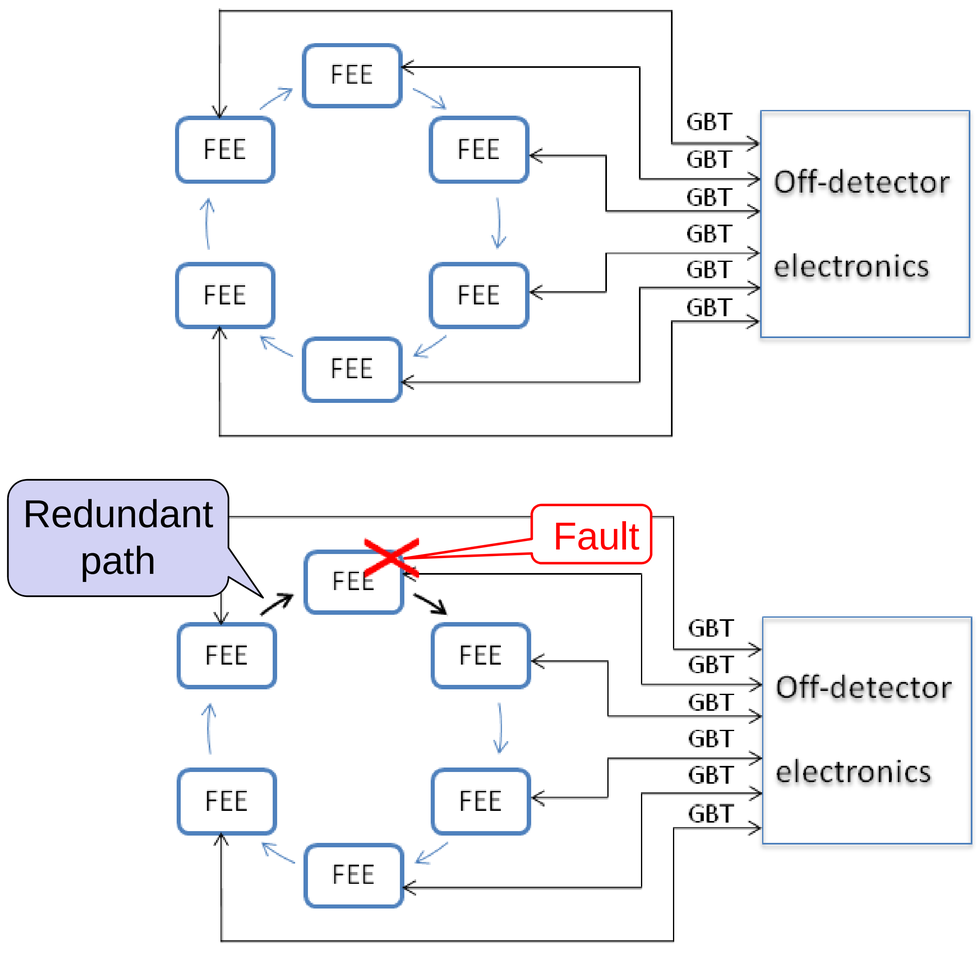



## Constraints

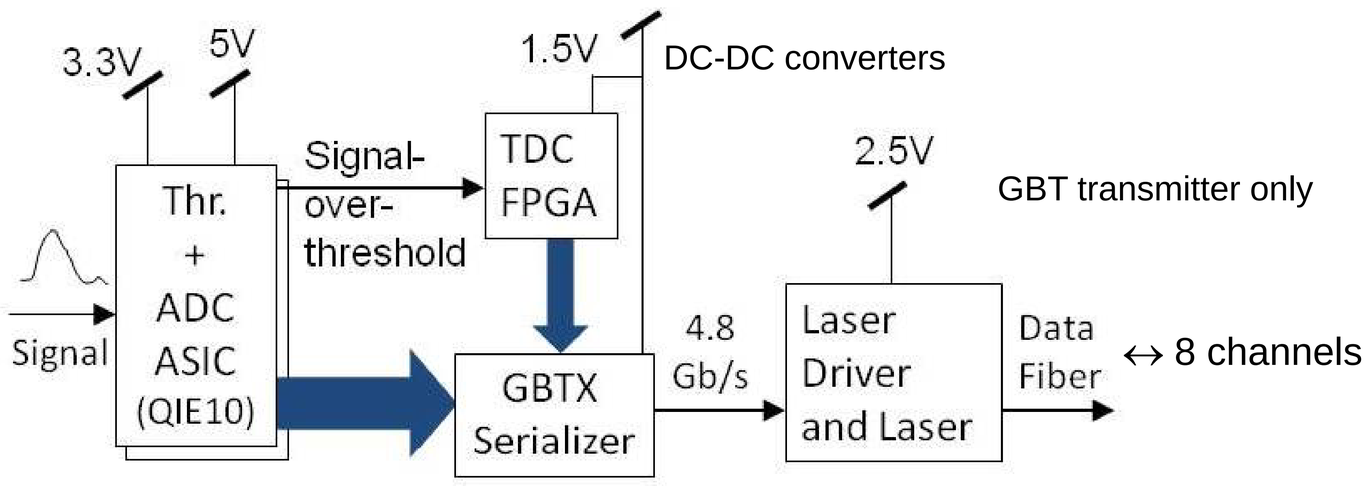
Readout Box: blocked under other CMS cables → only individual modules are swappable.
Must keep the existing infrastructure: power cables, cooling pipes and the fiber plant.




## Redundant control paths




## Readout Path




1. QIE10: new ASIC for charge-integration, ADC, encoding. Input impedance and sensitivity (3fC) matched to the new photo-sensors over a greater dynamic range (330pC)
2. TDC resolution ~2ns (compare to the existing timing of 25ns). Implementation on Igloo Actel FPGA
3. Limited bandwidth →

**optimize the algorithm in the experiment !**

## Thermal design

**Cooling**: only by contact with the metal enclosure of the Readout Box.
PCB with exposed metal around the edge of the board on every other layer of the board. Some of the layers have a copper ring that come out to the edge of the board and are all connected with vias. Other layers are interleaved and transfer heat from the core of the board to the ring.