



# Very low power, High Voltage base for a Photo Multiplier Tube for the KM3NeT deep sea neutrino telescope.

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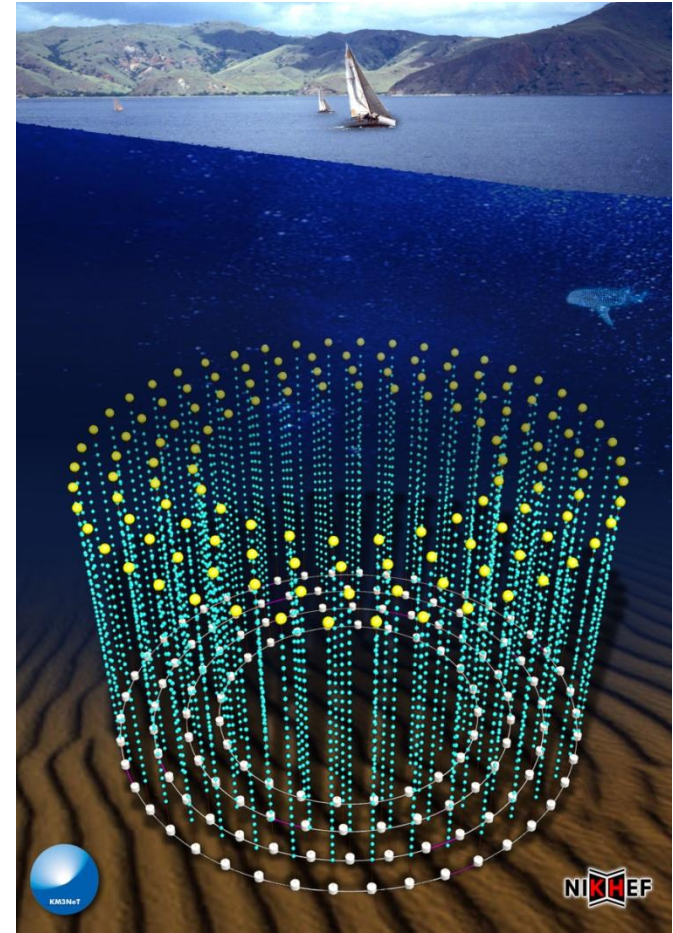
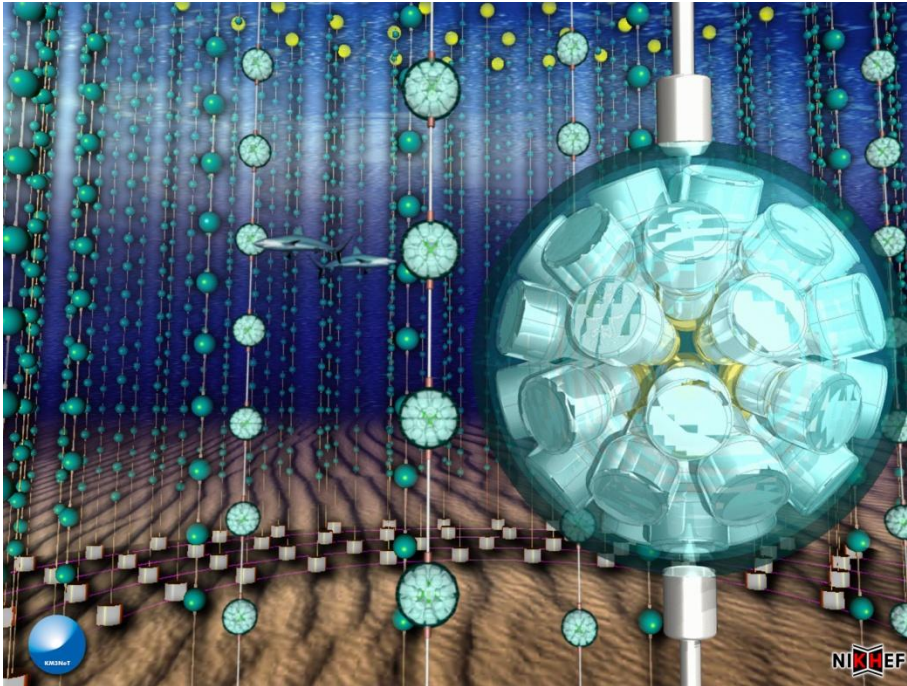


# Outline

- Design requirements for the high voltage circuit board.
- System overview.
- HV generation.
- Diagram.
- Where will these high voltage circuit boards being used.
- Measurement results.
- Prototype of the high voltage circuit board.
- Summary



# Multi PMT Optical Module system for detection of neutrinos



Location: Seabed of the Mediterranean Sea.  
Embracing: several cubic kilometers of  
seawater, max. 5000 meter depth.  
Number of optical modules: 12000  
Number of PMT's: 372000

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# What is KM3NeT

- **KM3NeT** is an acronym for cubic kilometre size (**KM3**) **N**eutrino **T**elescope and will host a neutrino telescope in the form of a water Cherenkov detector with a volume of at least one cubic kilometre.
- KM3NeT will search for neutrinos from distant astrophysical sources like gamma ray bursts, or colliding stars.
- An array of thousands of optical sensors will detect the faint light in the deep sea from charged particles originating from collisions of the neutrinos and the Earth.
- For the detection of this faint light (photons), Photon Multiplier Tubes will be used. 31 PMT's will be housed in a single Optical Module. A total of 300 detection units arranged in a string with 20 optical modules will be deployed.



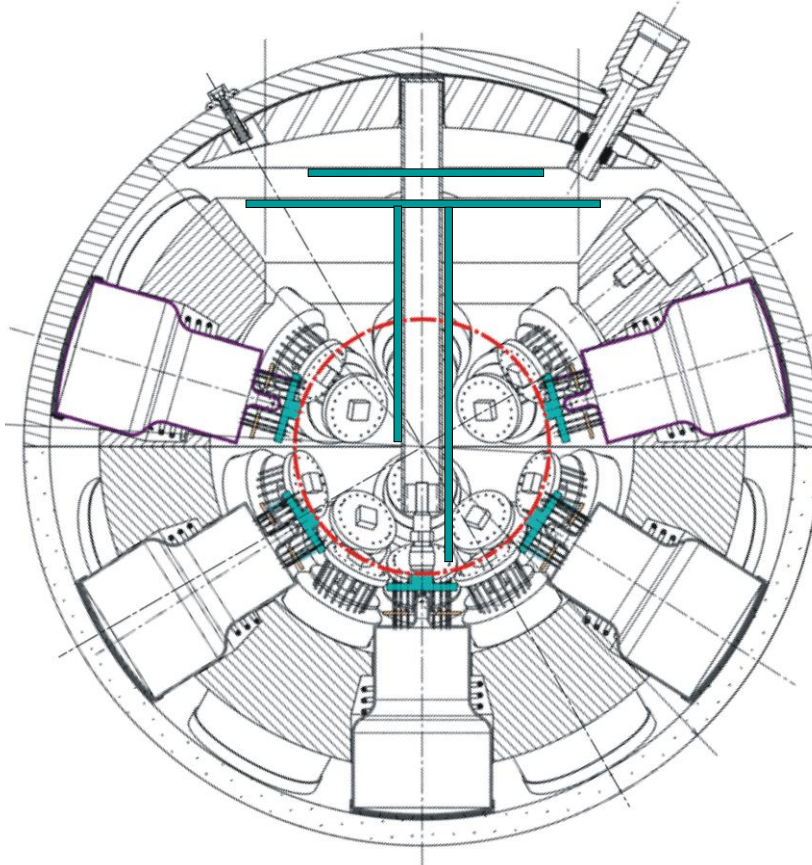
# Detecting photons caused by neutrinos.

- Photons caused by neutrinos are masked by background photons.
- Background photons come from decay of potassium 40 in the water, the glass of the sphere and the glass of the PMT itself.
- These photons are detected by the PMT's as single photons.
- Bioluminescence is also a source of photons.
- PMT's will have a their own dark count (caused by thermal electrons)
- Consequently, all PMT's generate random signals.
- Selecting the signals caused by neutrinos in the huge dataflow will be a defiant job.



# Optical Module

Vitrovex sphere 17 inch



12 PMT's in the upper half of the optical module  
19 PMT's in the lower half of the optical module

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# Design requirements for the high voltage circuit

Every PMT must give the same output signal as it is hit by a single photon. The gain of a PMT depends on the level of the supplied high voltage.

The HV for each PMT needs to be individually adjustable. Consequently **each PMT gets its own HV circuit board.**

Limited space in the OM available. Only in the centre of the sphere is room for the electronics. Consequently **limited board space.**

Heat dissipation must be kept to a minimum. No active cooling in the sphere available. The produced heat has to be transferred through the glass to the seawater. Consequently **low dissipation.**

Good design rules imply also low ripple and low RFI generation.

Be aware, if the circuitry dissipates e.g. 0.5 W more, 180 kW extra has to be transported over 100 km from shore to the detector.



# PMT global specifications

The detector will be designed for a lifetime of 15 years.

The lifetime of a PMT depends on the maximum amount of charge the anode can supply.

Because of this property a low gain PMT has been chosen.

A low gain PMT means a dedicated pre amplifier.

## Cathode characteristics

Radiant blue sensitivity at 470 nm > 130 mA/W

QE at 470 nm > 20%

Non homogeneity of cathode response target +/- 10%, +/- 20% acceptable

## Characteristics with voltage divider

Maximum supply voltage 1400 V

Maximum Gain  $5 \cdot 10^6$

External electro static coating to the cathode

## Anode characteristics

Dark count < 500Hz at 15 °C, > 0.3 pe threshold

Pulse rise time < 3 ns

Duration at half height 5 ns FWHM at single photon

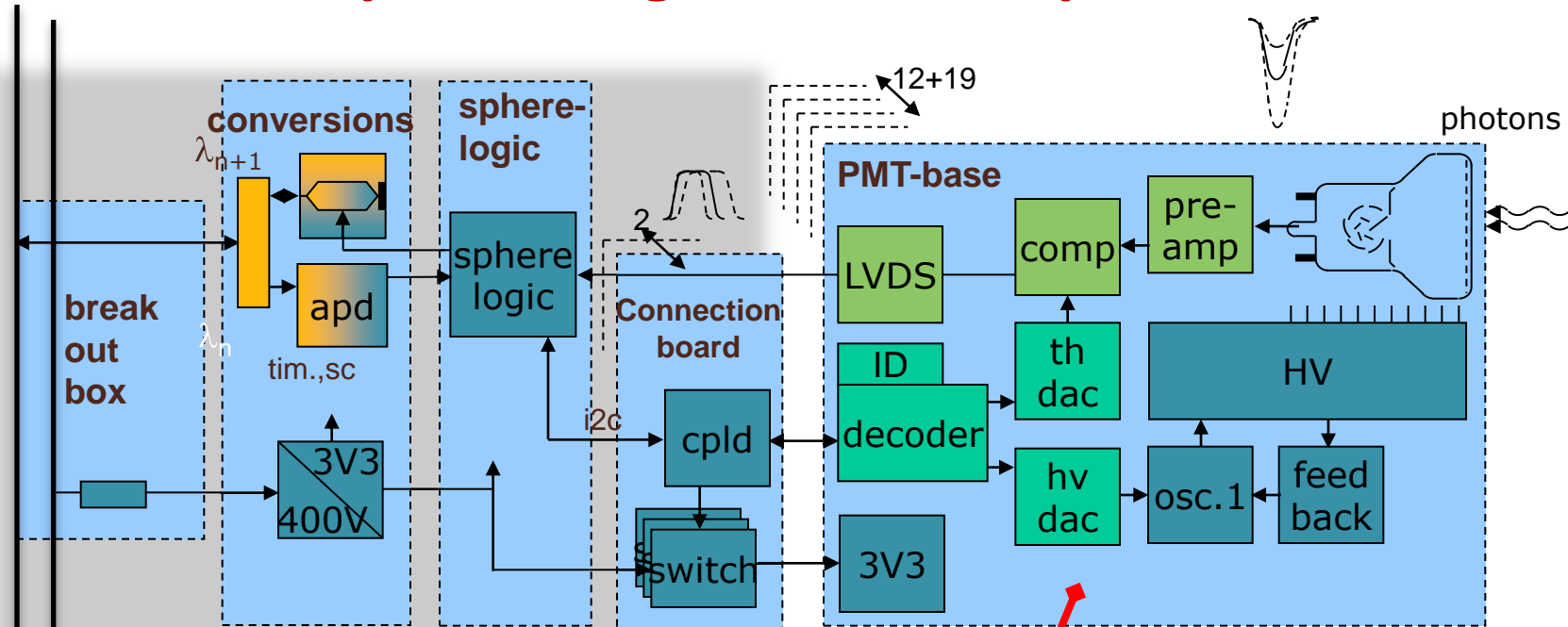
Transit time spread < 2 ns sigma

Peak to valley ration 3, typical 2





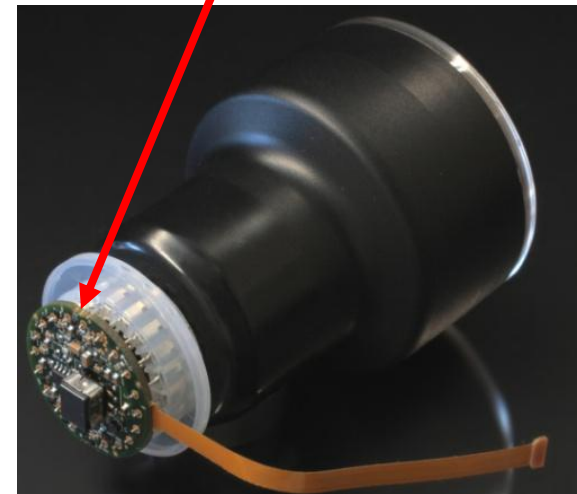
# Electrical/Optical Diagram of the Optical Module



Vertical Electric Optical Cable



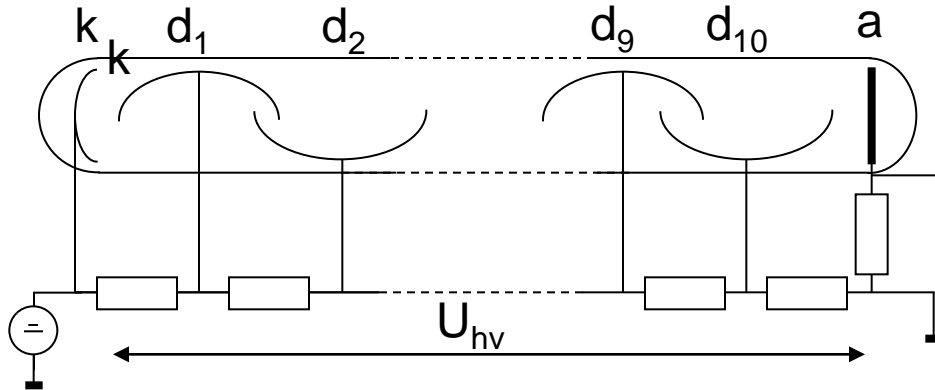
375V



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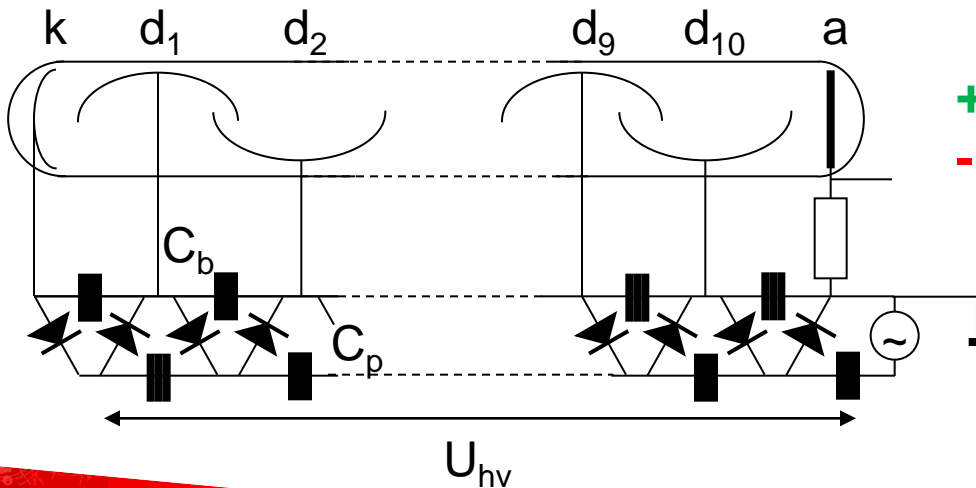
# HV generation 1

## Resistor Base



- 'High' power dissipation
- Temperature Sensitive output voltage
- Bigger volume then CW base
- DC current 10 times anode current

## Cockroft Walton base

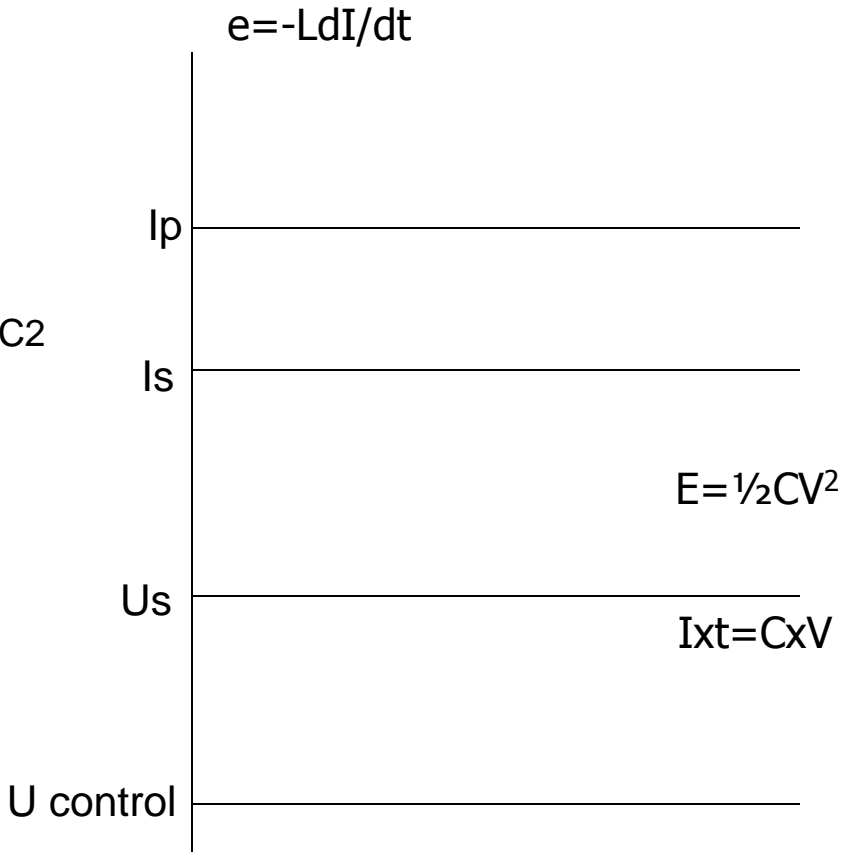
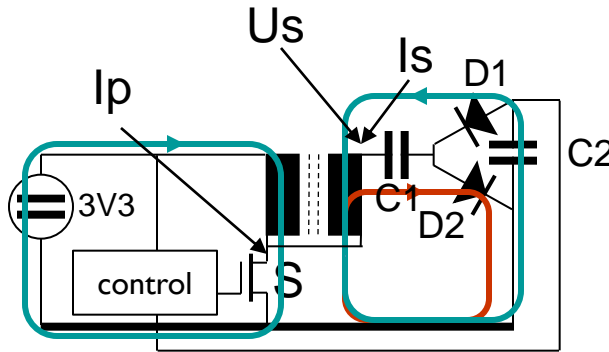


- + : Low power dissipation then RB
- : Fixed voltage ratio  
no DC current

# HV generation 2



Fly back principle

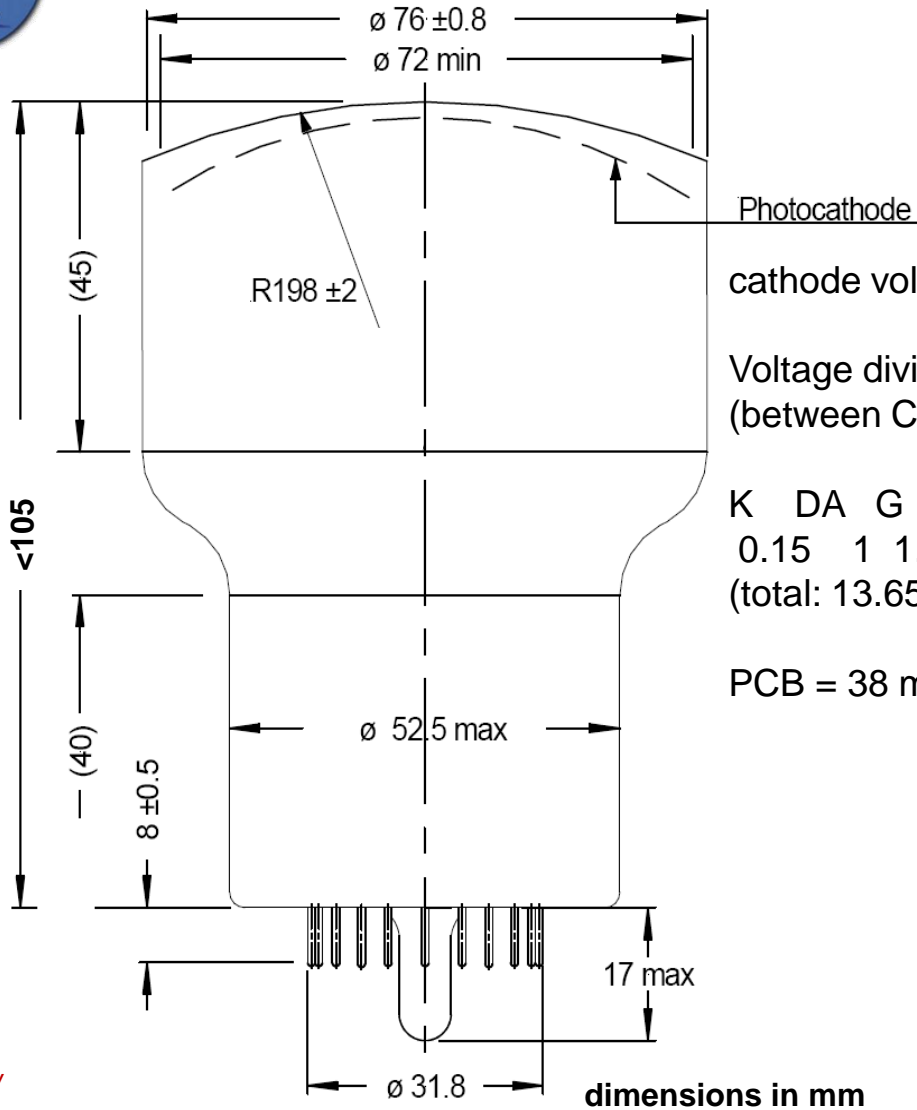


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# PMT proposed form factor



cathode voltage -800 - -1400 V

Voltage dividing ratio  
(between Cathode and Anode Photonis XP53B20)

K	DA	G	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	A
0.15	1	1.5	2	1	1	1	1	1	1	1	1	1	1
(total: 13.65)													

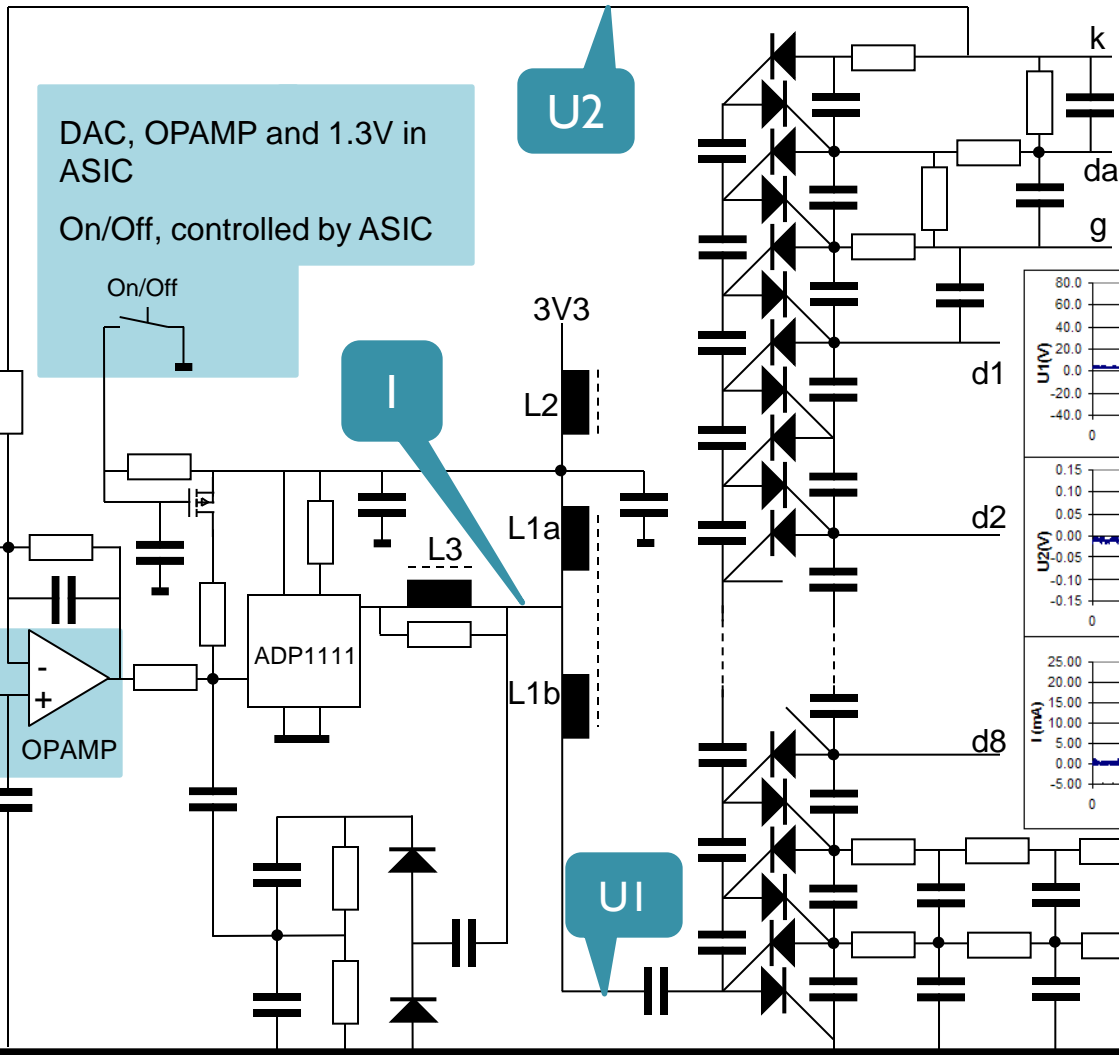
PCB = 38 mm $\varnothing$

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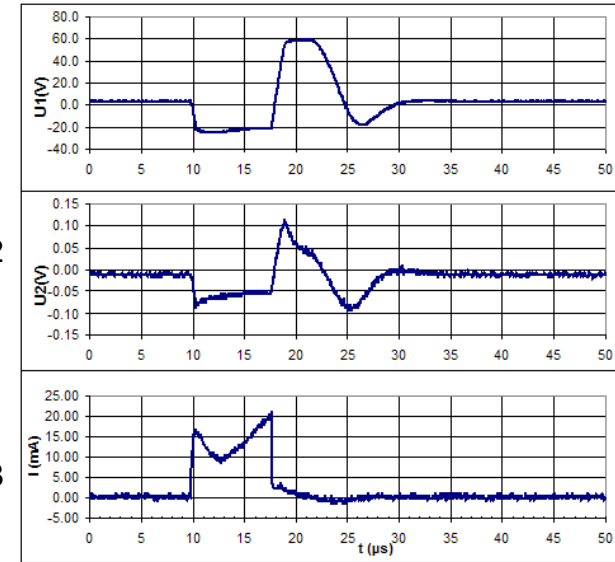


# Diagram



DAC, OPAMP and 1.3V in ASIC  
On/Off, controlled by ASIC

- Component choices,  
-Transformer core  
-Diode switching characteristics  
-Control IC  
-ASIC, low dissipation, less space



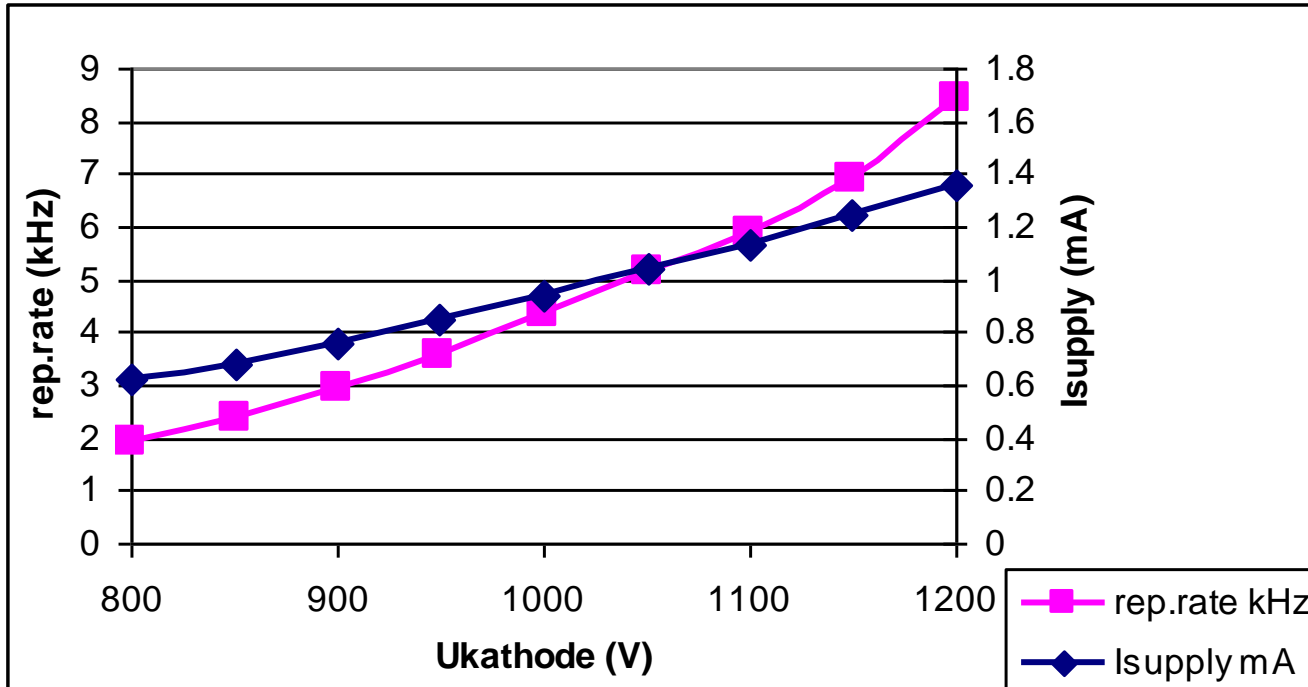
Pre Amp  
Comparator  
LVDS Driver

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# HV versus frequency and I<sub>supply</sub>

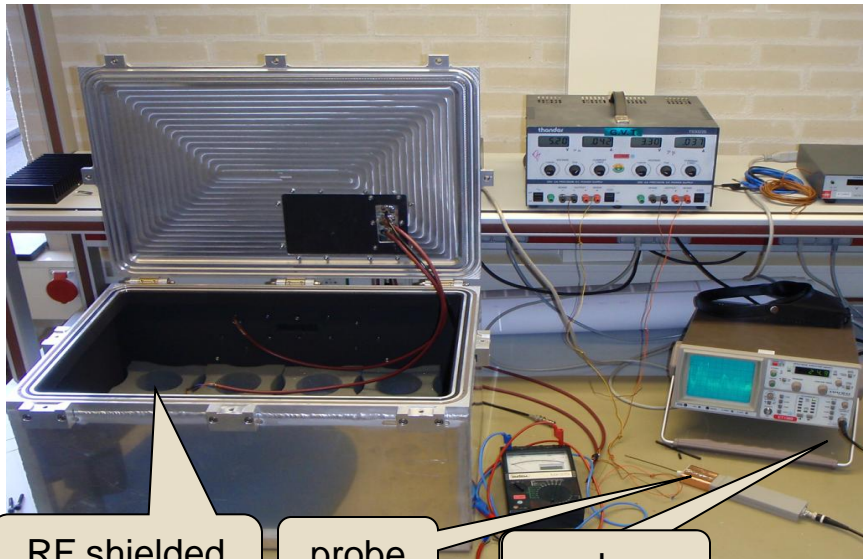


Power and frequency

2 - 9 kHz at 800 - 1200 V

0.6 - 1.4 mA<sub>3v3</sub> at 800 - 1200 V (0.66mW-4.6mW)

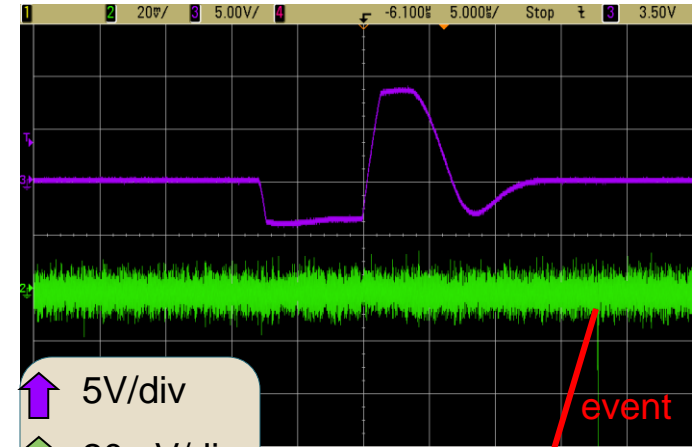
# EMC



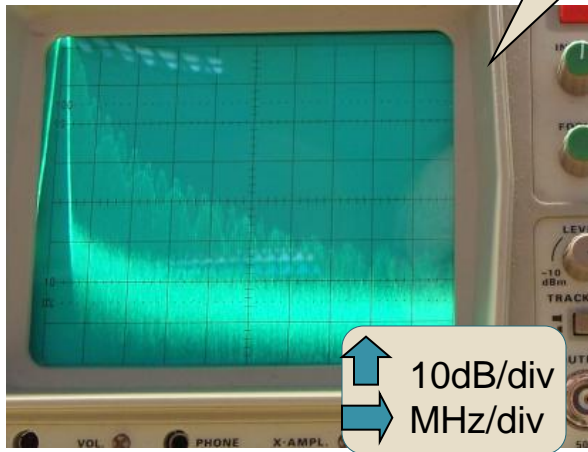
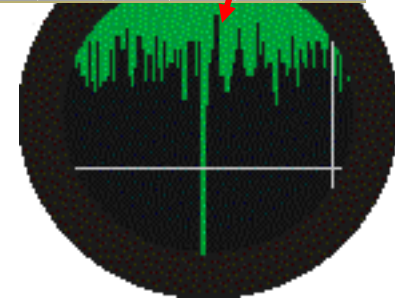
RF shielded box

probe

analyzer



5V/div  
20mV/div  
5μs/div



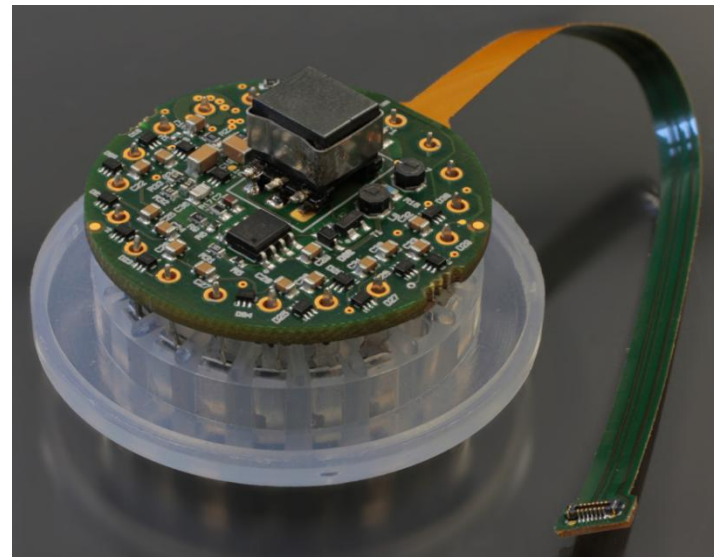
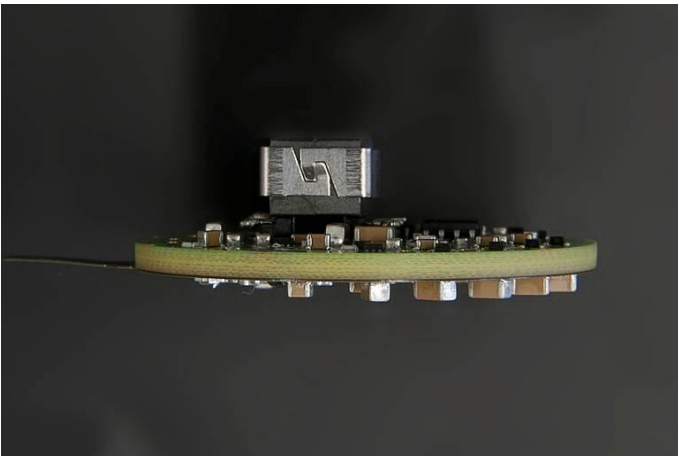
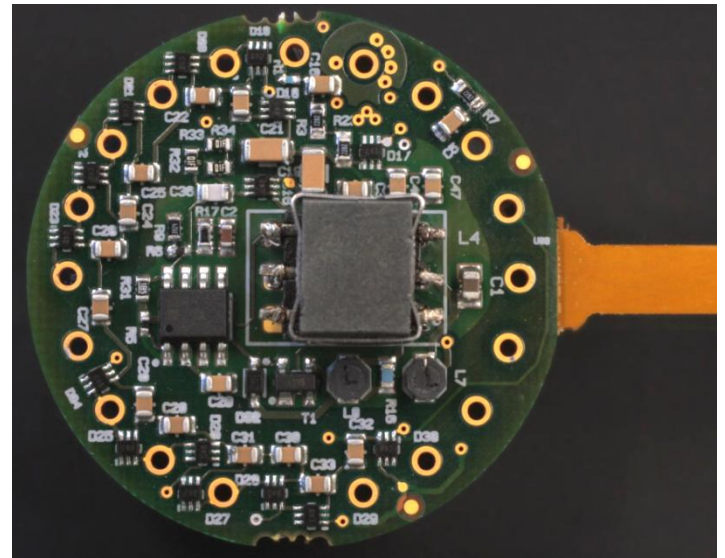
10dB/div  
MHz/div

RFI -20 dB @ 150 kHz-10 MHz

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# PMT and HV circuit

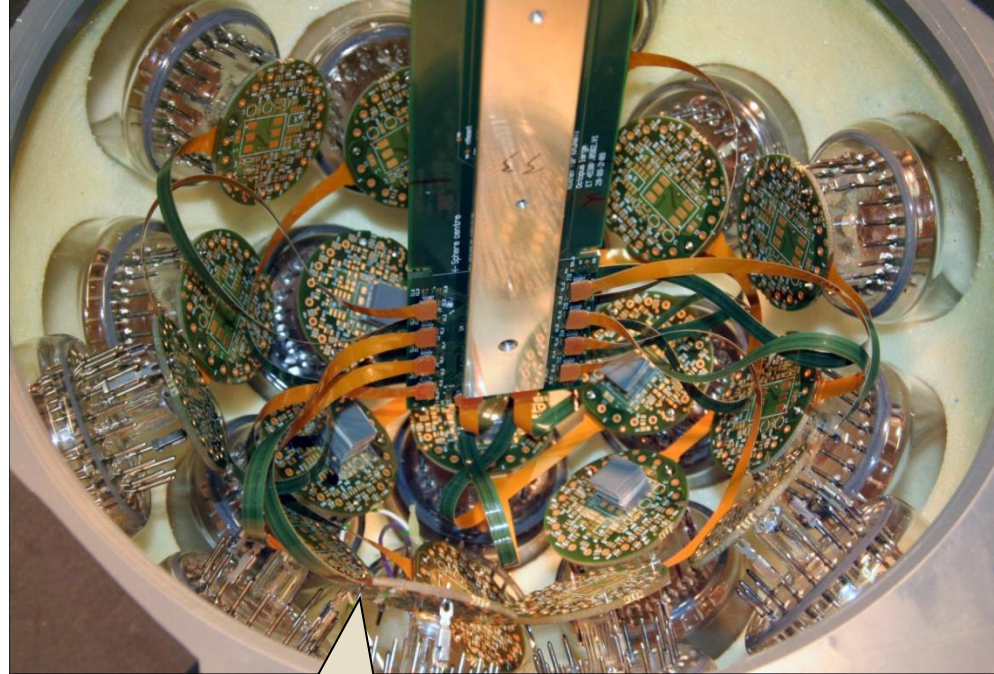
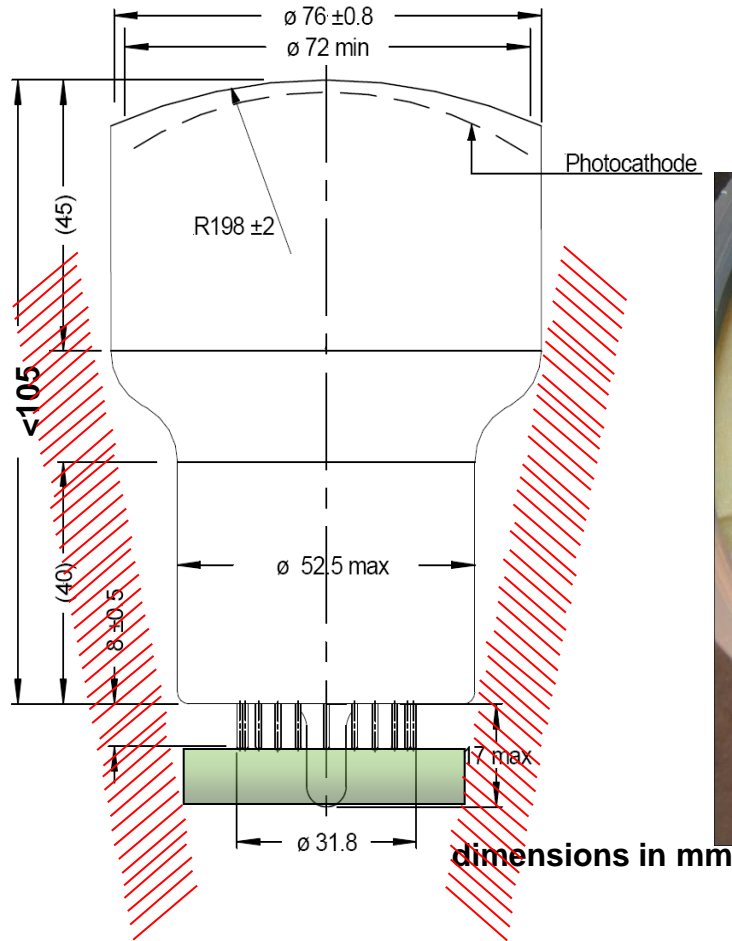


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# Form factor mostly dictated by PMT

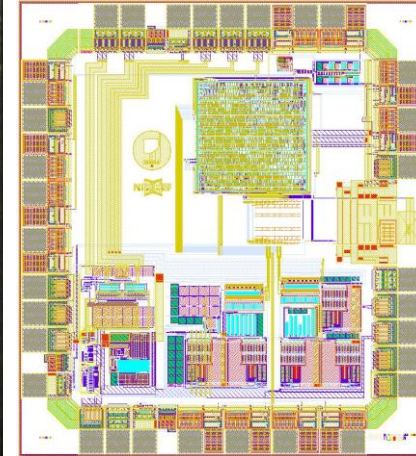
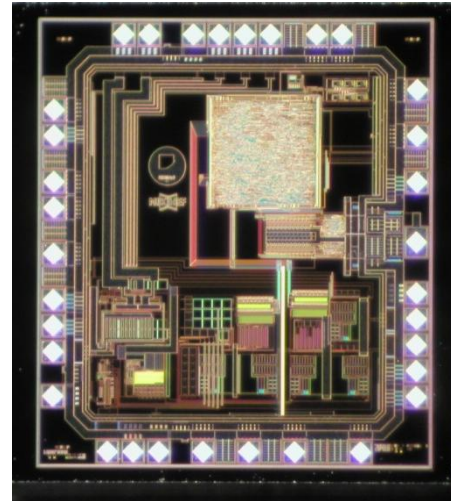
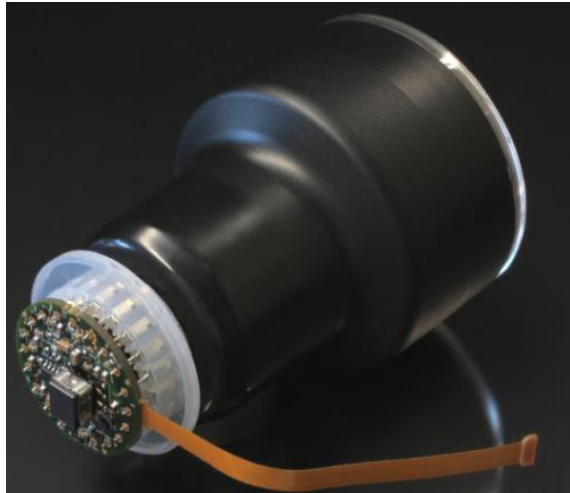


PCB space

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# PMT base



Digital part  
Identifier  
Analogue part

$V_{\text{ripple}} 706 \text{ mV}_{1056}$      $8.5 < T(^{\circ}\text{C}) < 22.1$   
 $V_{\text{ripple}} 0.07\%$      $8.5 < T(^{\circ}\text{C}) < 22.1$   
 $V_{\text{ripple}} < 150 \text{ mV/dynode}$   
 Voltage stabilization 0.95% on 38% input variation  
 Supply voltage  $2V5 < 3V3 < 4V0$   
 Power  $.6 - 1.4 \text{ mA}_{3V3}$  at  $800 - 1400 \text{ V} < 4.5 \text{ mW}$   
 $dV/dt < 75 \text{ mV}/\mu\text{s}$ , RFI -20 dB @ 150 kHz-10 MHz  
 cathode voltage -800 - -1400 V  
 Voltage divider (between D1 – D10 and A for Photonis XP53B20)  
 K    DA    G    D1    D2    D3    D4    D5    D6    D7    D8    D9    D10    A  
 0.15    1    1.5    2    1    1    1    1    1    1    1    1    1  
 (total: 13.65)  
 PCB = 38 mmØ

Time resolution	2 ns
Two-hit time separation	25 ns
Threshold DAC	8 bits
HV DAC	8 bits
PROM (ID)	20 bits
Communication I <sup>2</sup> C	
Supply voltage	$3V0 < 3V3 < 3V6$
Power consumption	20 mW
Technology	350 nm CMOS
Silicon area	1.6 mm x 1.8 mm

Presentation given by Deepak Gajanana  
A Front End ASIC for the read out of the PMT  
in the KM3NeT Detector

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# Summary

**HV circuit,** designed for a 10 dynodes PMT after the requirements

- ✓ **Adjustable HV**  
cathode voltage -800 - -1400 V
- ✓ **Small footprint**  
PCB = 38 mmØ
- ✓ **Low power**  
Vinput 3.3V  
0.6 - 1.4 mA<sub>3V3</sub> at 800 - 1200 V < 4.5 mW  
(commercial available 50 mW)
- ✓ **Low ripple**  
706 mV<sub>1056</sub>    8.5 < T(°C) < 22.1  
0.07%            8.5 < T(°C) < 22.1  
Vripple < 150 mV/dynode
- ✓ **Low RFI**  
RFI -20 dB @ 150 kHz-10 MHz

**Thank you**

## Amplifier

With a prototype of the dedicated amplifier 80 fC was successfully detected. (PMT gain  $0.5 \cdot 10^6$ )  
No influence of the switching cycle of the HV converter was seen.