Upgrade of the ALICE-TPC read-out electronics

Antoine Junique, Luciano Musa, Magnus Mager, Attiq Ur Rehman
for the ALICE collaboration

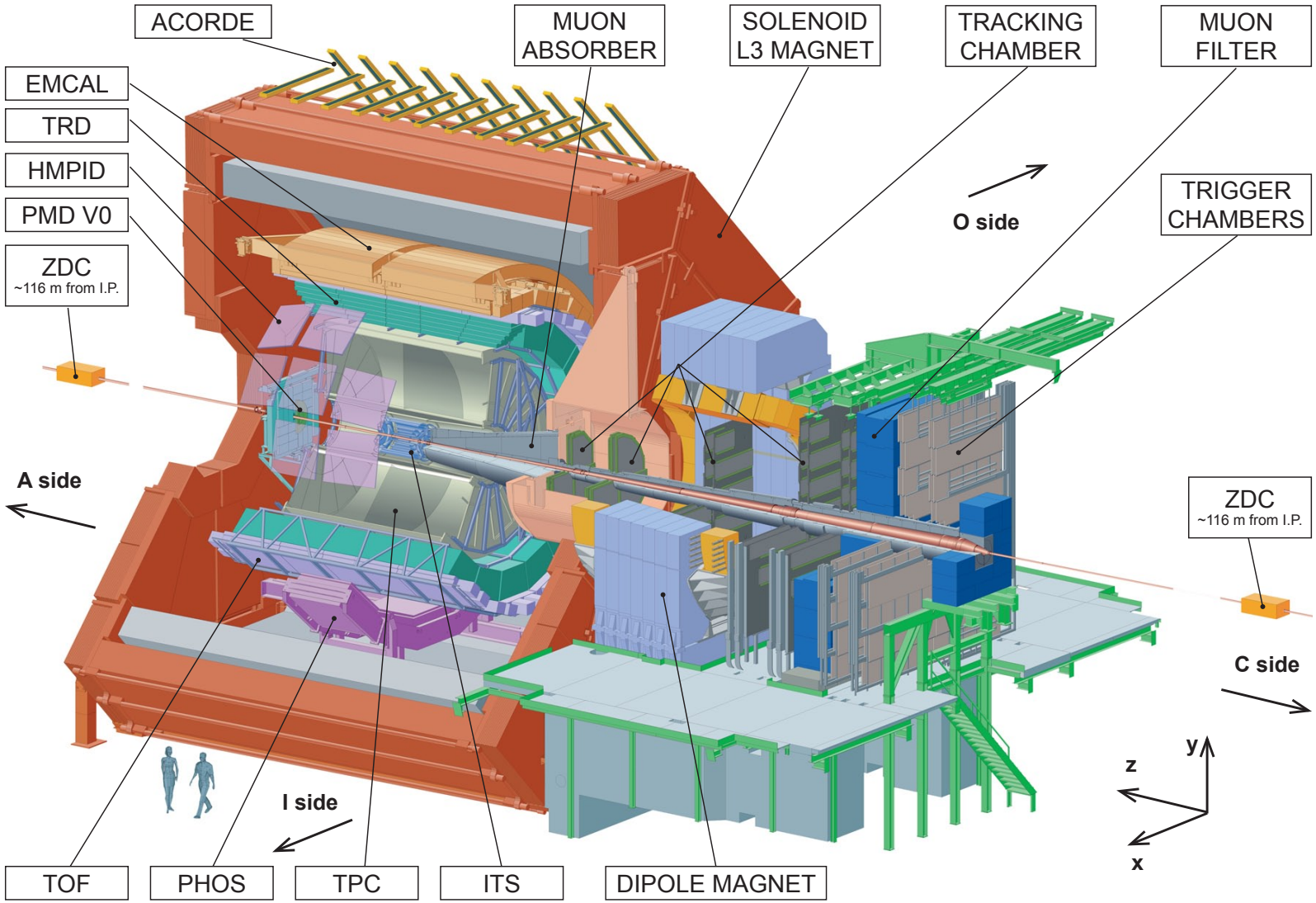
CERN

TWEPP Aachen
September 21st, 2010

Outline

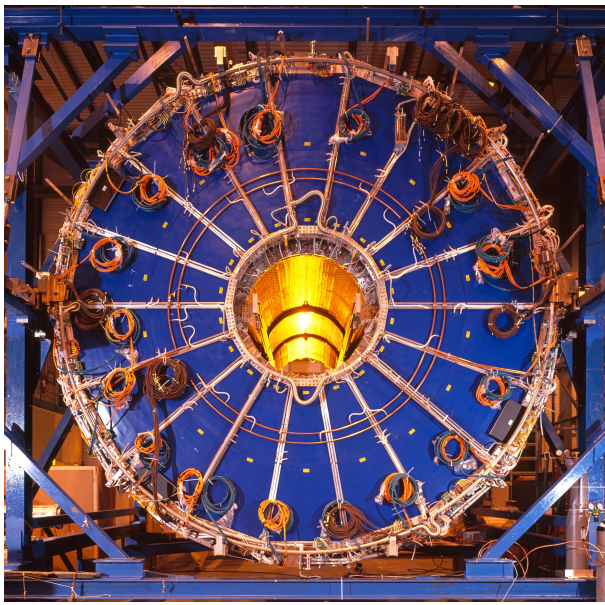
- Overview of ALICE and its TPC
- Current read-out and performance
- Proposed upgrade & first prototype
- Planning

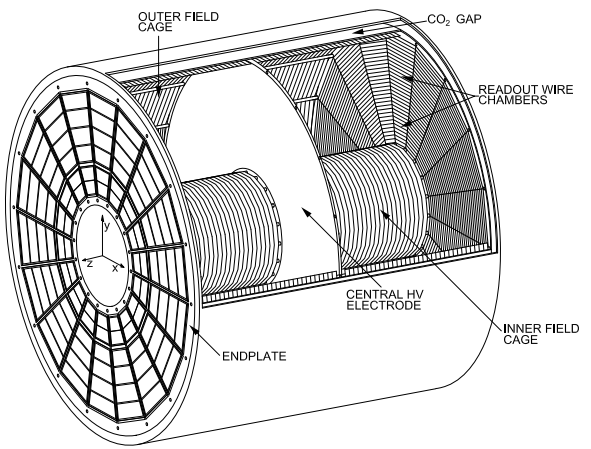
ALICE


ACORDE
MUON ABSORBER
SOLENOID L3 MAGNET
TRACKING CHAMBER
MUON FILTER
EMCAL
TRD
HMPID
PMD V0
ZDC ~116 m from I.P.
O side
TRIGGER CHAMBERS
A side
ZDC ~116 m from I.P.
C side
I side
y
z
x
TOF
PHOS
TPC
ITS
DIPOLE MAGNET

The TPC – key facts

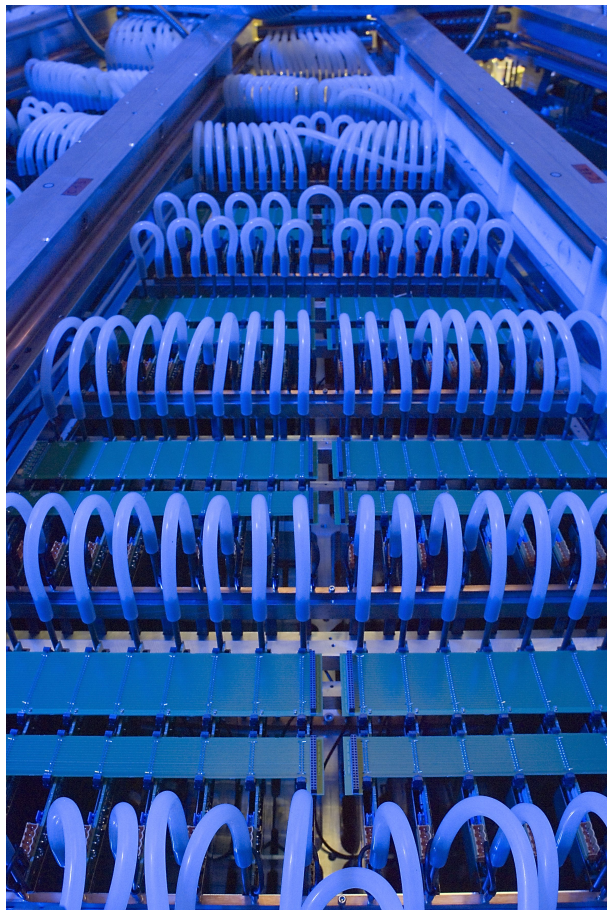
- pseudo-rapidity coverage: $|\eta| < 0.9$ or $|\eta| < 1.5$ for full and 1/3 of radial track length, respectively
- active volume: $-2497 < z < 2497$ mm times $848 < r < 2466$ mm
- read-out chambers: $2 \times 2 \times 18$ (side, radial and azimuthal segmentation) multi-wire proportional chambers
- gas: Ne–CO_2–N_2 [85.7–9.5–4.8]
- drift-time: 96 μs (nominal)





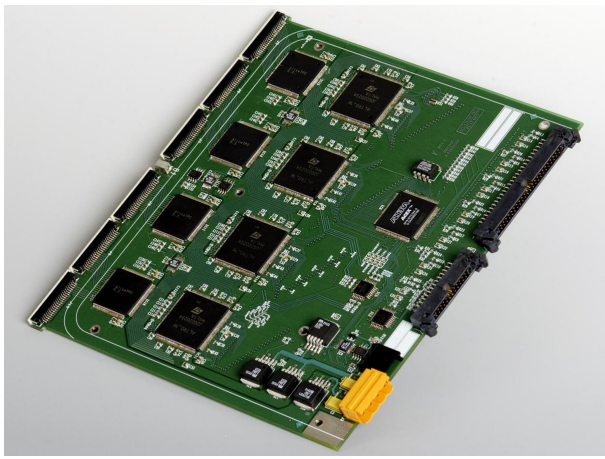
Electronics

- number of pads: 557,568; distributed over:
  - 4,536 front-end cards (FECs)
  - 216 independent read-out partitions:
    - 2 sides times
    - 18 sectors (azimuthal) times
    - 6 partitions (radial) times
    - 18, 25, 18, 20, 20, 20 FECs (inner to outer)
- full parallel/concurrent operation
- sampling:
  - 10 bit at 10 MSPS
  - up to 1,008 samples
- multiple event buffering: 4 events
- (very) raw event size: 700 MByte



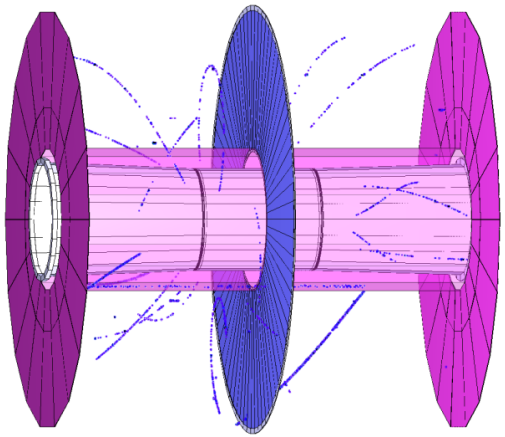
The front-end card (FEC)

- 128 channels
- components:
  - 8 PASAs (pre-amplifier and shaper)
  - 8 ALTROs (ADC, DSP and event buffering)
  - board controller (BC)
- interface:
  - $40 + 5$ bit (data + control) wide bus (GTL)
  - triggers
    - L1 (GTL)
    - L2 (GTL)
  - clocks
    - read-out (GTL)
    - sampling (PECL)
  - 4-wire serial I^2C-like slow control bus (GTL)
  - card-switch line (CMOS)

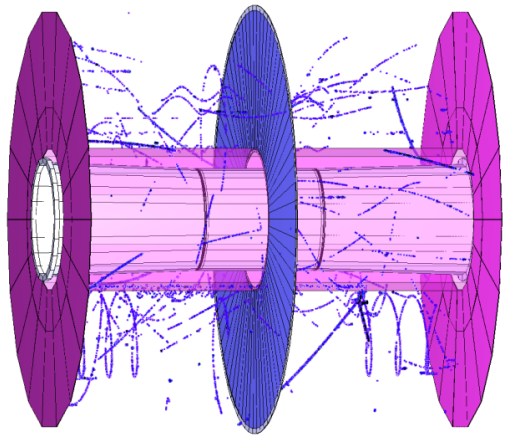


Foreseen operating scenarios

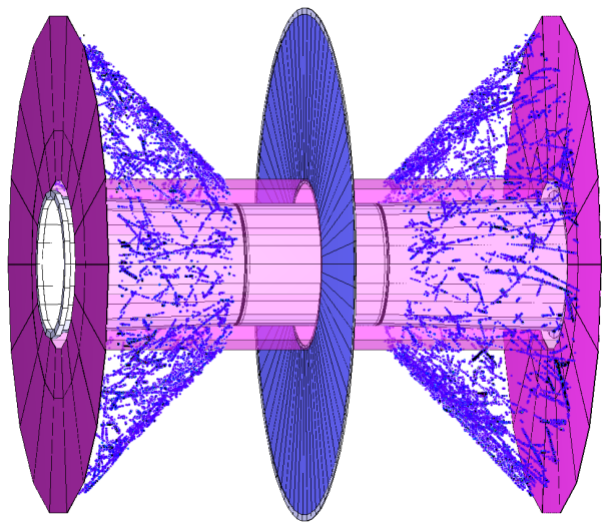
- proton-proton
  - isolated events
    - low interaction rate
    - past-future protected
  - pileup (up to 100 events)
    - within a bunch
    - within the drift time
- heavy ions
  - isolated events
  - multiplicity trigger



1 *pp* event



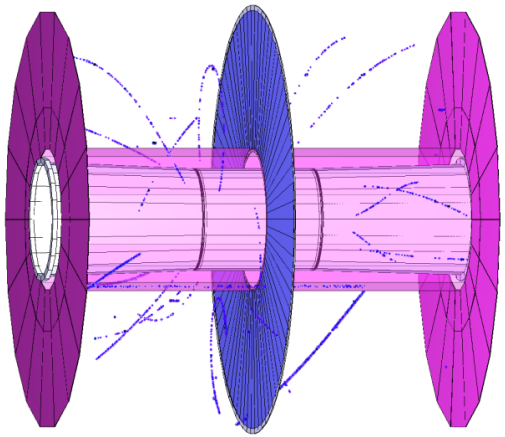
3 *pp* events (pileup)



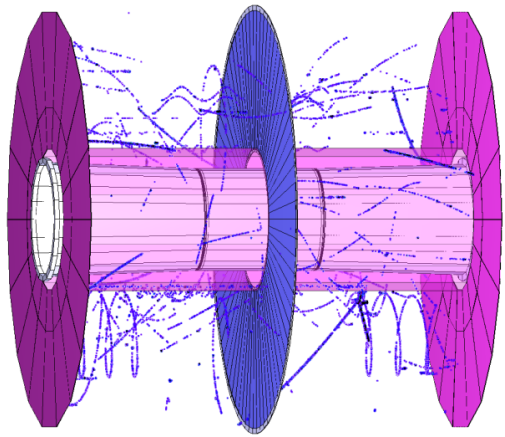
1 *PbPb* event (θ-slice)

Foreseen operating scenarios – Simulations

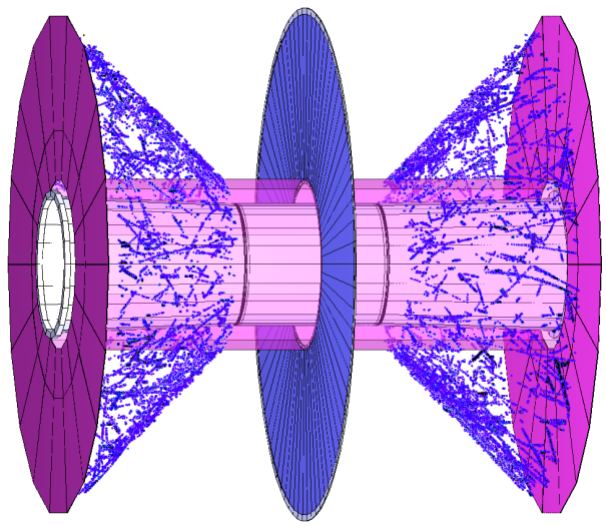
- simulations done by merging $\sqrt{s} = 7$ TeV min. bias *pp* events
- proton-proton pileup
  - overlay of displaced events
  - equally spaced from $T - 100$ to $T + 100$ μs.
- heavy ions
  - overlay of events without displacement
  - 100 for min. bias *PbPb*, and
  - 300 for central collisions



1 *pp* event



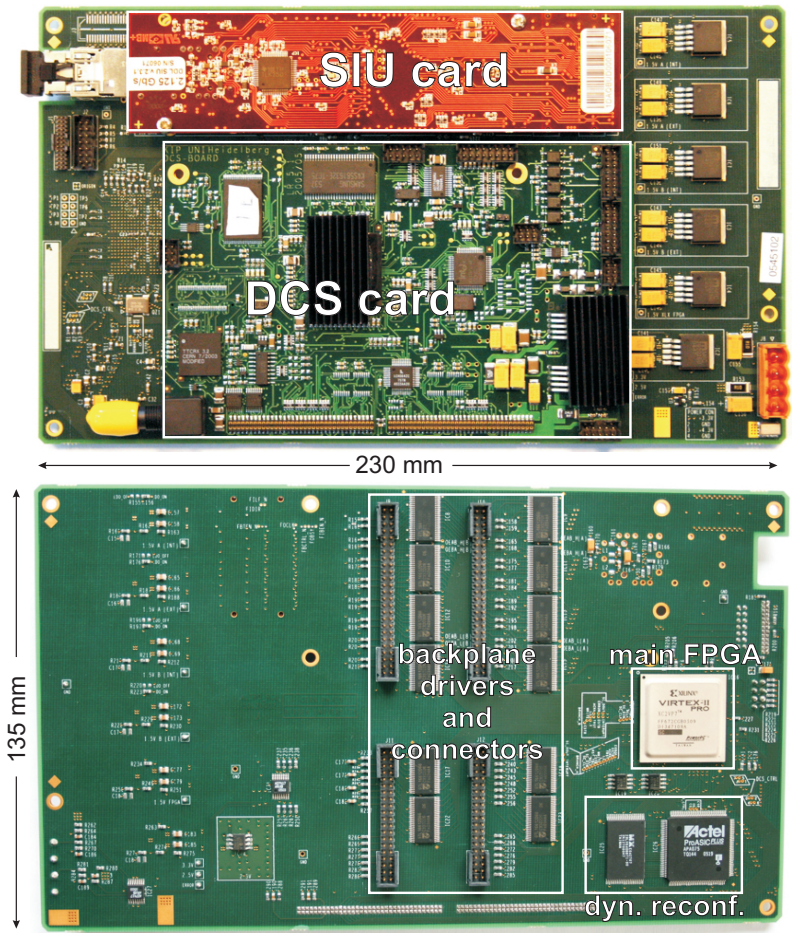
3 *pp* events (pileup)



1 *PbPb* event (θ-slice)

Read-out control unit (RCU)

- 216 RCUs, one per read-out partition
- 2 buses connect to half of the FECs each
- 2 daughter cards:
  - SIU card: optical link (DDL) interface to experiment-wide data acquisition
  - DCS card:
    - clock and trigger receiver
    - embedded Linux to monitor electronics
- 2 FPGAs:
  - Xilinx: communication to FECs and daughter cards
  - Actel: active partial reconfiguration to increase radiation tolerance



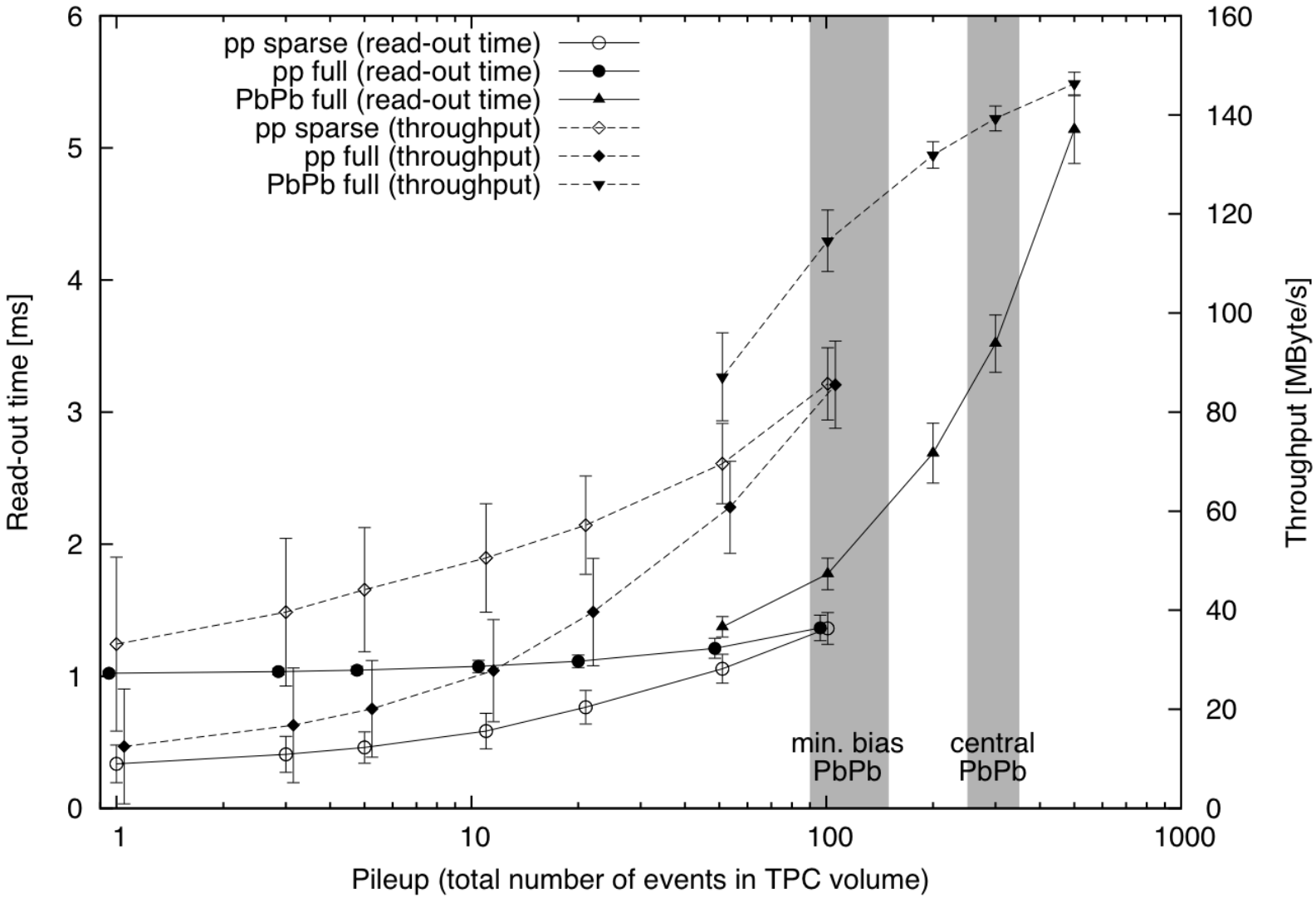
Read-out modes

- full read-out:
  - read out every channel ($T_{rdo,ch} \geq 450$ ns)
  - multiple event buffer usable
  - used for high occupancy events
- sparse read-out:
  - BCs compile lists of channels with data (parallel on all FECs) ($T_{sevl} = 90\ \mu$s)
  - BCs transfer list of active channels to RCU (total: $T_{revl} = 10\ \mu$s)
  - read-out of non-empty channels only
  - multiple event buffer not usable (FEC isolated during first point)
  - used for sparse events

Read-out times and throughput

- front-end electronics designed for *PbPb* events and rates of $100 - 300$ Hz.
- read-out times measured by overlaying different numbers of events events in
  - in *pp* pileup topology (sparse and full read-out)
  - in *PbPb* topology (only full read-out)
- read-out time: maximum read-out time of all 216 links: $\max\{T_{rdo}\}$
- throughput: maximum link-size divided by maximum read-out time of all 216 links each: $\max\{S_{DDL}\}/\max\{T_{rdo}\}$

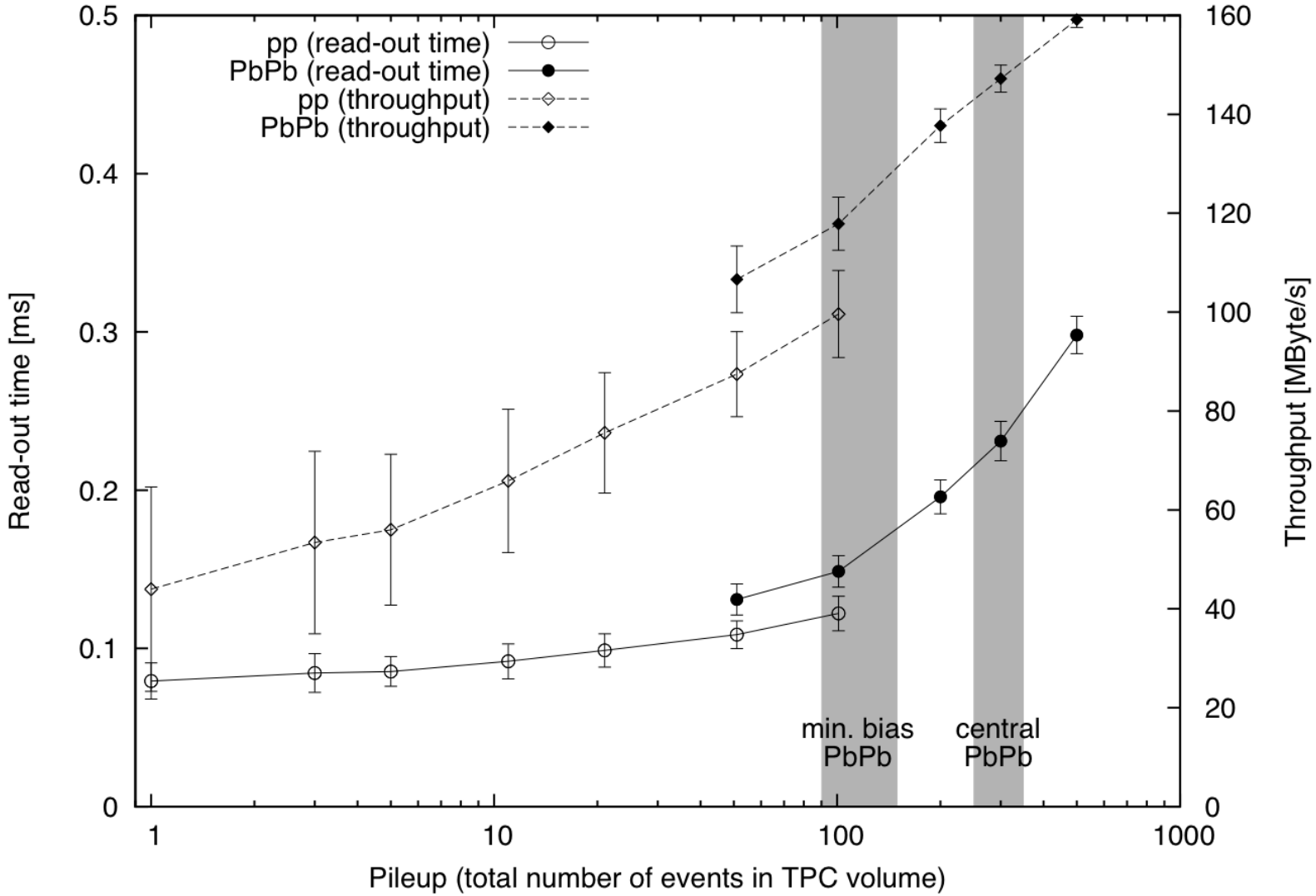
Read-out times and throughput – measurements



Motivations to upgrade

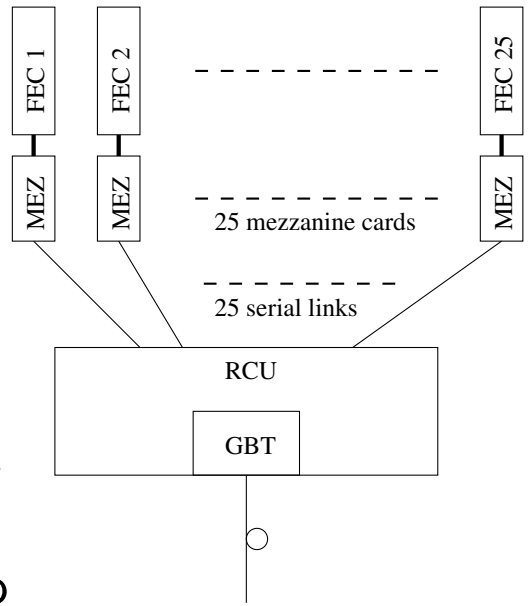
- physics:
  - lower expectation for $\mathrm{d}N/\mathrm{d}\eta$ for central *PbPb* collisions: 2,500 instead of 8,000 (TDR)
  - stable operation of other similar devices observed at high rates
  - event selection by HLT
- electronics:
  - reduce impact of ALTRO protocol overhead
  - make better use of available (future) bandwidth
  - resolve full VS. sparse read-out issue
  - increase fault tolerance

Motivations to upgrade II: FEC performance



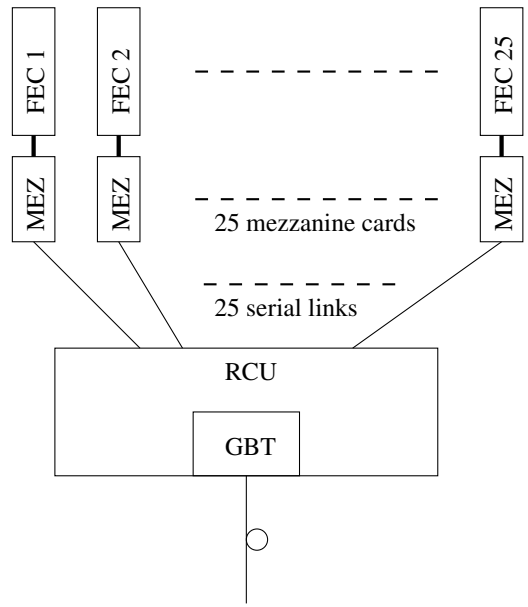
Proposed architecture

- restrictions:
  - keep FECs (worth 80% of whole TPC)
- topology:
  - replace bus by star
  - use serial links
- parts:
  - "FECint" (4,536): interface card to translate FEC bus to serial
  - "master RCU" (about 216): star-point and link to central services (Trigger, DAQ, DCS)



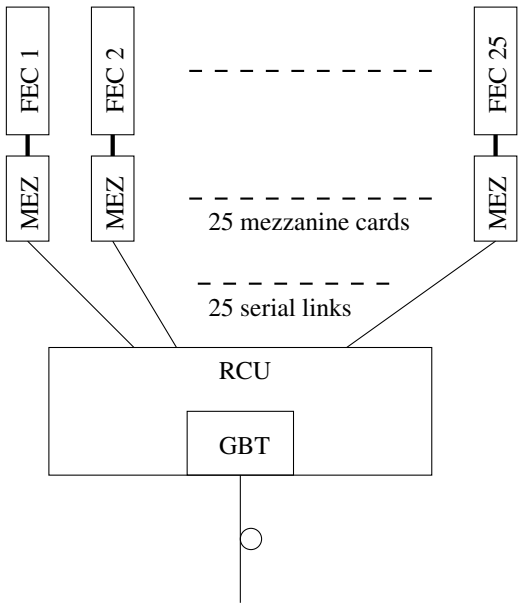
FECint

- translates parallel bus to serial bus
- adds memory to further derandomise events
- parallel interface to FEC:
  - clocks (sampling and read-out)
  - triggers
  - data
  - slow control
- serial link to master RCU:
  - 4 differential lines:
    - receive (2 GBit/s)
    - transmit (2 GBit/s)
    - *clock*
    - *trigger*
  - I^2C
- targets Xilinx Spartan-6 (cheap FPGA with high speed serial links)



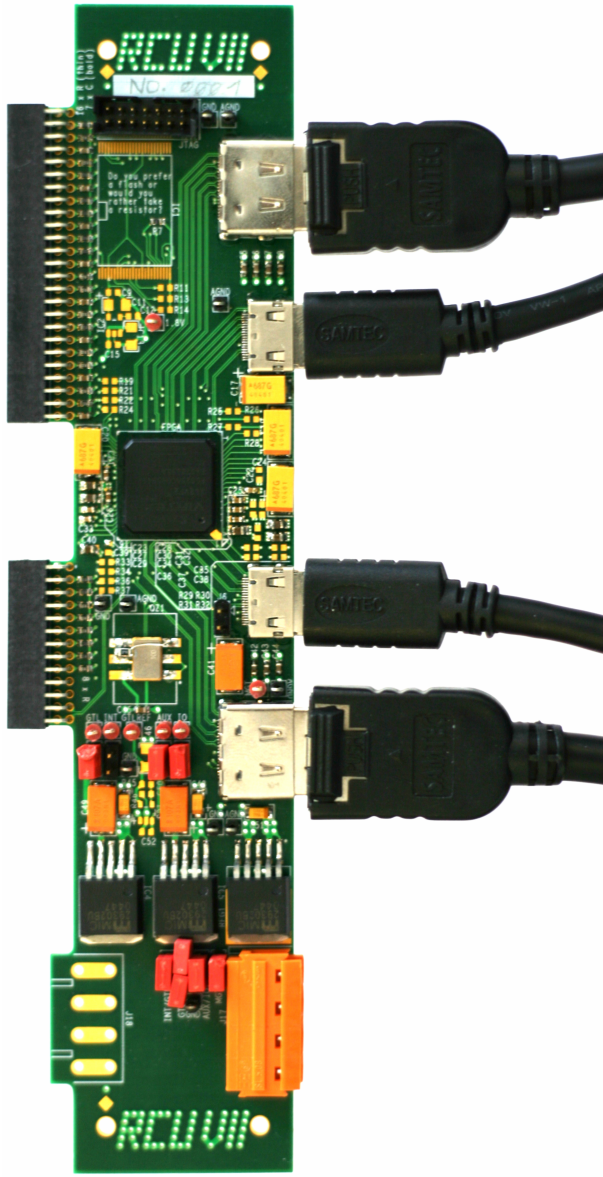
Master RCU

- star-point in data flow
- serial connection to about 20 FECs
- interface to central services, by (depending on DAQ upgrade) either:
  - integration of DDL and DCS, or
  - integration of new high level link
- integration into a single FPGA
- targets Xilinx Virtex-6



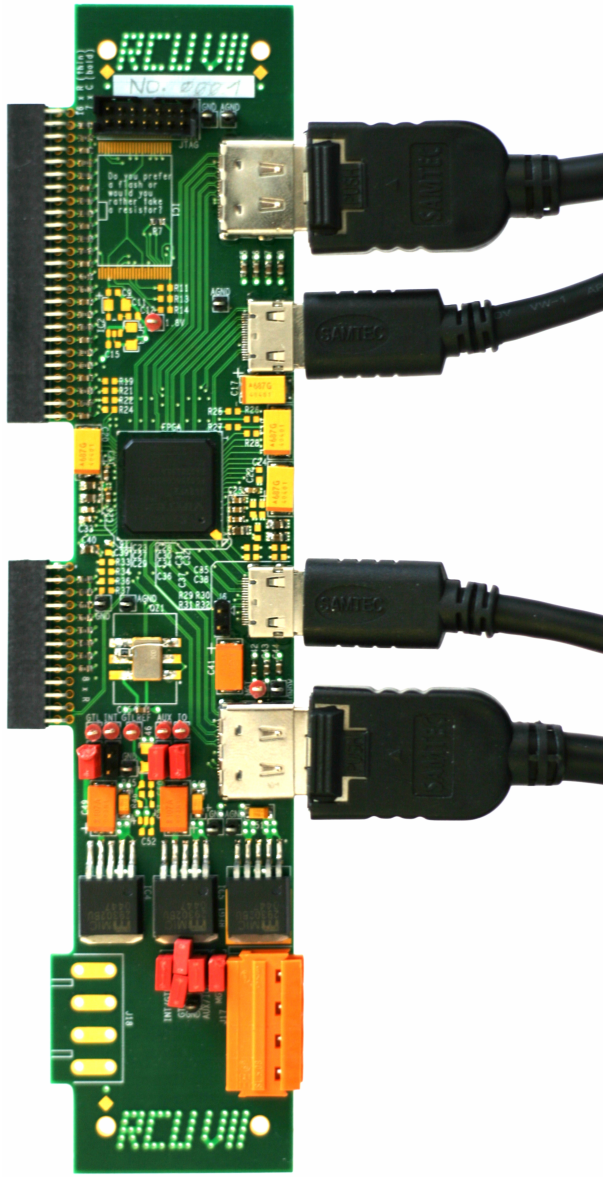
FECint prototype – design

- based on Virtex-II Pro (availability)
- aims:
  - mechanics:
    - minimum size
    - FEC connectors
    - choice of serial connectors
    - weight
  - electronics:
    - GTL–CMOS interfacing
    - signal integrity
  - price



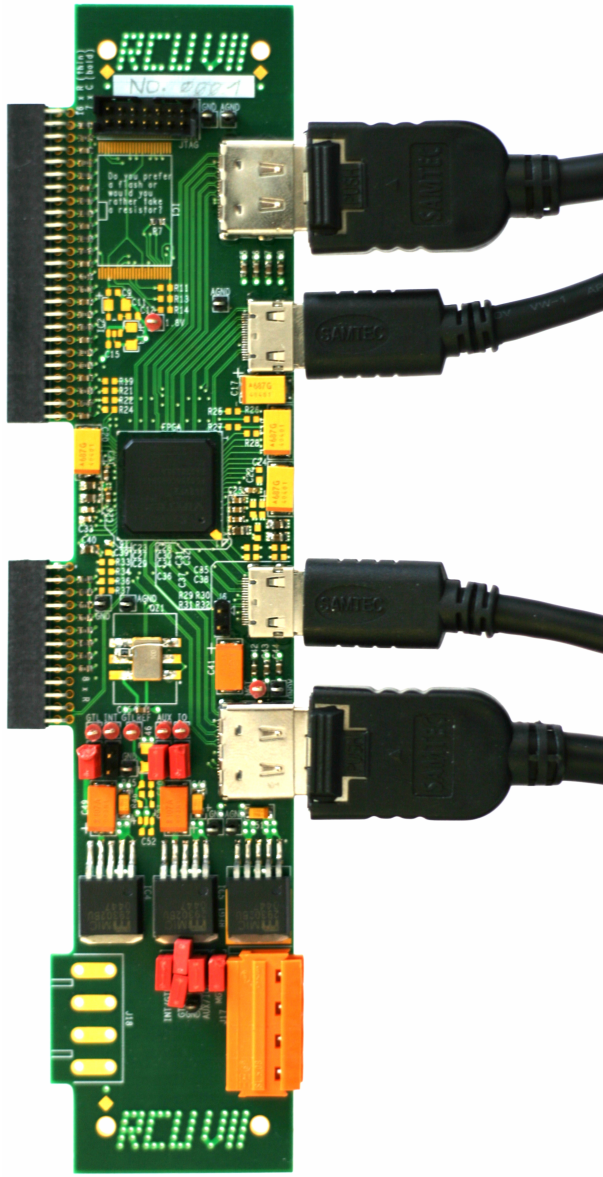
FECint prototype – hardware

- PCB:
  - dimensions: 18.4×4 cm
  - layers: 8 (to have enough power planes to assess decoupling)
- connectivity:
  - 4 serial ports:
    - 2 HDMI
    - 2 mHDMI
    - 2 rx-tx swapped
  - JTAG (programming and communication)
- testability features:
  - currents
  - voltages
  - FPGA temperature



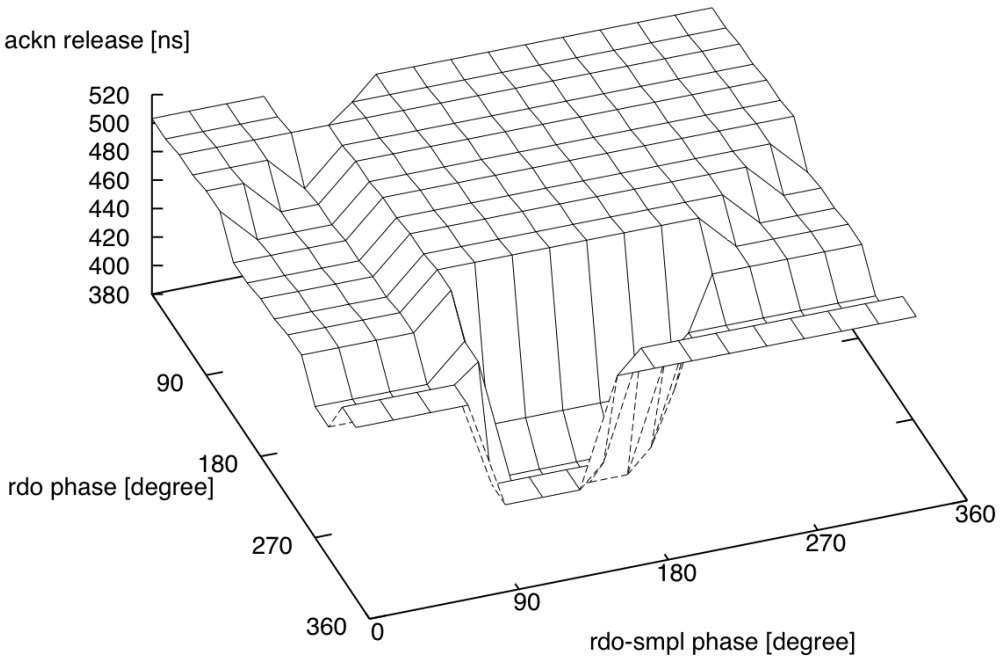
FECint prototype – firmware

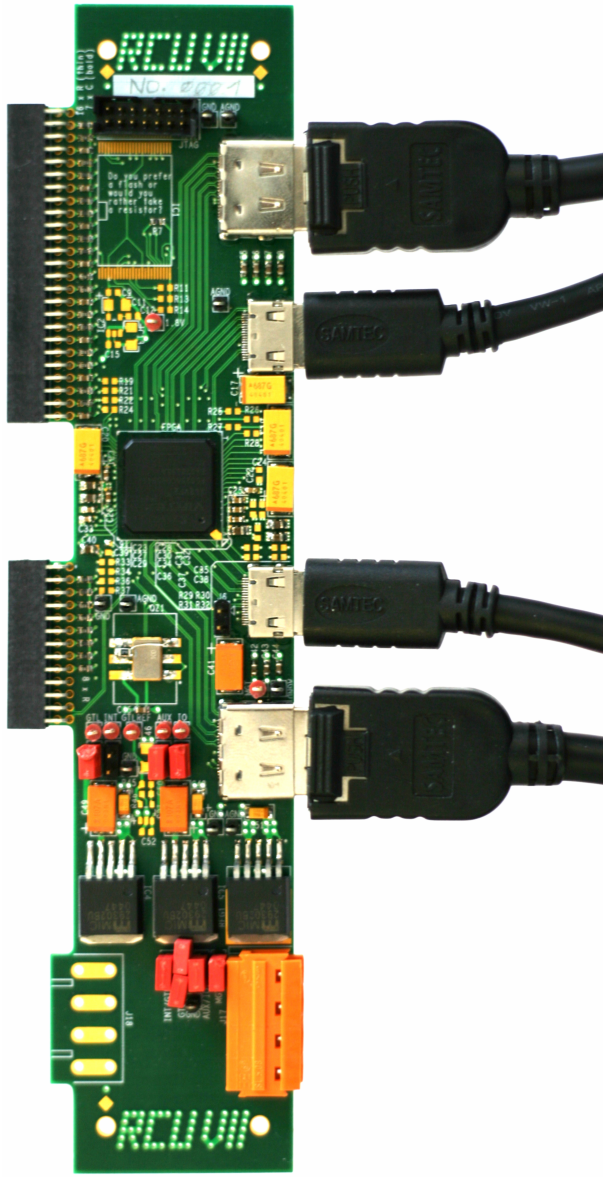
- FEC link:
  - software controlled DCMs for phase shifts of read-out and sampling clocks
  - in system ALTRO bus state analyser
  - detailed phase scans and characterisation of transactions
- serial link:
  - simple data packet transmitter and receiver
  - power consumption and temperature monitoring



FECint prototype – results

- approach is feasible
- minor issues:
  - FEC-connectors: needs adjustment in height
  - PCB size need to be adjusted for cooling hoses
- improvement of ALTRO communication possible (due to direct connection):





Near future

- second iteration of the FECint:
  - Spartan-6
  - adjusted geometry (size and connectors)
  - cost-optimised routing
  - USB/SFP connectivity
- implementation of “master RCU”:
  - as counter part for the front-end link
  - including modules to interface Trigger and DAQ
- re-assessment with real PbPb data

Farer future

- 2012: qualification of components
- 2013: engineering of large scale prototype
- 2014–2015: production & testing
- 2016: installation (long LHC shutdown)