FOM

The Design for Test Architecture in Digital Section of the ATLAS FE-I4 Chip

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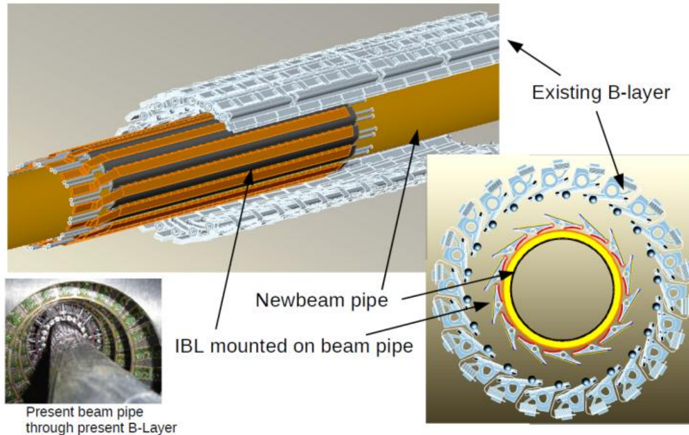
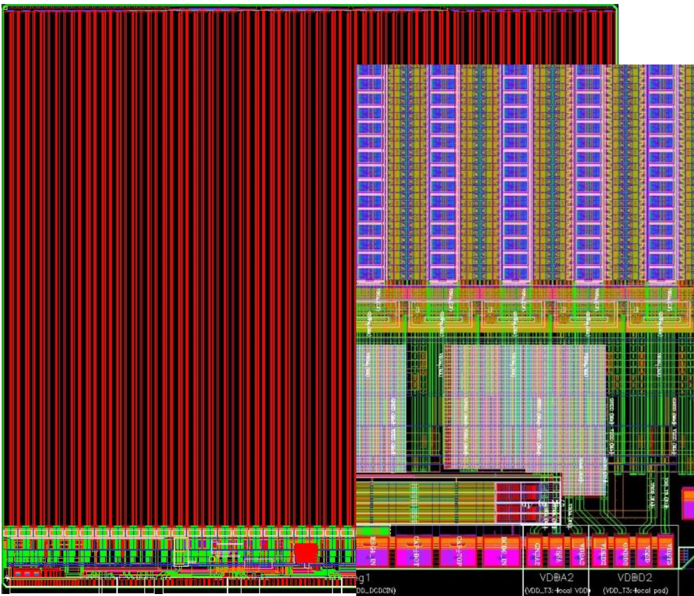
Outline

- Introduction
- Implementation of the Design-for-Test (DfT) Architecture in FE-I4
- Test Development Flow
- Method evaluation - benchmarking
- Conclusion and further challenges

FE-I4 Chip

Insertable B-Layer (IBL) Application

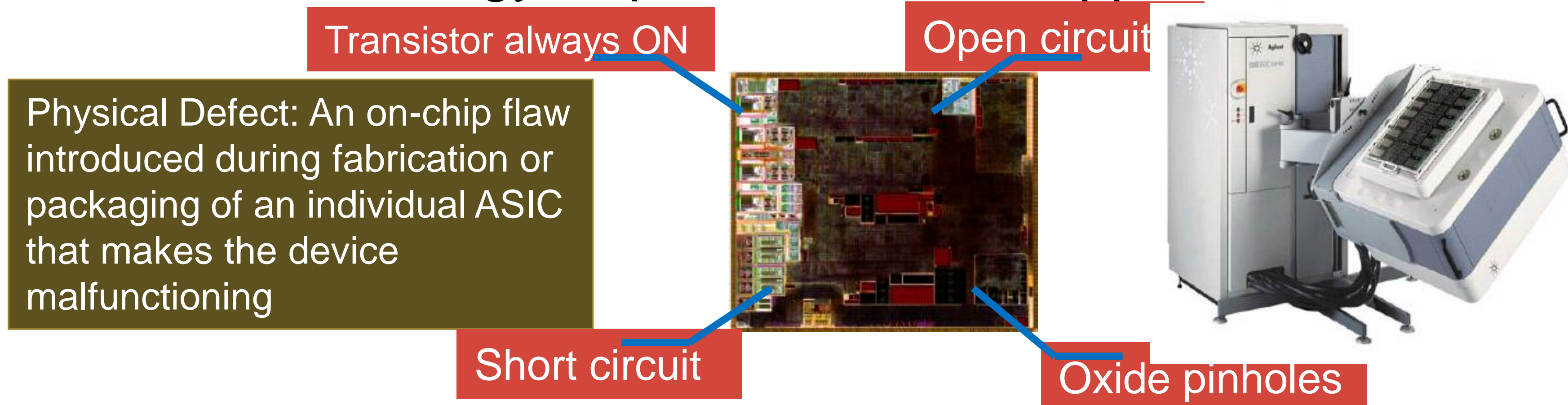




Pixel array size	80x336
Pixel size	50x250 mm^2
Maximum charge	100 000 e^-
Hit trigger association resolution	25 ns
Same pixel two-hit discrimination (time)	400 ns
Tuned threshold dispersion	< 100 e^-
Charge resolution	4 bits
ADC method	TOT
Radiation tolerance	250 MRad
Operating temperature range	-40° C to 60° C
Average hit rate with < 1% data loss	400 MHz/cm^2
Readout initiation	Trigger command
Max number of consecutive triggers	16
Trigger latency (max)	6.4 μs
Maximum sustained trigger rate	200 KHz
External clock input (nominal)	40 MHz
Single serial command input (nominal)	40 Mb/s
Single serial data output (nominal)	160 Mb/s
Output data encoding	8b/10b
I/O signals	LVDS

Importance of IC Test

- IBL has raised concerns on large-volume product quality: yield has to be increased
- Complexity of State-of-the-Art ICs produced in deep submicron technology requires dedicated approach for test



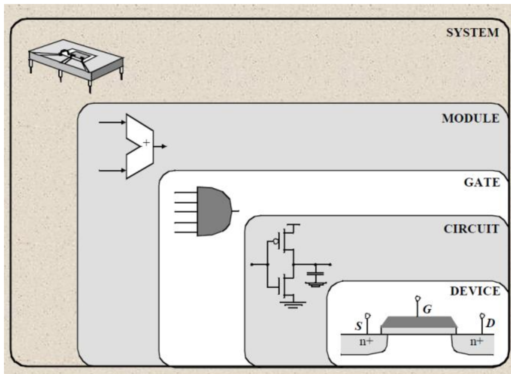
- Times when the designers were able to write the procedures to distinguish between correct and faulty chips quickly, with ease and map them to tester platforms, are past long times ago

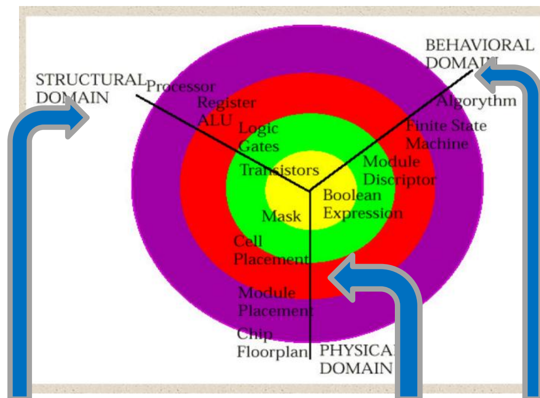
Test development process in deep-submicron technologies

Internal probing of ICs too costly

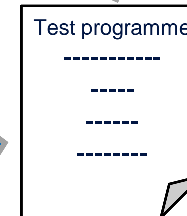
Rule of the game: Tester access to the Device Under Test (DUT) only possible through its primary I/O ports – the Design for Test (DfT) needed

Fact: Test is not any longer back-end process – the development and implementation begins during the design stage



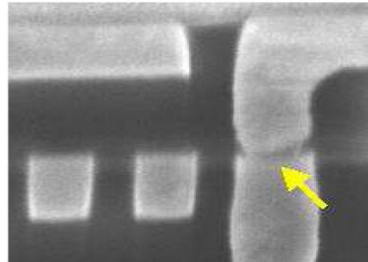
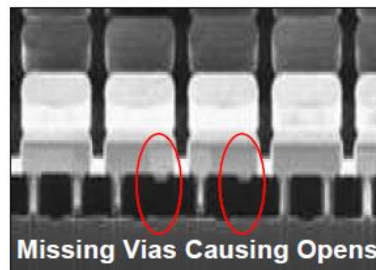


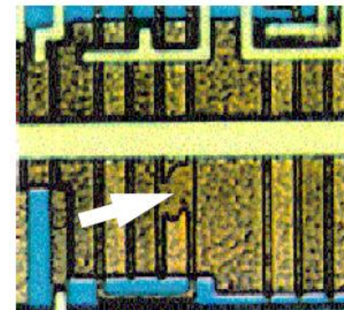
Test Development and Test Vector Generation



Functional vs Structural Testing

- Functional testing verifies that a circuit fulfils the desired spec
- Functional testing not feasible for exhaustive tests
  - An example: 32-bit adder requires $2^{65} \approx 3.7 \times 10^{19}$ test vectors
- Structural test focuses rather on the circuit structure and can cover manufacturing defects that otherwise may not have been detected by functional testing
  - Power or ground shorts
  - Open interconnection on the die
  - Short-circuited drain or source of the transistor, caused by metal-spike through



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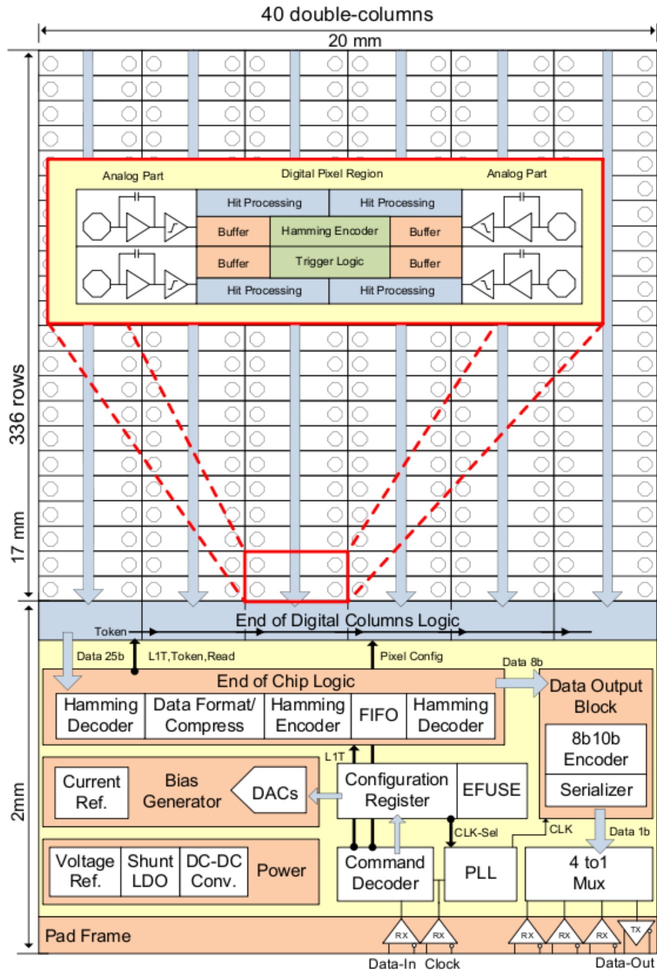
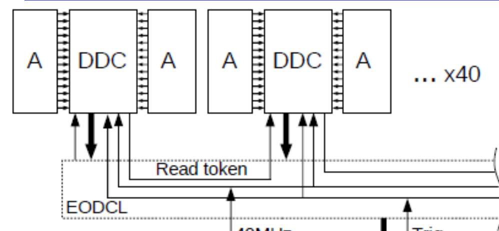
FE-I4 Architecture Overview

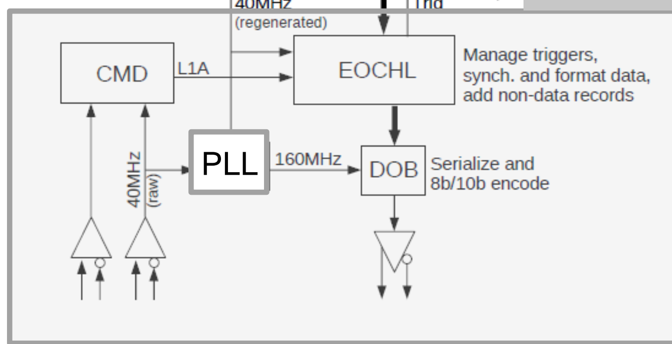


Courtesy of M. Barbero*

For the sake of SEU robustness, the design makes extensive use of triple redundancy, emphasizing further the internal test structures requirement



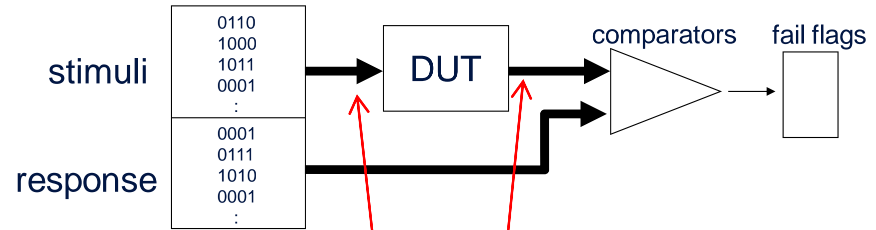
The Design for Test Circuitries are inserted in the output data path of the readout part of the FE-I4



The DfT architectural choice: Full-scan Modular (Core-Based) test architecture

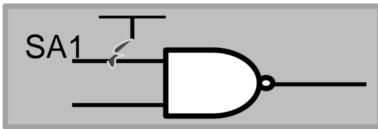
Basics of digital structural testing

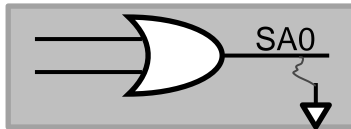
- Stimulus and response calculated by Automatic Test Pattern Generator (ATPG) based on fault models
- Applied on the whole device or in a divide-and-conquer fashion, individually on the embedded modules (cores)



Access to internal terminals of the embedded modules (cores) through design for test (DfT) is necessary

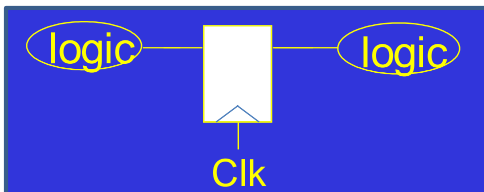
Stuck-at Fault Model: A logical model representing the effects of a physical defect

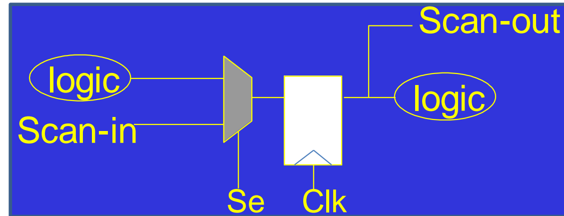




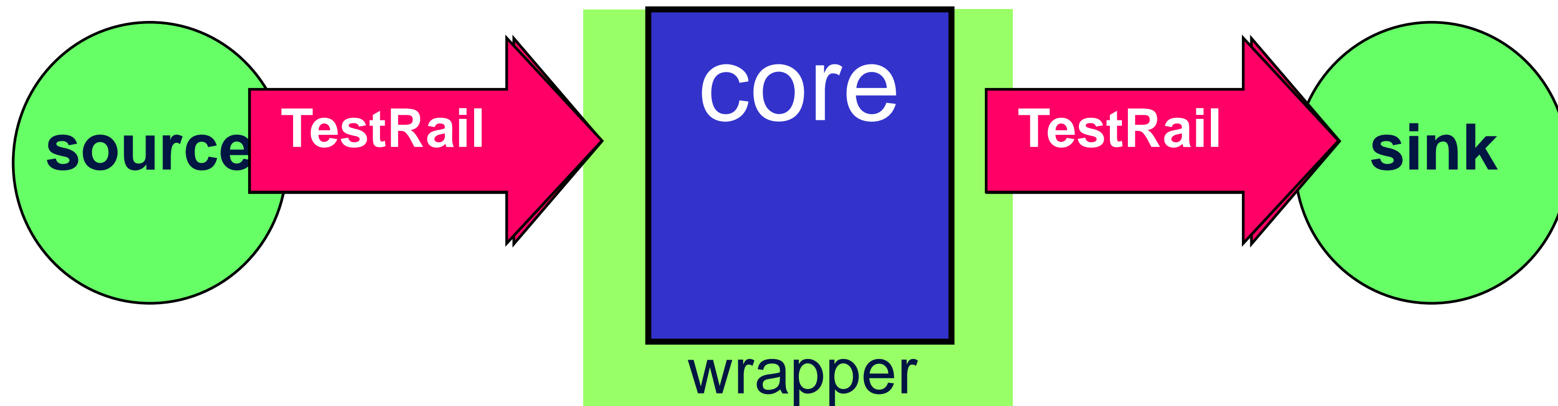
Most of the commercials Automatic Test Pattern Generator (ATPG) based on stuck-at fault model (D-algorithm)

Handling sequential designs: full-scan concept





Core-Based Test concept



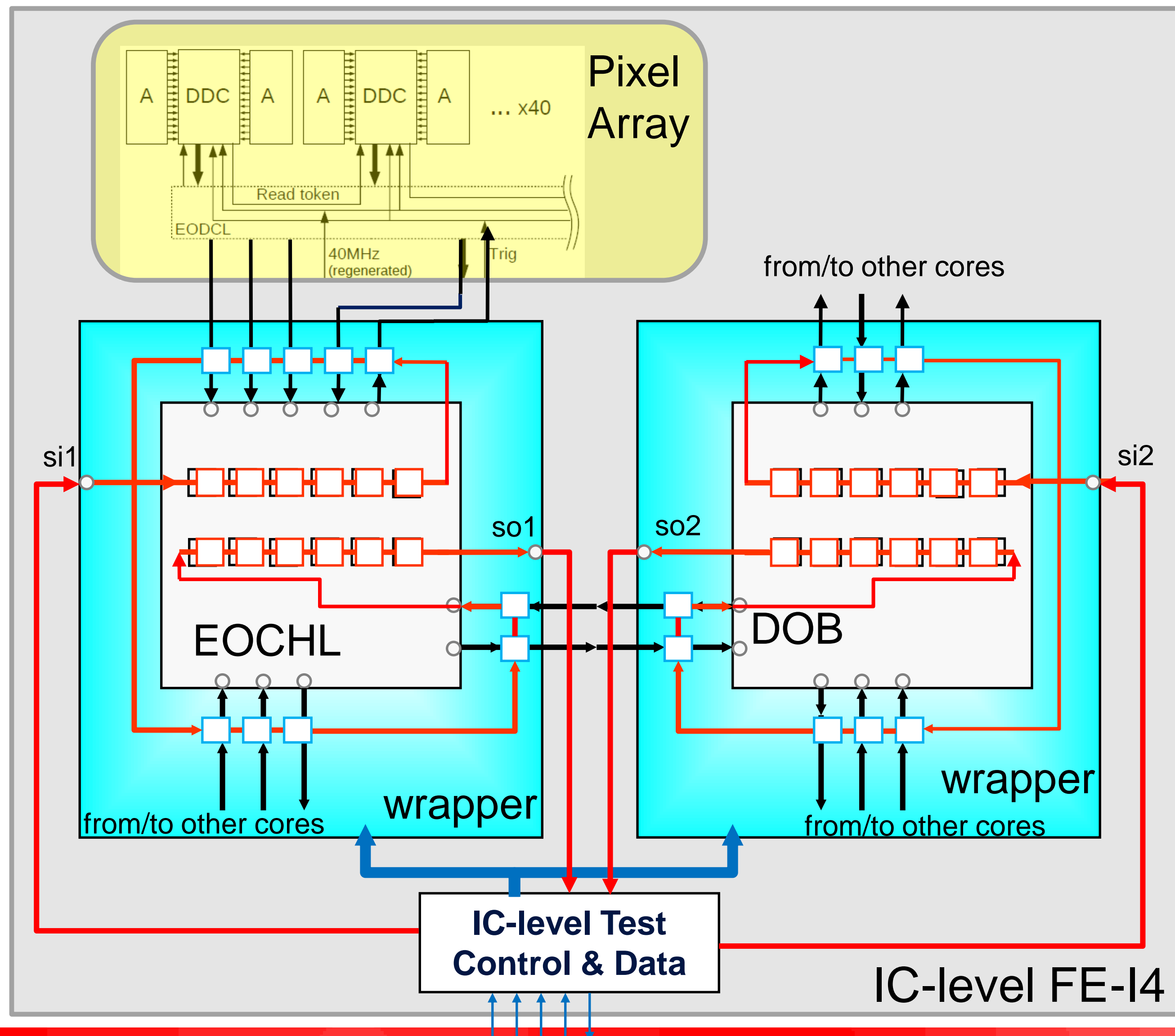
1. **Test Pattern Source and Sink**
2. **Test Access Mechanism (TAM)**
3. **Core Test Wrapper**

[Zorian, Marinissen, Dey - ITC'98]

Core-Based Test in FE-I4

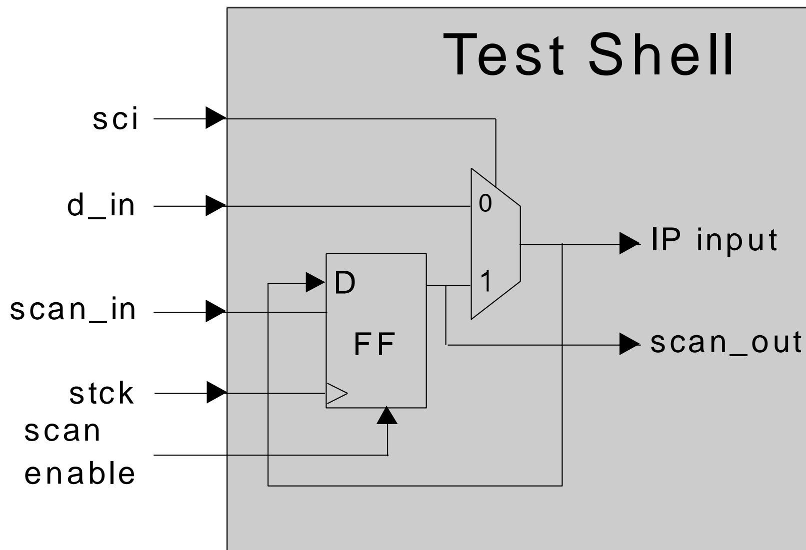
Mandatory

- Internal scan chain insertion
- Wrapper cells providing function access and test controllability + observability at IP's data terminals
- TestRail access to wrapper cells ('surround chains') and IP flip flops ('scan chains')
- SEU proof

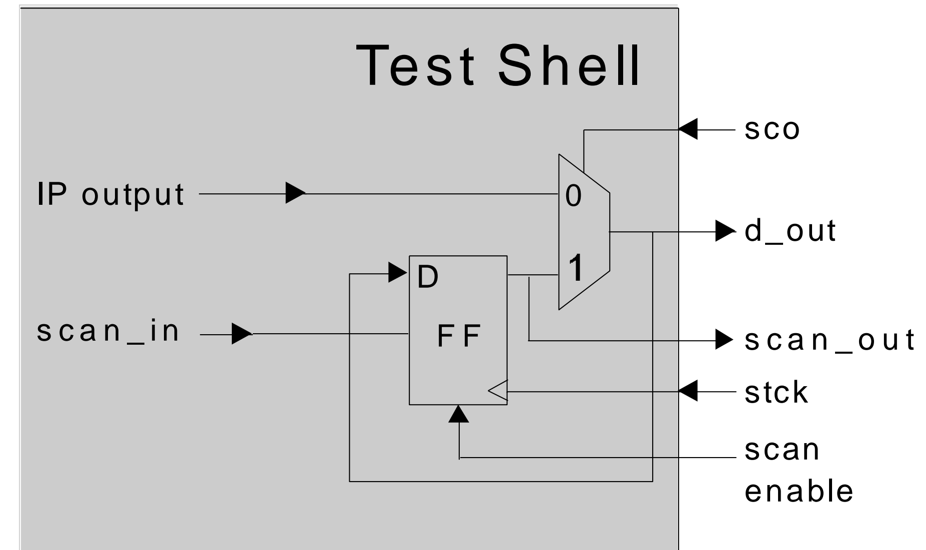


Wrapper cells in the nutshell

Input isolation

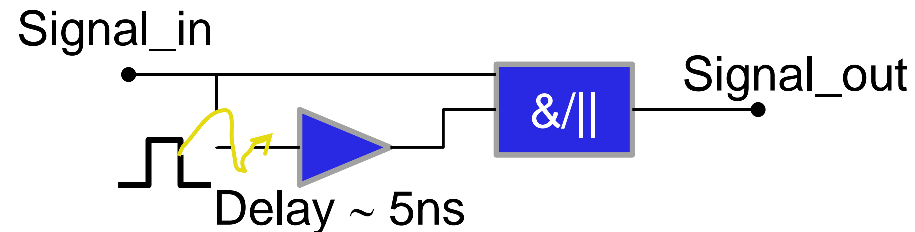


Output isolation



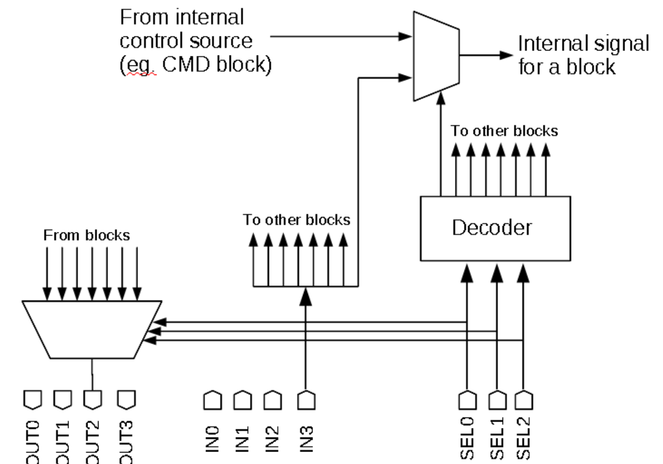
Note: Only the combinatorial inputs require isolation

Deglitcher cells implemented on scan enable, test mode and reset signals



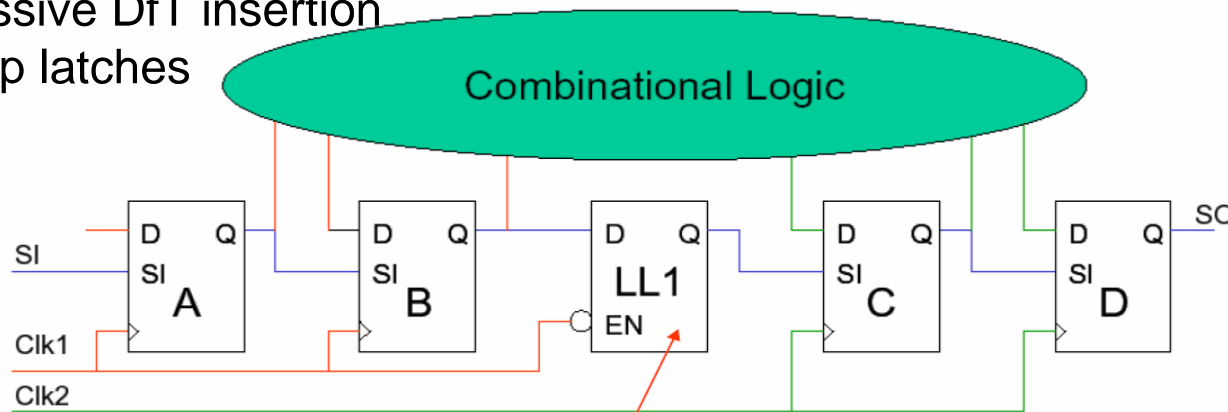
IC-level control and consequences on core internal DfT

- Cores will be scan-tested independently, i.e. in isolation of each other
- Top-level test control (scan enable, test mode selection) routed to each of the cores
- No more than one scan chain per core



Courtesy of M. Garcia-Sciveres *

Additional challenge for multiple-clock cores: most aggressive DfT insertion strategy with lockup latches



Lockup latch inserted on the clock domain boundary

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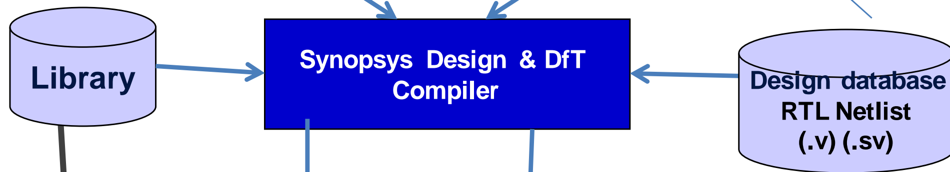
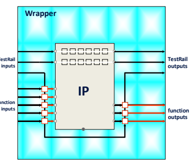
DfT generation: Two-pass mapped flow

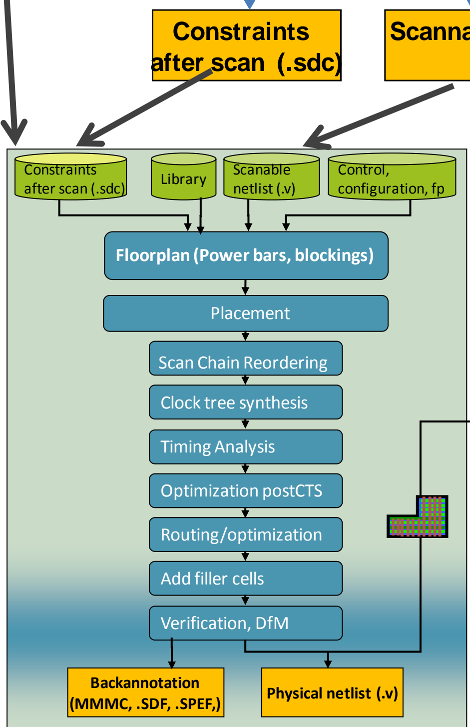
scx3_cmos8rf_lpvt_ff_1p32v_m55c.db scx3_cmos8rf_rvt_tt_1p2v_25c.db
scx3_cmos8rf_rvt_ss_1p08v_70c.db

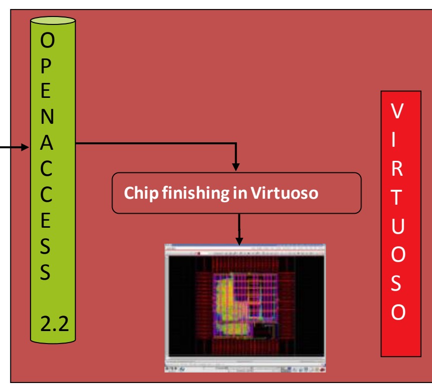


Input, output delay =5ns,
Clock(s) timing and uncertainty (500p)
False path on reset, scan,
wire_load_model,



Synthesis & DfT



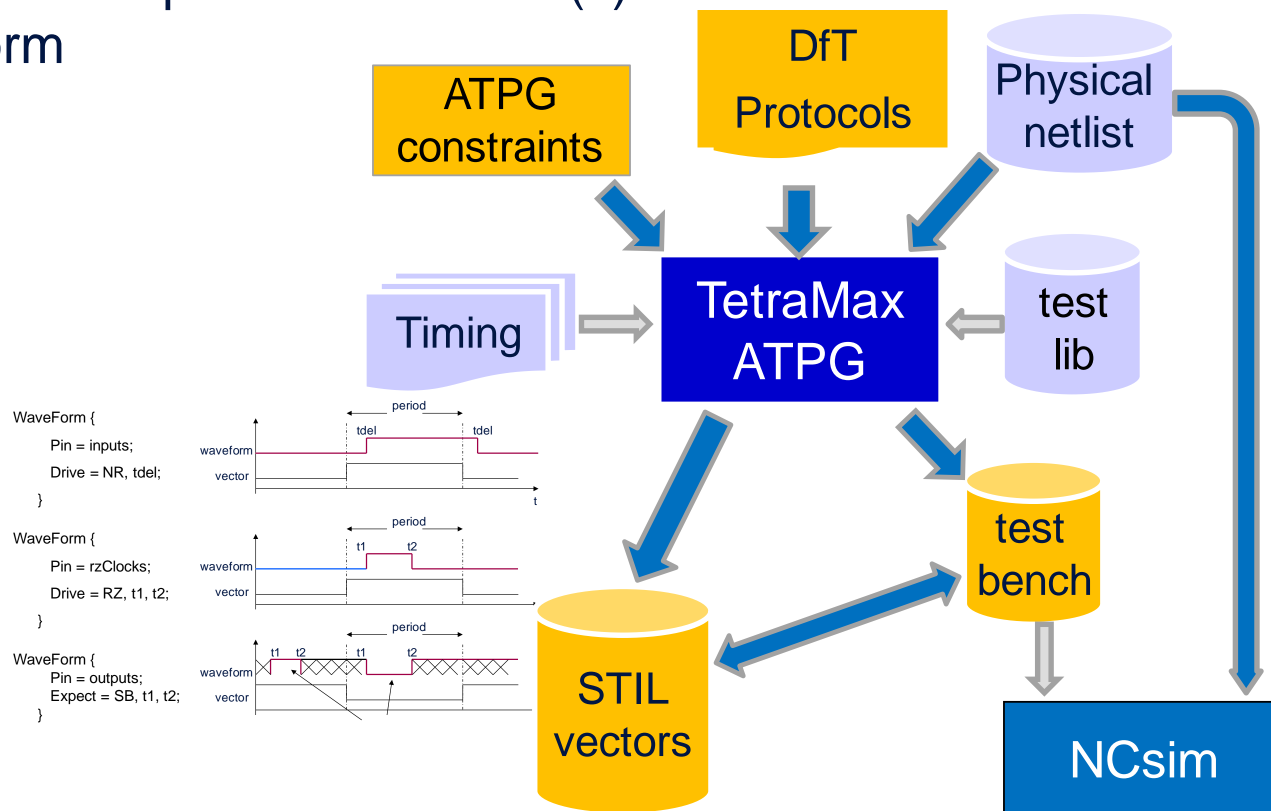


Physical Implementation

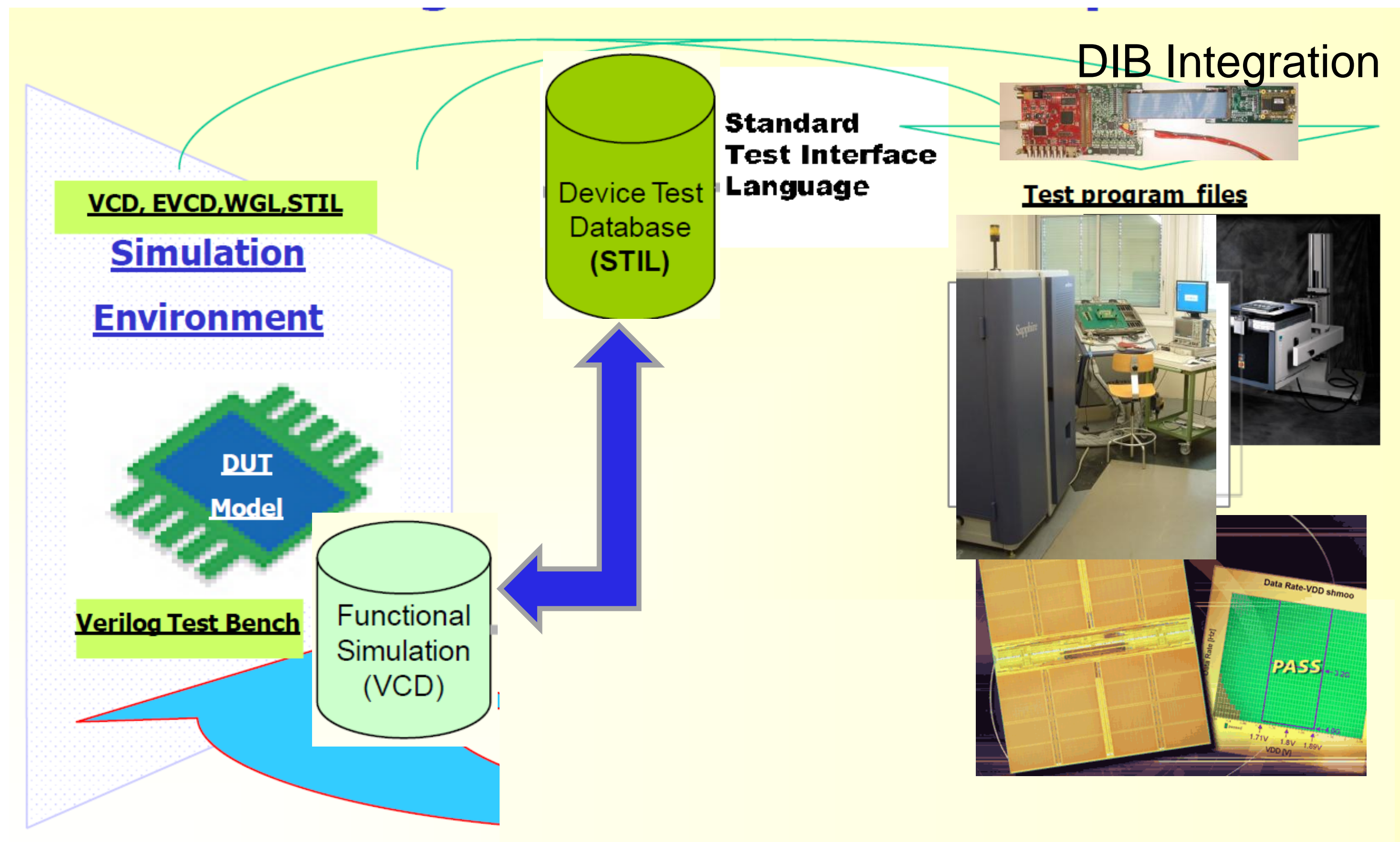
Courtesy of MUG *

ATPG & Test Assembly

- Generate the test patterns
- Generate the test bench for the simulation with both stimuli and response with timing and wave information
- Assemble the test patterns of the IP(s) into the test vectors running at the tester platform



Test execution



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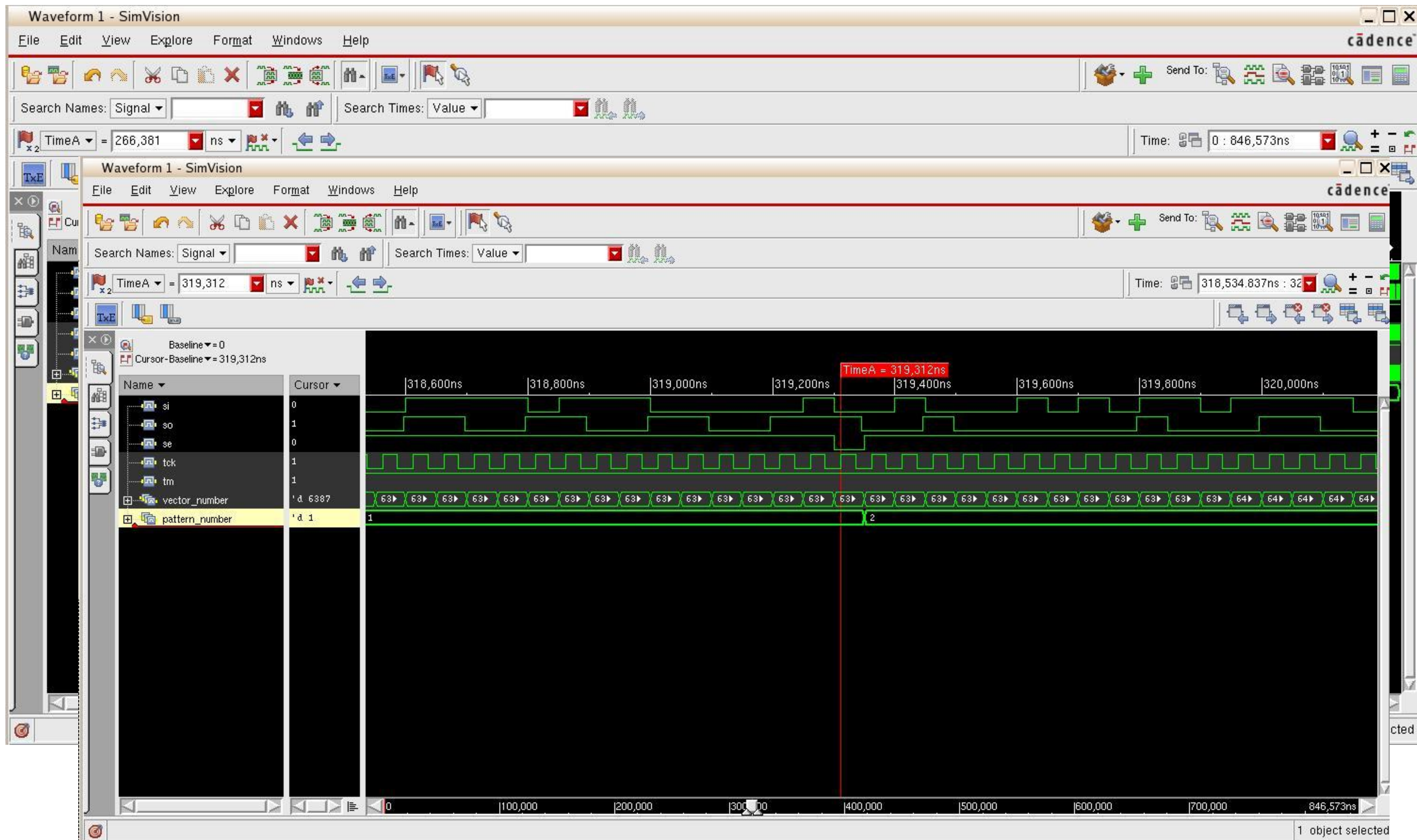
Reports

- End of Chip Logic (EOCHL) Core
  - Total faults 105980
  - Fault coverage 90.83%
  - Number of patterns 231 (3192 bit-stream wide, each)
  - DfT area overhead ~ 8 % relative, < 0.1% absolute
- Data Output Block (DOB) Core
  - Total faults 2183
  - Fault coverage 78.67%
  - Number of patterns 26

Test Cost (time) = $\sum_{i=1}^{Nc}\left(\left\lceil \frac{ff_i}{nsc_i} \right\rceil (p_i + 1) + p_i\right)\frac{1}{ftck_i}$

Nc	nr of modules
ff	nr of flip-flops
nsc	nr os scan-chains
p	nr of patterns
ftck	Test clock frequency

Simulation charts (EOCHL core)



- The test infrastructure in digital portion of ATLAS FEI4 IC is in place for production test
- The fault coverage figures are sufficiently high for this type of application
- Minimal area overhead, while the performance penalties are virtually none
- Reusability of the method
- Compliant to the industrial standards

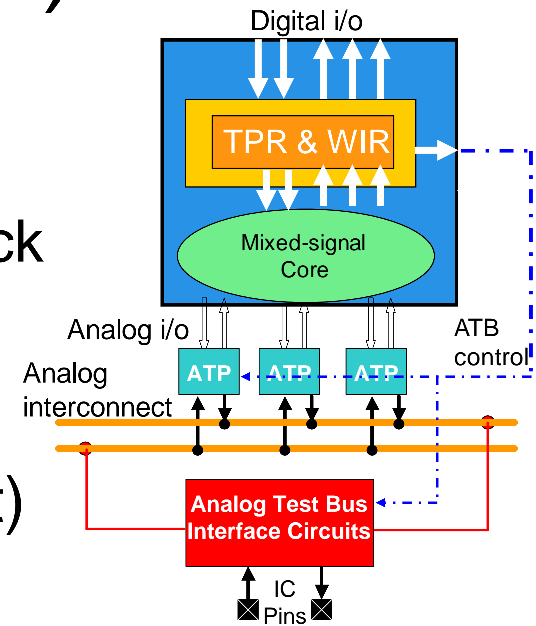
Future challenges

- Implementing the DfT in a digital portion only may not be sufficient – analog mixed-signal dedicated test approach needed
- Probability of the random defect landing on a random location leads to unpredictable quality levels

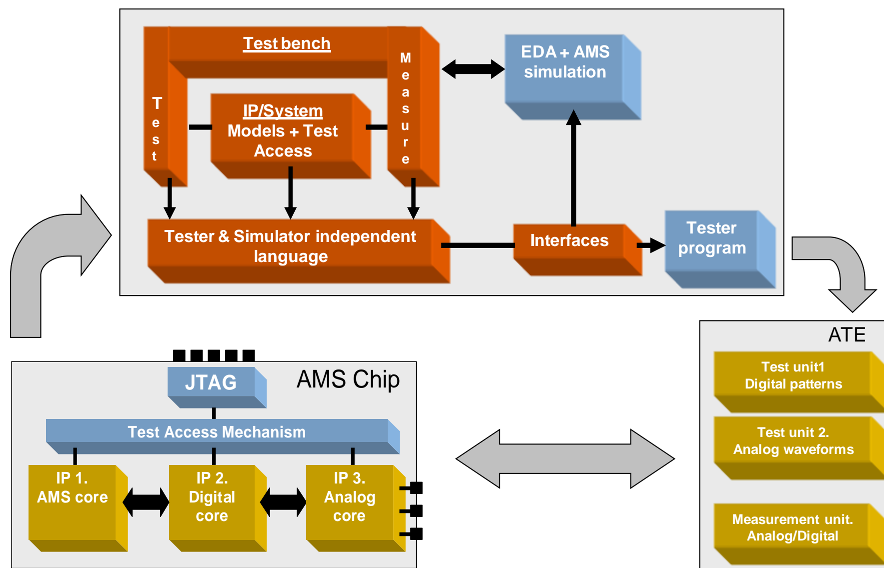
- Gaining in importance with smaller feature size

Future challenges (II)

- Apply Analog Mixed-Signal DfT/BIST
  - E.g. analog/mixed-signal test bus and/or digitally controlled patterns to test AMS block



- Automate the AMS Test Development (no analog ATPG tools available on the market)



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