The GBT – SerDes ASIC

P. Moreira[a], S. Baron[a], S. Bonacini[a], O. Cobanoglu[a], F. Faccio[a], S. Feger[a], R. Francisco[a], P. Gui[b], J. Li[b], A. Marchioro[a], C. Paillard[a], N. Panilla[b], D. Porret[a] and K. Wyllie[a]

TWEPP

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http://cern.ch/proj-gbt

[a] *CERN, 1211 Geneva 23, Switzerland*

[b] *SMU, Dallas TX 75275-0338, USA*

Outline

- *Radiation Hard Optical Link Architecture*
- *GBTX – To – Frontend*
- *The GBT – SerDes*
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  - Serializer:
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    - Hardening
    - Fast multiplexer
    - Measurements
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    - Architecture
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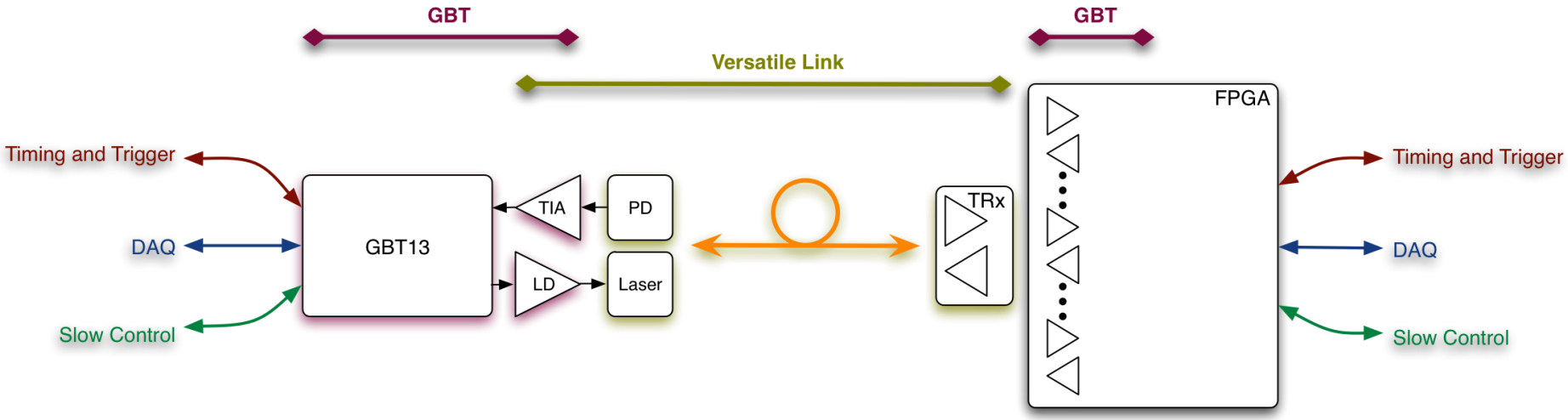
Radiation Hard Optical Link Architecture

Defined in the "DG White Paper"

- *"Work Package 3-1"*
  - Objective:
    - Development of an high speed bidirectional radiation hard optical link
  - Deliverable:
    - Tested and qualified radiation hard optical link
  - Duration:
    - 4 years (2008 – 2011)

Radiation Hard Optical Link:

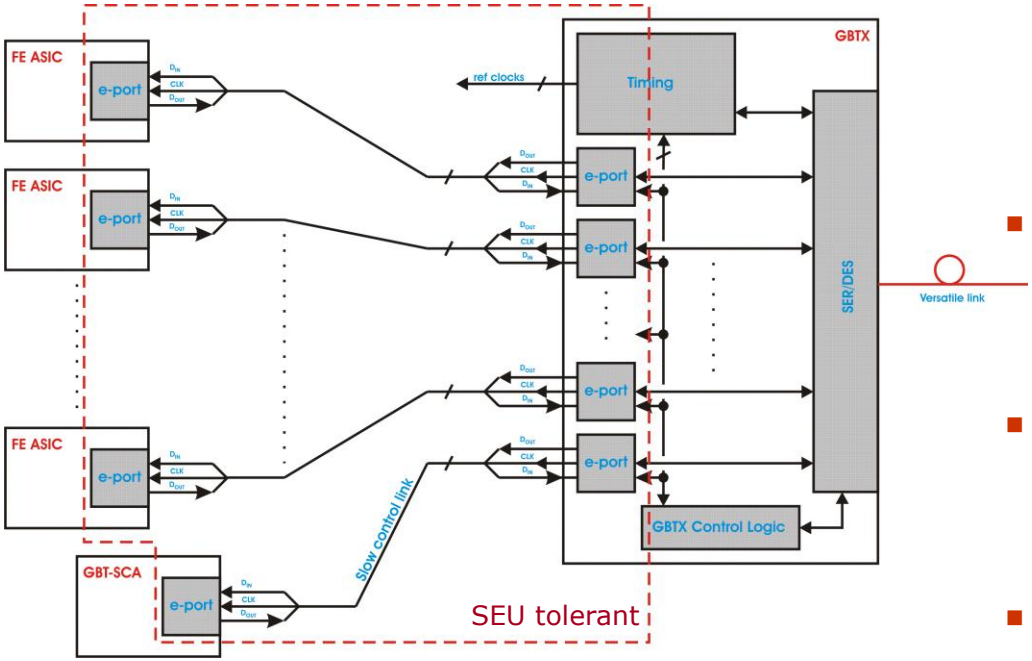
- *Versatile link project:*
  - Opto-electronics
  - Radiation hardness
  - Functionality testing
  - Packaging
- *GBT project:*
  - ASIC design
  - Verification
  - Functionality testing
  - Packaging



On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

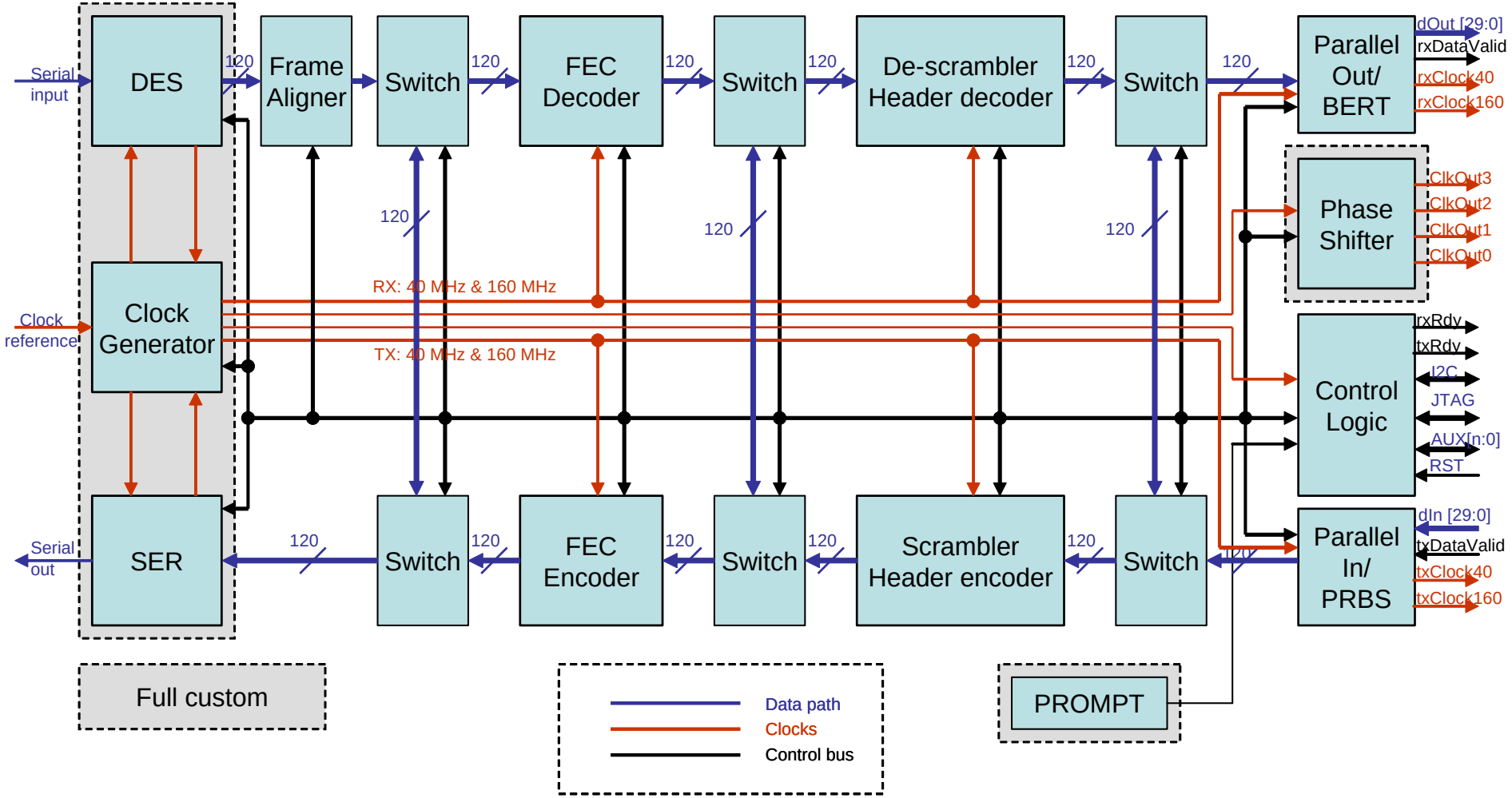
GBTX-TO-FRONTEND: E - Link Modes



Mode	Type	Data Rate	Notes
OFF	Power off	-	
P-Bus	parallel	80 MW/s	One 40-bit word (DDR)
B-Bus	parallel	80 MB/s	Up to 5 Bytes (DDR)
N-Bus	parallel	160 MN/s	Up to 5 Nibbles (DDR)
2 ×	serial	80 Mb/s	Up to 40 serial links
4 ×	serial	160 Mb/s	Up to 20 serial links
8 ×	serial	320 Mb/s	Up to 10 serial links
8 ×	serial-lanes	> 320 Mb/s	See "**Error! Reference source not found.**"

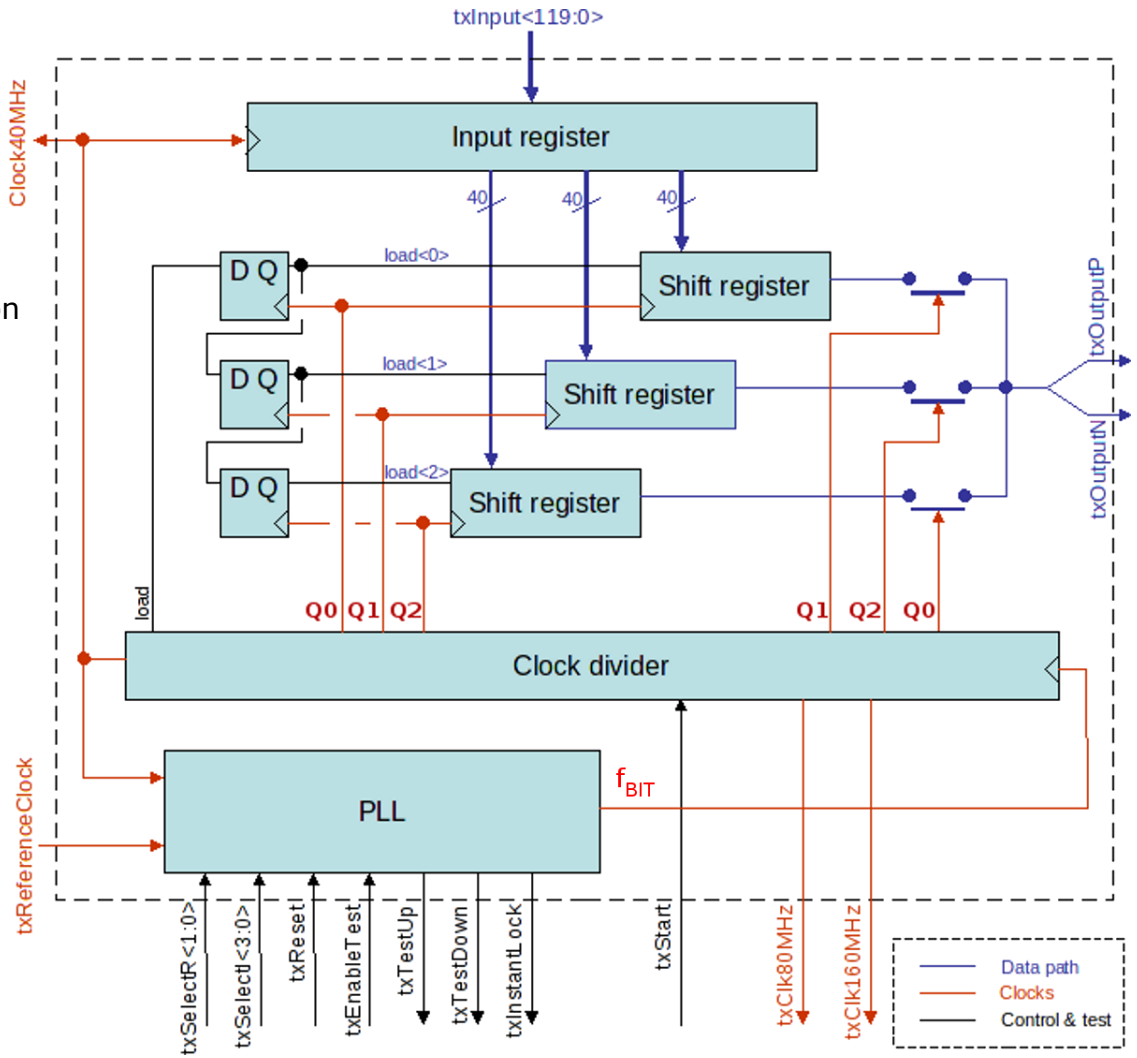
- *GBT/Frontend interface:*
  - Electrical links (e-link)
  - Serial
  - Bidirectional
  - Up to 40 links
- *Programmable data rate:*
  - Independently in five groups
  - Independently for up/down links
  - 80 Mb/s, 160 Mb/s and 320 Mb/s
- *Lanes:*
  - To achieve > 320 Mb/s
  - Two or more e-links can be grouped forming a "lane"
- *Slow control channel:*
  - 80 Mb/s
- *E-Link:*
  - Three pairs: $D_{OUT}/D_{IN}/CLK$
  - SLVS
- *E-Links will be handled by E-ports:*
  - Electrically
  - "Protocol"
- *Package (preliminary):*
  - BGA: 361 – PINS
  - 16 mm x 16 mm, 0.8 mm pitch

GBT – SerDes: Architecture



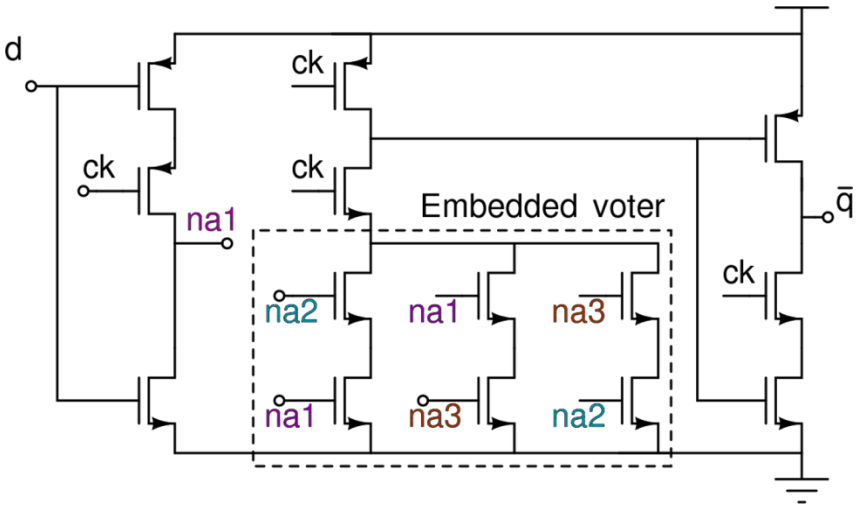
Serializer: Architecture

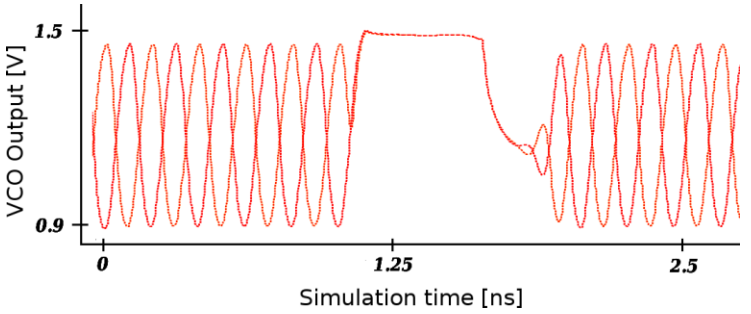
- *Serializer:*
  - 4.8 Gb/s
  - 120-bit shift register
    - 3 × 40-bit shift register (f=1.6 GHz)
    - 3-to-1 fast multiplexer (f=4.8 GHz)
- *Data path:*
  - No SEU protection
  - SEUs handled by the Reed-Solomon CODEC
- *Clock divider:*
  - Divide by 120
  - f = 4.8 GHz
  - Triple voted for SEU robustness
- *PLL:*
  - SEU hardened VCO
  - SEU hardened Clock Divider
    - Based on "custom" dynamic flip-flop

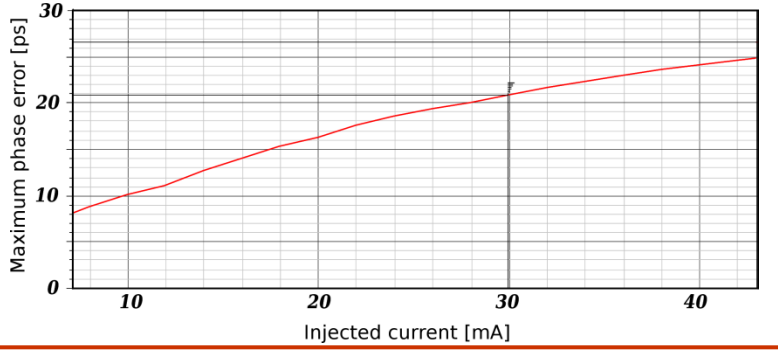


Serializer: Hardening

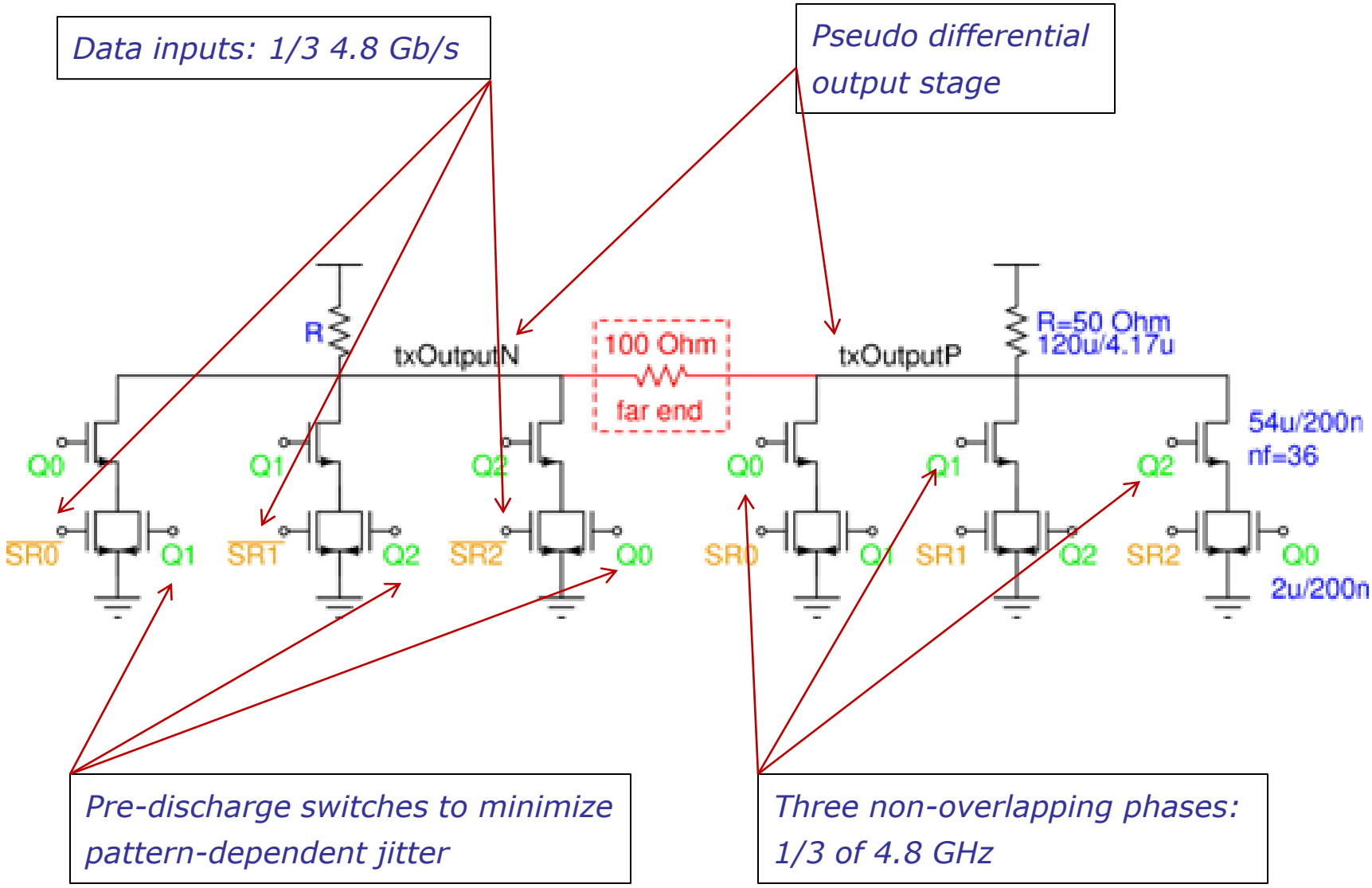
- *Clock divider:*
  - A "missing" count on the clock divider unlocks the PLL resulting in a burst of errors lasting for "μs"
- *TMR in the counter mandatory:*
  - A voter + a static DFF is far to slow!
  - Even a voter + a dynamic DFF will not pass the corner simulations!
  - A new "voted DFF" is proposed and used in the GBT-SERDES
- *VCO:*
  - Depending on the charge injected, an SEU can stop the VCO oscillations for a few cycles!
  - SEUs were modeled by current pulses injecting 300 fC in 10 ps
  - The VCO current is set so that an SEU event causes a phase shift which is a fraction of the bit period.
  - Penalty: high power consumption.





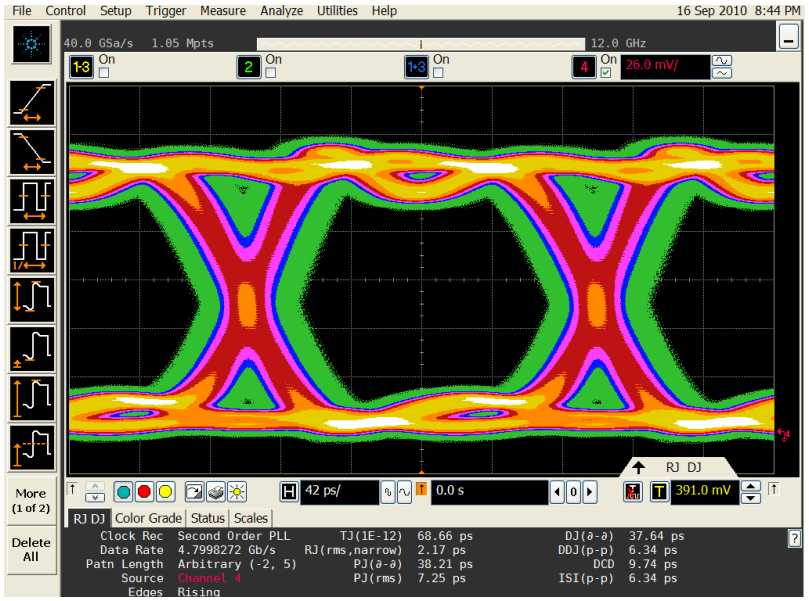


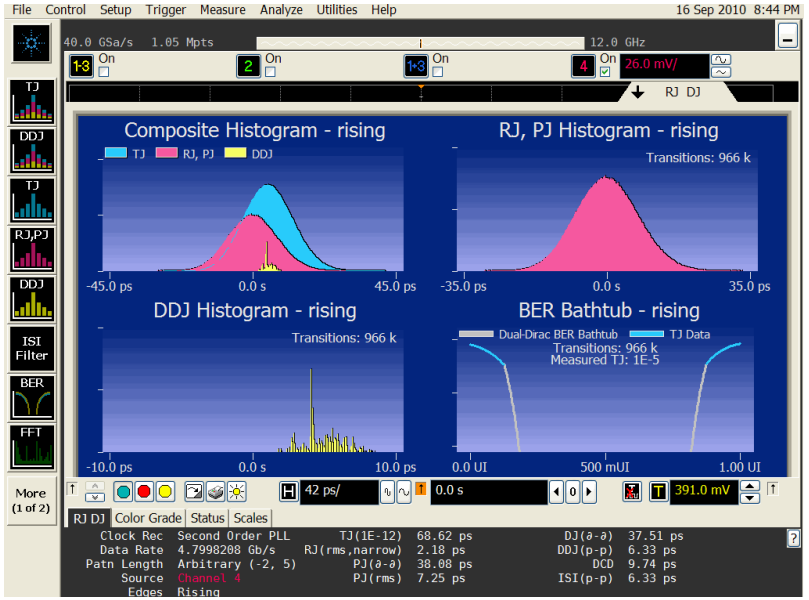
Serializer: Fast Multiplexer



Serializer: Measurements

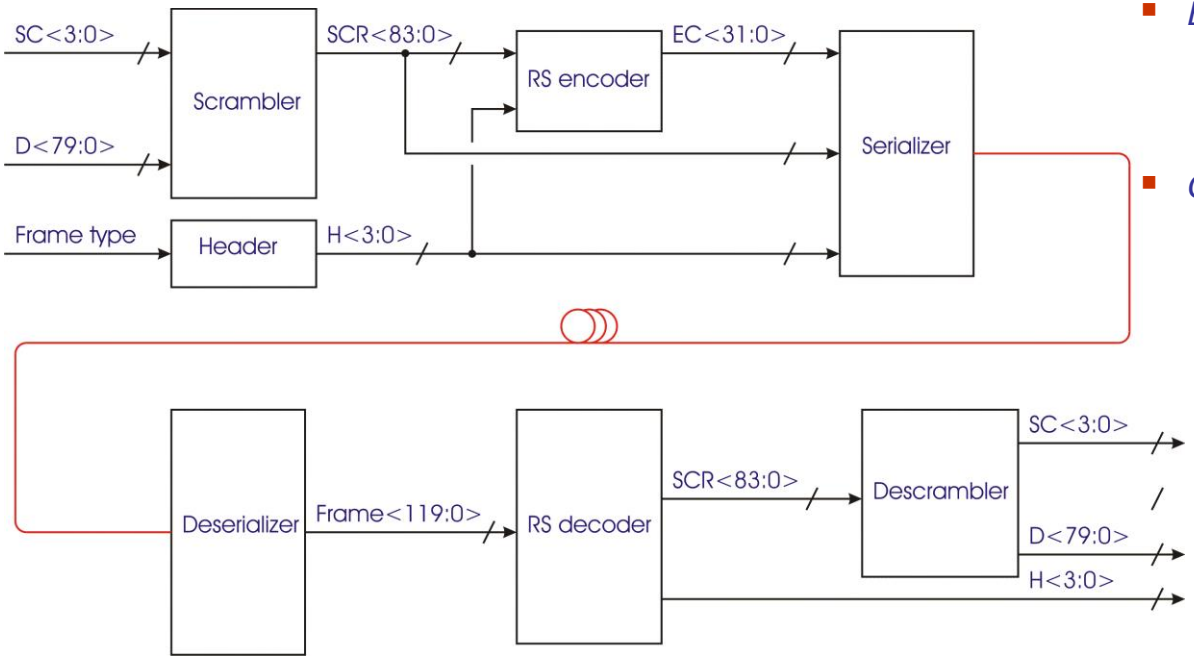
- *Tx Jitter:*
  - Total jitter ($1e^{-12}$): 68.7 ps
  - Random jitter: 2.2 ps (rms)
  - Deterministic jitter: 37.6 ps
    - Data dependent: 6.3 ps
    - Periodic:
      - RMS: 7.2 ps
      - PP: 38.2 ps
    - Duty-cycle-distortion: 9.7 ps
    - Inter-symbol interference: 6.3 ps





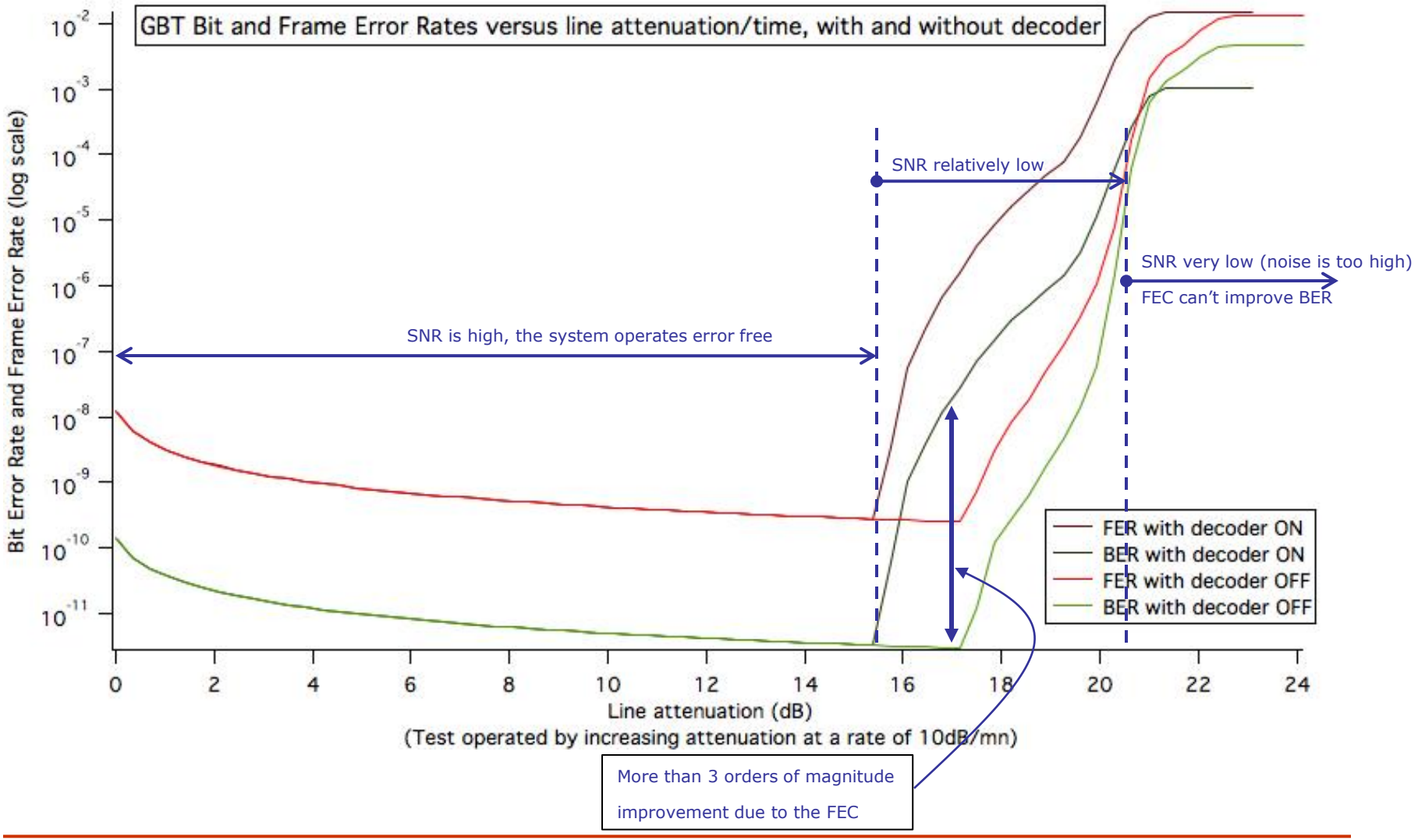
Line Coding/Decoding

- *High rates of Single Event Upsets (SEU) are expected for HL – LHC links:*
  - Particle "detection" by Photodiodes used in optical receivers.
  - SEUs on PIN-receivers, Laser-drivers and SERDES circuits
- *The GBT high speed data path is not SEU hardened!*
- *Transmitted data is however protected by a Forward Error Correction (FEC) code*



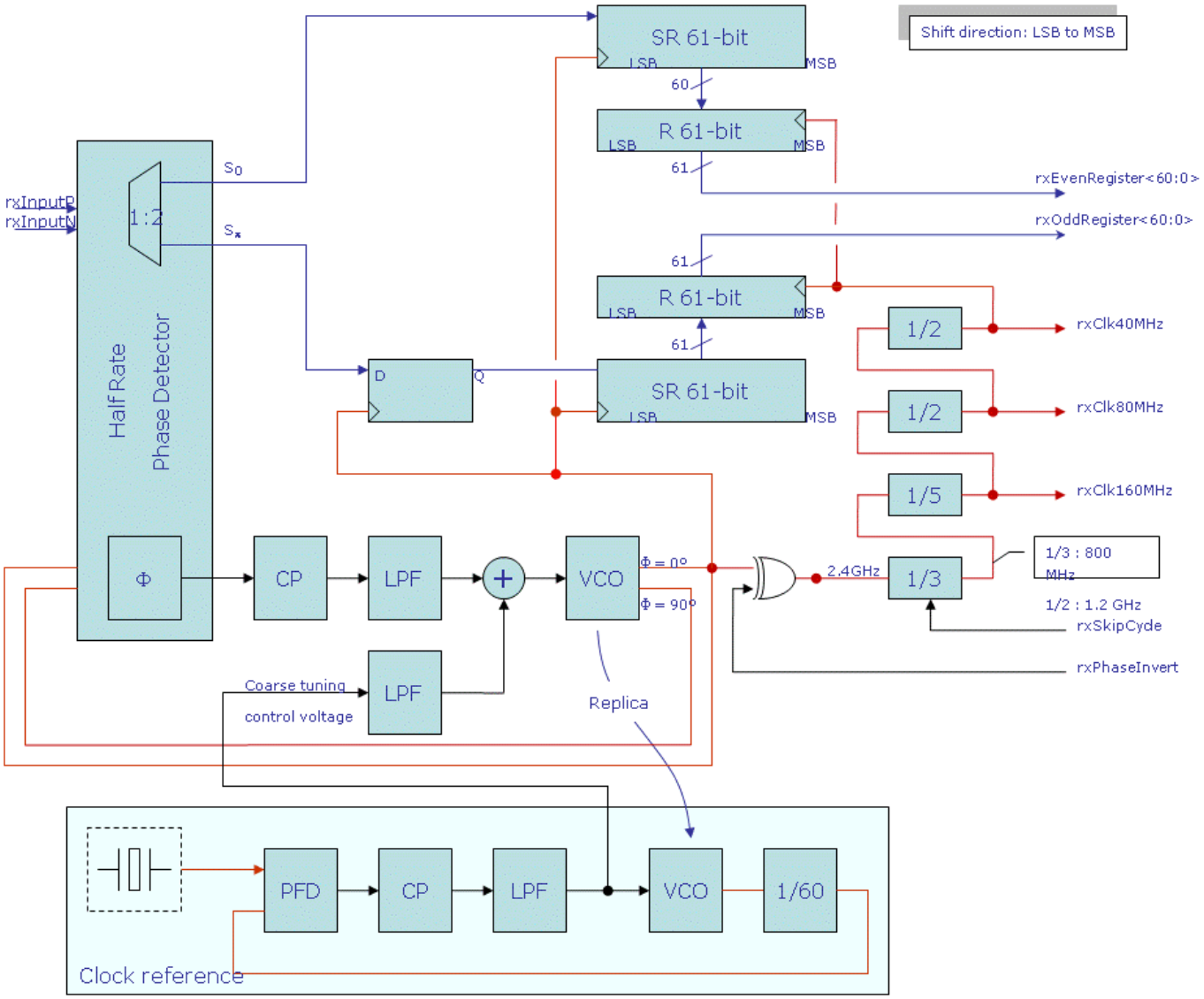
- *Scrambler:*
  - *4 × Maximum run length 21-bit scrambler*
- *FEC code:*
  - *Interleaved Reed-Solomon double error correction*
  - *4-bit symbols (RS(15,11))*
  - *Interleaving: 2*
- *Error correction capability:*
  - *2 (Interleaving) × 2 (RS) = 4 symbols = 16-bits*
- *GBT frame efficiency: 70%*
  - *A line code is always required for DC balance and synchronization*
  - *For comparison, the Gigabit Ethernet frame efficiency is 80% (at the physical level)*
  - *At a small penalty (10%, when compared with the Gigabit Ethernet) the GBT protocol will offer the benefits of Error Detection and Correction*

BER Measurements



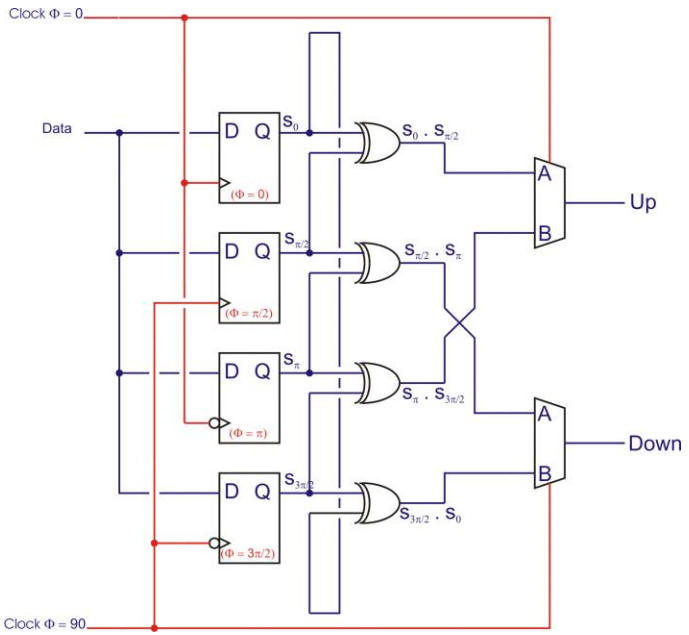
CDR: Architecture

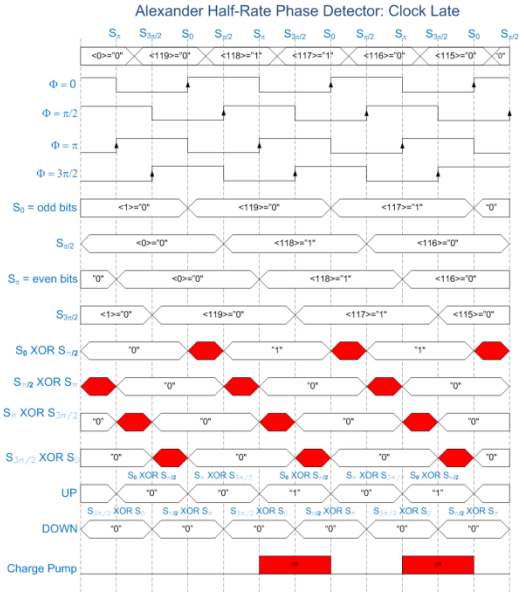
- *Dual PLL CDR Loop:*
  - 1st Loop: Frequency centering PLL
  - 2nd Loop: CDR
  - Allows to reduce the CDR VCO gain for lower Jitter
- *Half-Rate:*
  - Phase-detector
  - Frequency-detector
- *Constant latency frame alignment circuit*
- *As for the serializer:*
  - Unprotected data path
  - TMR clock divider
  - SEU hardened VCO

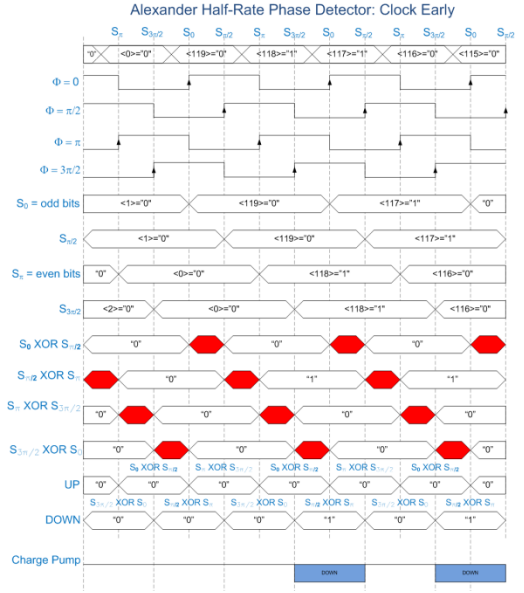


CDR: Half-Rate Phase Detector

- *Advantages:*
  - Clock runs at f/2
  - Data is automatically retimed
  - VCO design "can be" relaxed
  - "Only" serial data sampling operation remains critical!
- *Disadvantages:*
  - Four well controlled clock phases are needed
  - One bit period uncertainty on the clock phase:
    - Is the ½ rate clock phase aligned with an "even" or "odd" bit?
    - Constant latency requires this phase uncertainty to be resolved latter (only important in HEP applications)





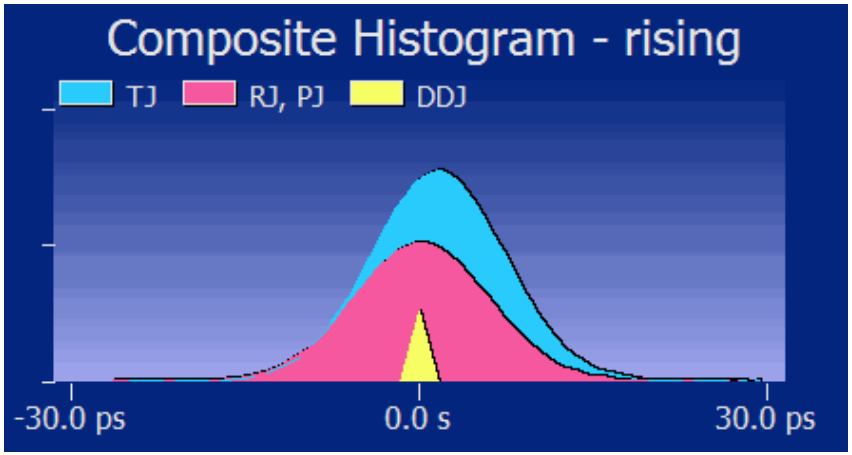


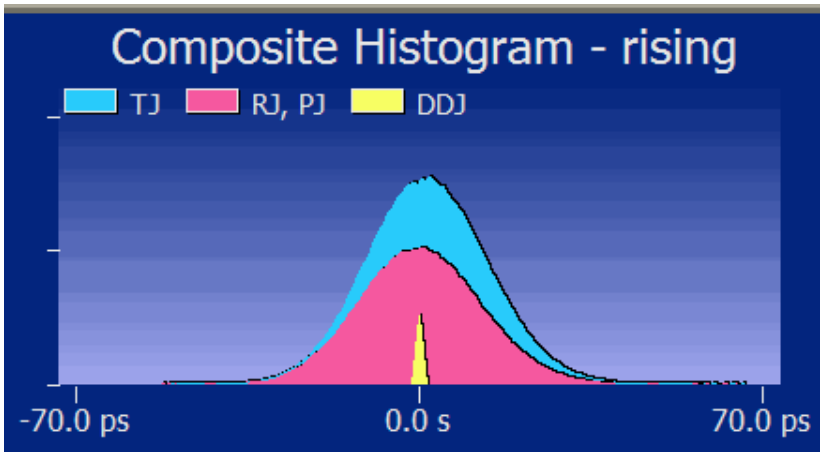
CDR: Measurements

Recovered Clock: 40 MHz

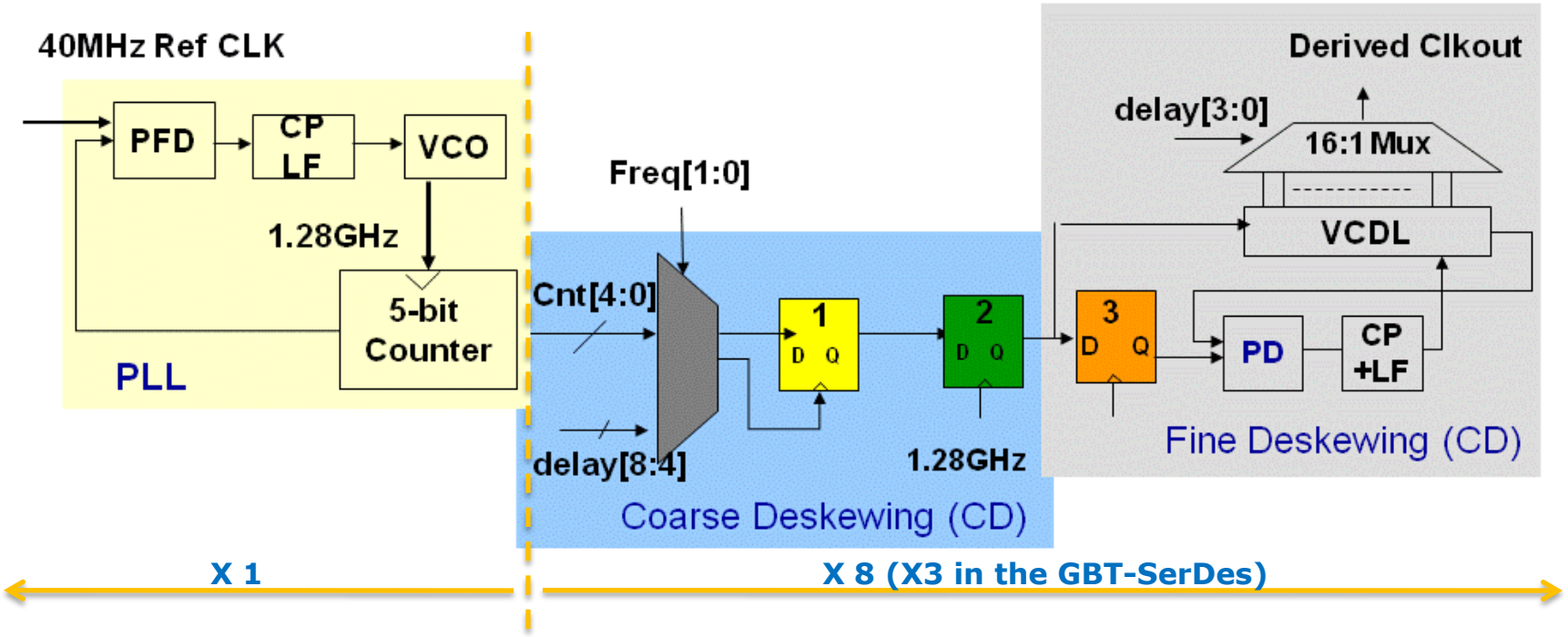
- *Fixed pattern:*
  - Total jitter ($1e^{-12}$): 60 ps
  - Random jitter: 2.2 ps (rms)
  - Deterministic jitter: 27.5 ps (pp)
    - Periodic:
      - RMS: 5.6 ps
      - PP: 28 ps

- *PRBS:*
  - Total jitter ($1e^{-12}$): 159 ps
  - Random jitter: 9.5 ps (rms)
  - Deterministic jitter: 24 ps (pp)
    - Periodic:
      - RMS: 7.8 ps
      - PP: 24 ps





Phase – Shifter: Architecture



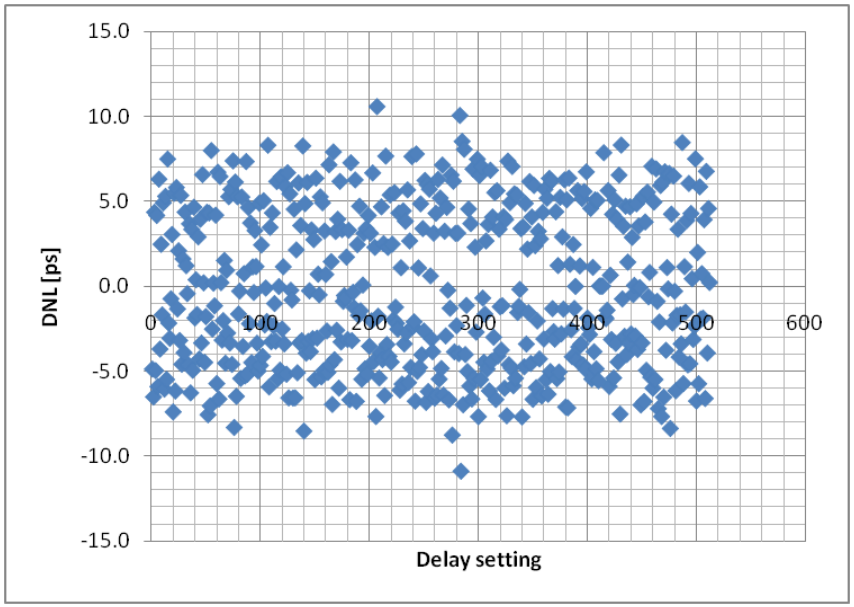
Main features:

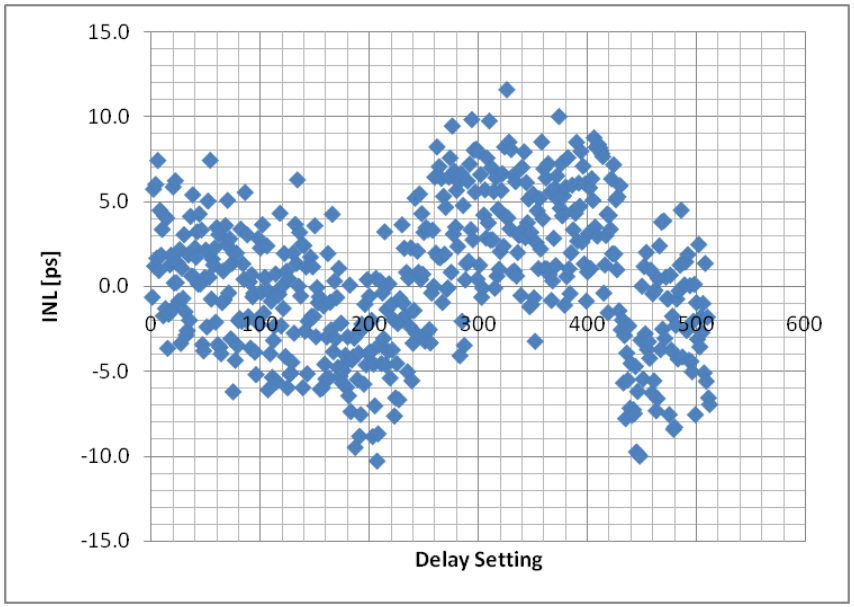
- 3 channels in the GBT – SerDes
- 1 PLL + Counter generates the three frequencies: 40 / 80 and 160 MHz
- 1 DLL per channel: 48.83 ps resolution
- Mixed digital/analogue phase shifting technique:
  - Coarse deskewing – Digital: Δt(coarse) = 781.25 ps
  - Fine deskewing – Analogue: Δt(fine) = 48.83 ps
- Power consumption: 5.6 mW/channel (simulated)
- Differential non-linearity: DNL <6.7% LSB
- Integral non-linearity: INL<6.5% LSB

} Predicted by simulation

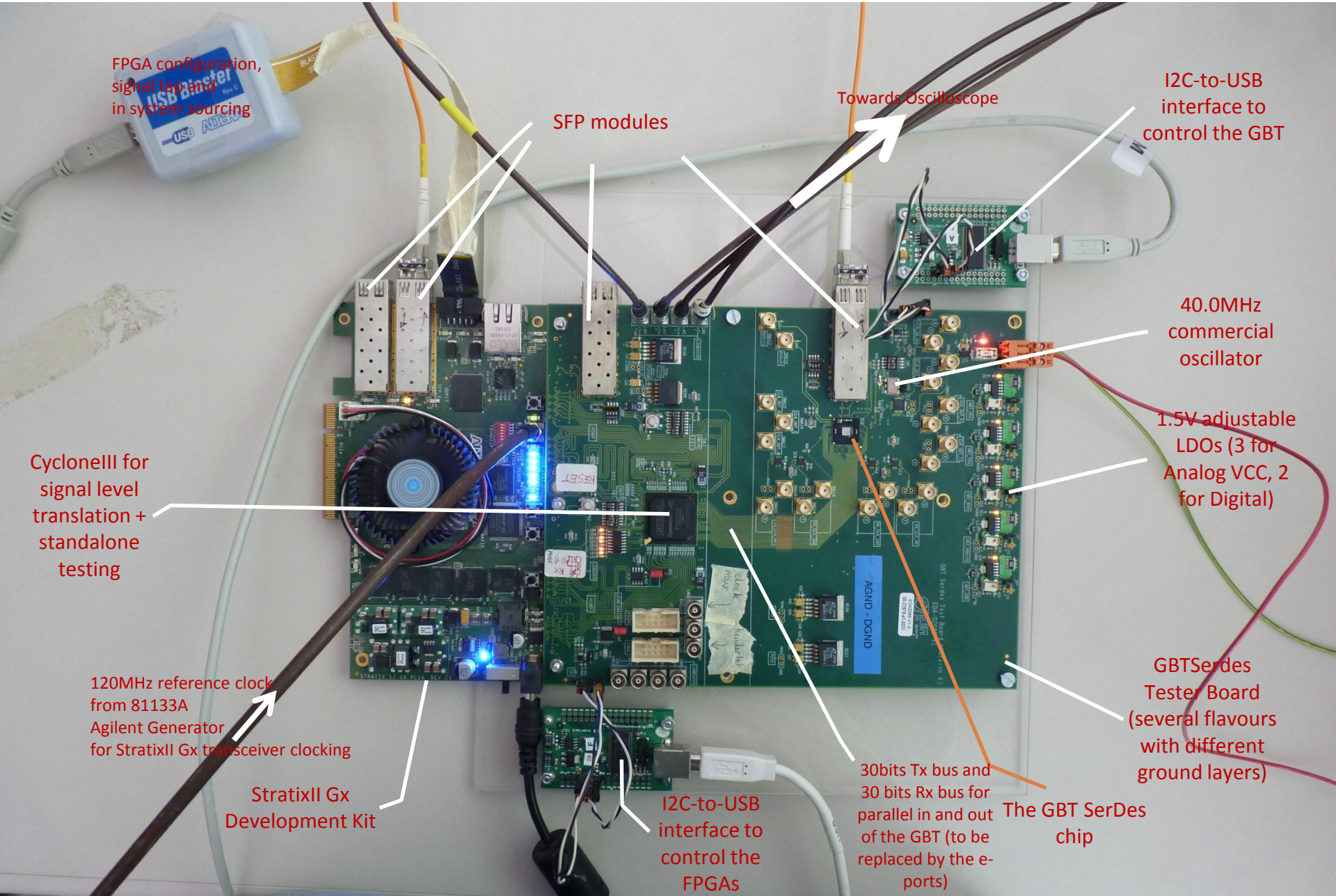
Phase – Shifter: Measurements

- **Resolution:** Δt = 48.83 ps
- **Jitter:** σ = 5 ps (pp = 30 ps)
- **Differential Non-Linearity**:
  - σ = 4.7 ps (9.6% of Δt)
  - pp = 21.5 ps (44% of Δt)
- **Integral Non-Linearity**:
  - σ = 4.3 ps (8.7% of Δt)
  - pp = 21.9 ps (48.7% of Δt)





Test Setup


FPGA configuration, signal tap and in system sourcing
SFP modules
Towards Oscilloscope
I2C-to-USB interface to control the GBT
40.0MHz commercial oscillator
1.5V adjustable LDOs (3 for Analog VCC, 2 for Digital)
CycloneIII for signal level translation + standalone testing
120MHz reference clock from 81133A Agilent Generator for StratixII Gx transceiver clocking
StratixII Gx Development Kit
I2C-to-USB interface to control the FPGAs
30bits Tx bus and 30 bits Rx bus for parallel in and out of the GBT (to be replaced by the e-ports)
The GBT SerDes chip
GBTSerdes Tester Board (several flavours with different ground layers)
AGND - DGND

Summary

- *The GBT – SerDes:*
  - Fabricated in 130 nm CMOS technology
  - Packaged in a custom 13 × 13 bump-pad C4 package (168 pin)
- *A test bench was developed based on:*
  - StratixII Gx Development Kit
  - Test board with different ground options
- *Almost all of the functions proved 100% functional:*
  - Serializer
  - Frame-Aligner
  - Constant-latency "barrel-shifter"
  - Encoder/Decoder
  - Scrambler/Descrambler
  - Phase-shifter
  - Logic
  - Parallel I/O interface
- *For the De-serializer*
  - The clock recovery function works fine over the full range
  - However, error free data reception at 4.8 Gb/s has not (yet?) been achieved!
    - OK up to 2.4 Gb/s