The front-end Electronics for the LHCb upgrade.

Jan Buytaert (*C.E.R.N.*)

On behalf of the LHCb collaboration.

TWEPP 2010 Workshop, Aachen,
September 21, 2010

Outline :

- The LHCb upgrade plan & main issues.
- The new trigger/daq architecture.
- Overview of the subdetector modifications.
- Subdetector electronic developments.
- Summary.

The LHCb upgrade.

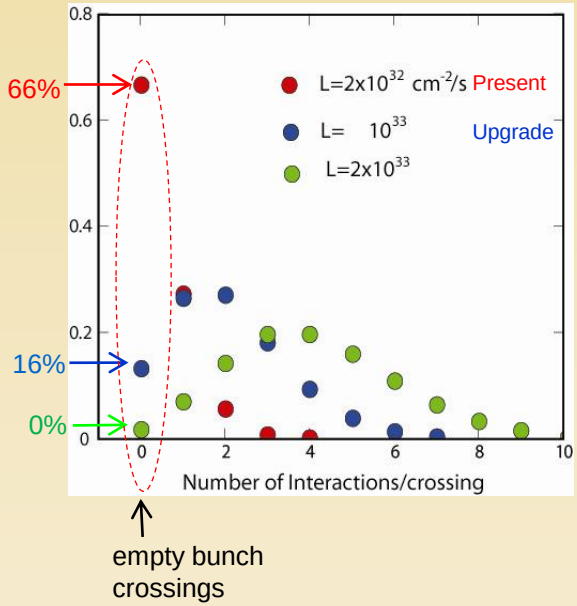
- The Plan:

	E	Peak $\mathcal{L}$ ($10^{32}cm^{-2}s^{-1}$)	$\int \mathcal{L}$	
2011	7 TeV	2	1 fb^{-1}	= LHCb design luminosity !
2012				
2013	>10 TeV	2	1 fb^{-1}	
2014	>10 TeV	2	2 fb^{-1}	
2015	>10 TeV	2	2 fb^{-1}	Total $\int \mathcal{L}$ ~ 6 fb^{-1}
2016				Install LHCb upgrade !
2017	>10 TeV	10	10 fb^{-1}	
2018	>10 TeV	10	10 fb^{-1}	

- The increase in luminosity 'only' requires stronger beam squeezing , i.e. does not depend on any LHC upgrade.
- A 'letter of intent' will be submitted very soon to LHCC.

The occupancies.

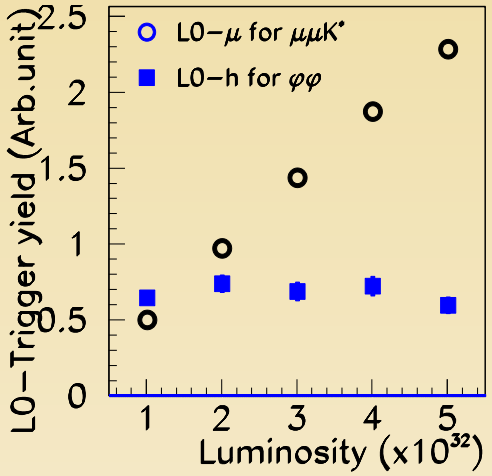
Peak L ($10^{32}cm^{-2}s^{-1}$)	2	10	20
Average # of interactions/crossing	0.4	2.0	4.0
Average # of interactions/non-empty crossing	1.3	2.4	4.3



- The occupancies will only increase by ~ 2 due to multiple interactions.
- The current detector granularities are adequate and no major detector changes required.
- The exact beam conditions are under discussion with LHC.

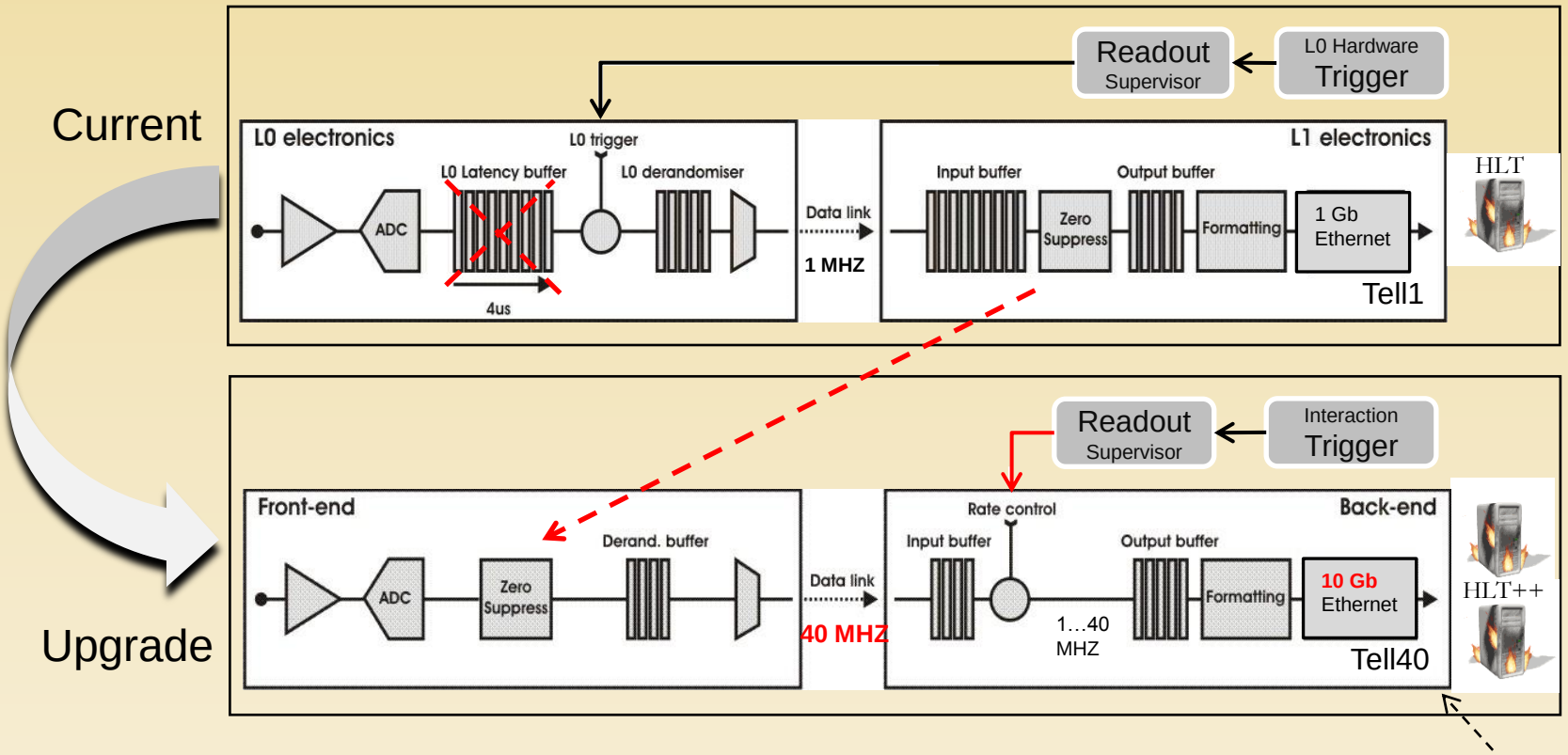
L0 trigger efficiency.

- **Problem**: the L0 hadron hardware trigger loses efficiency at higher luminosities. The event yield is even dropping...
  - Because the DAQ event readout rate is limited to 1MHz, the trigger thresholds must be raised …



- **2 solutions:**
  - A more sophisticated hardware hadron trigger or
  - No hardware trigger, increase the readout rate and implement trigger in a CPU farm !
    - Full detector information available.
    - Flexible algorithm.
    - Double the hadron trigger efficiency .

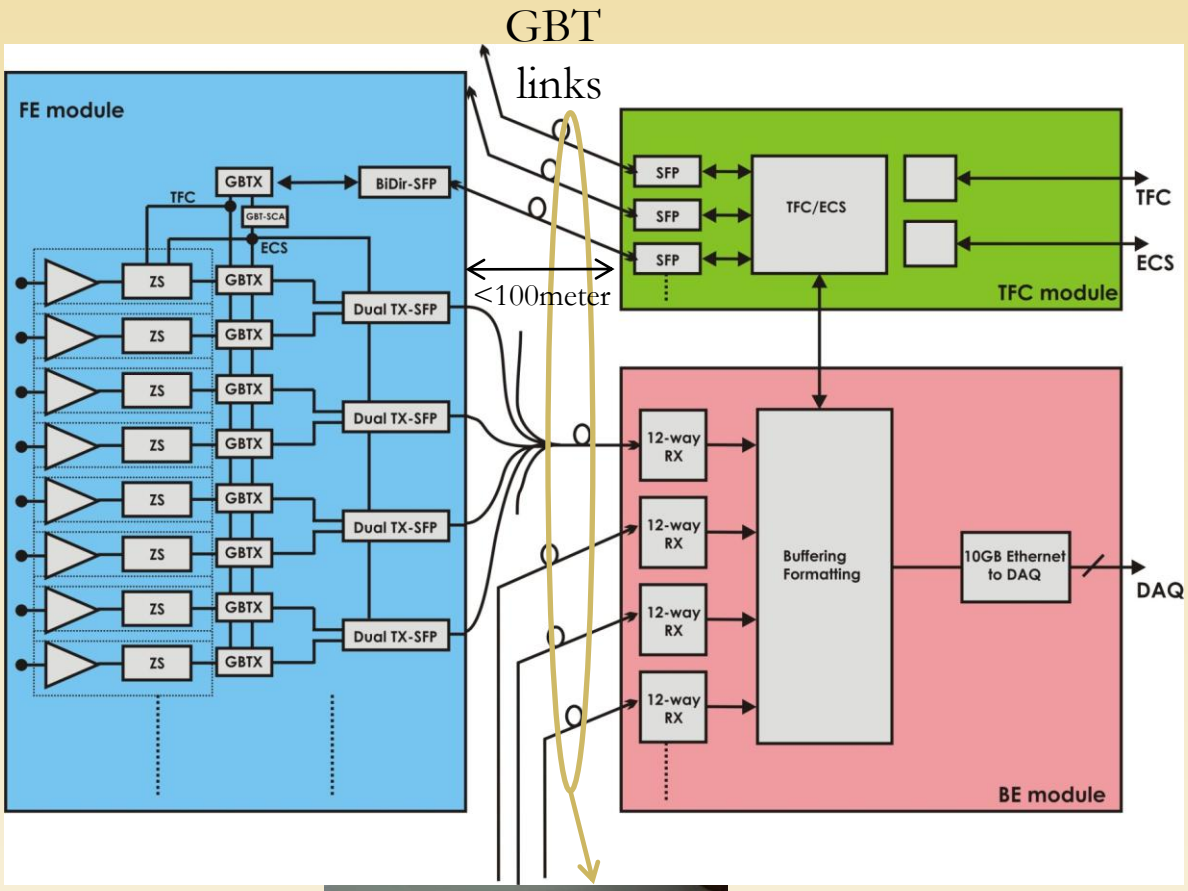
New Trigger/DAQ architecture.



- All frontend electronics must be adapted or redesigned to
  - readout all collision data @ 40MHz
  - and zero-suppress to minimize data bandwidth.
- The L0 hardware trigger is re-used to reduce the event rate to match the installed router and CPU farm capacity (staging). Initially run at ~ 5MHz.

(Tell 40: talk of J.P. Cachemiche on wednesday)

Typical Subdetector readout & control:



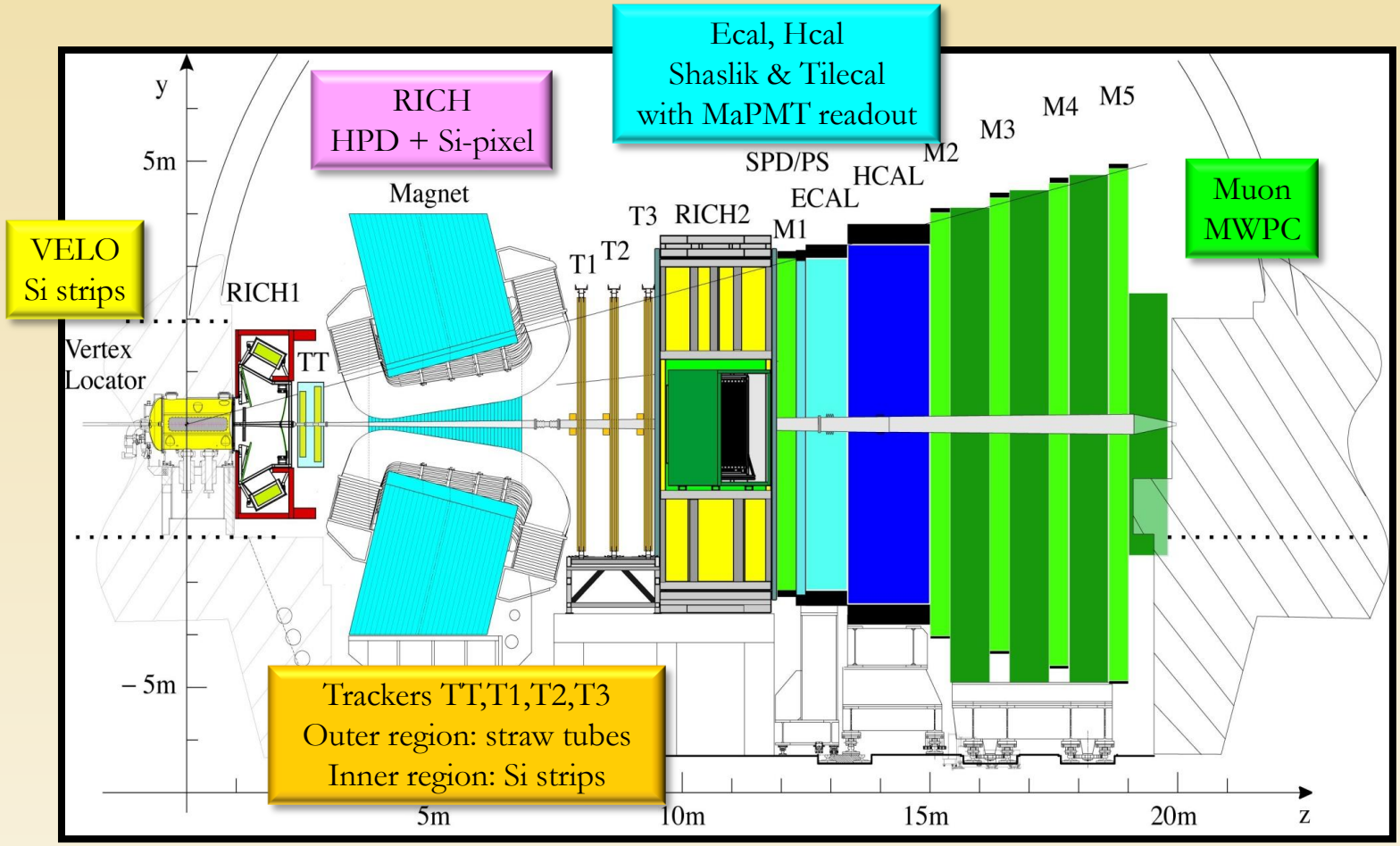

Bundle of 8 x 12way ribbon

- Number of GBT links:

	Data	TFC/ ECS
Velo	2496	52
OT	3456	72
IT	1200	~100
RICH	2476	~200
Calo	952	238
Muon	1248	104
Total =	11684	766

- Total optical links required ~ 13000.
- LHCb has already 8300 links installed today.

LHCb detector.



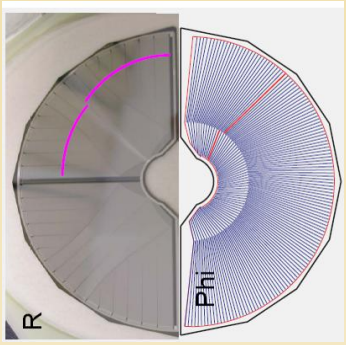
(See talk of K. Henessy on Friday).

Main detector modifications.

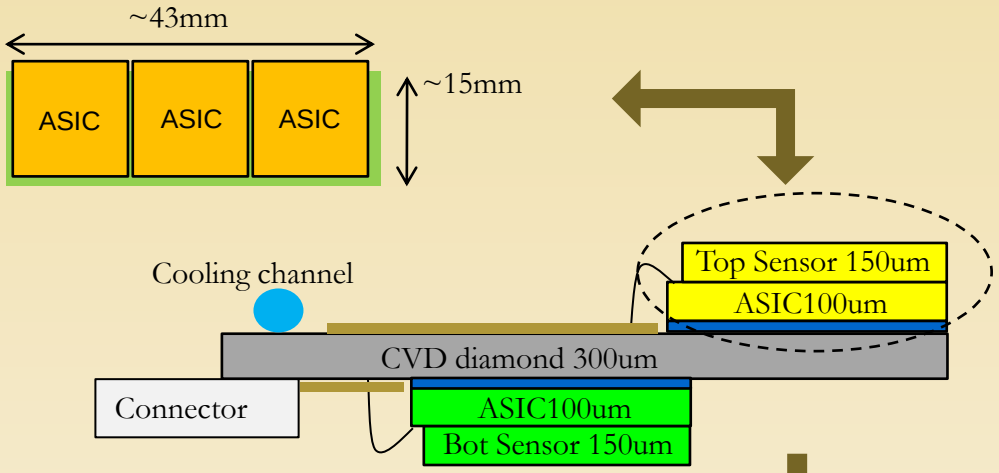
- VELO and RICH:
  - Fullz new sensor modules and photon detectors (because they are highly integrated with the FE-electronics) :
    - VELO : pixel sensors will replace R-Phi strip sensors.
    - RICH : multi-anode PMT's will replace Hybrid photon detector (HPD) tubes.
- Tracker :
  - Inner Tracker : Keep current Si strip sensors or use scintillating fibers.
  - Outer Tracker : Keep straw tubes and part of the FE electronics.
- Calorimeters:
  - Keep MaPMT's, but at reduced HV to avoid ageing.
    - -> 5x lower signal gain -> to maintain S/N, need lower noise -> new amplifiers …
  - Possibly remove pre-shower (PS) and scintillating pad (SPD).
- Muon:
  - Detector and FE electronics stay unmodified.
  - The M1 station will be removed.

VELO upgrade.

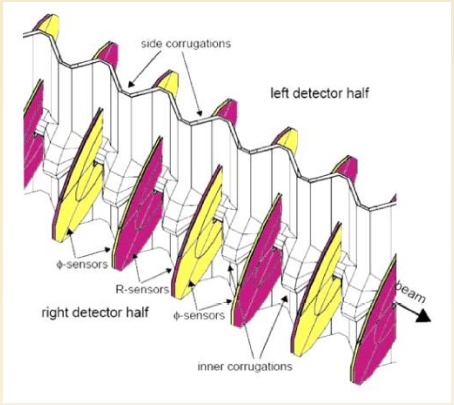
Current VELO R&Phi strips

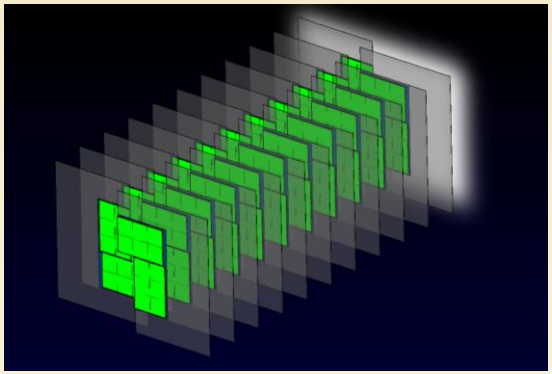


Upgrade : Pixel Sensor tile

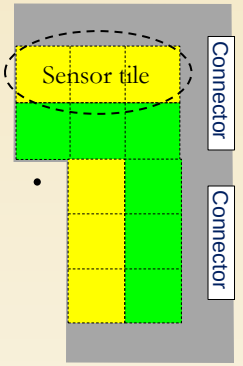


Current VELO module layout





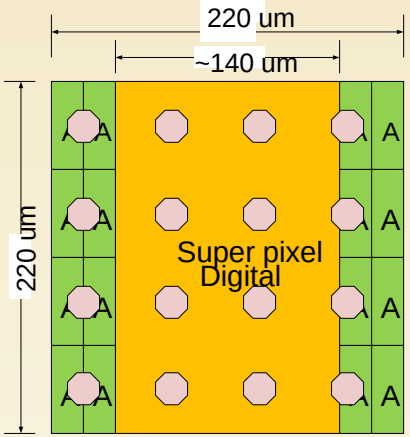
Pixel module



VELO upgrade.

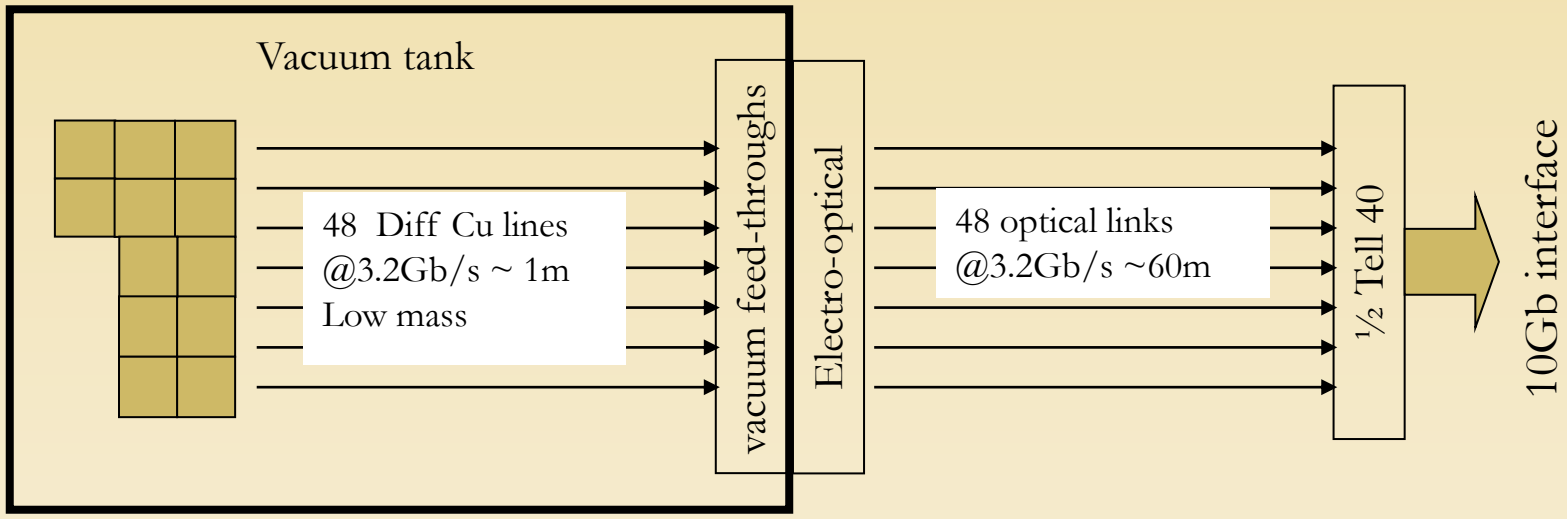
- Design of a readout asic VELOPIX' in close collaboration with TimePix2.
  - 256x256 pixel array, 55um x 55um pixel size.
  - Minimal insensitive area (~5%)
  - Analog requirements identical.
  - Simultaneous meaurement of Time-over-threshold and time identification of hits.
  - Radiation hardness TID 400Mrad.
- Specific VELOPIX:
  - Highest average particle rate is 200MHz/cm^2. =>12Gb/s data generation rate /asic !
  - Clustering and formatting in pixel.
  - 'Superpixel' = group digital logic of 4x4 pixels in a single area.
  - High speed column readout (8bit@40MHz).
  - 4 multi-Gbit output links.
  - Total power budget < 3W@ 1.2 V

Bipolar Input charge	
Leakage current compensation	
Peaking time	≤ 25ns
Preamp output linear dynamic range	< 40 Ke-
ENC (σ_{ENC})	~75 e-
Detector capacitance	< 50 fF
Discriminator response time	< 2ns
Full chip minimum detectable charge	< 500 e-
Threshold spread after tuning	< 30 e-
Pixel analog power consumption @ 1.2V	< 15-20 µW



VELO upgrade.

Module readout concept :



- Total of 52 modules in full system.
- Work is starting on the link technology.

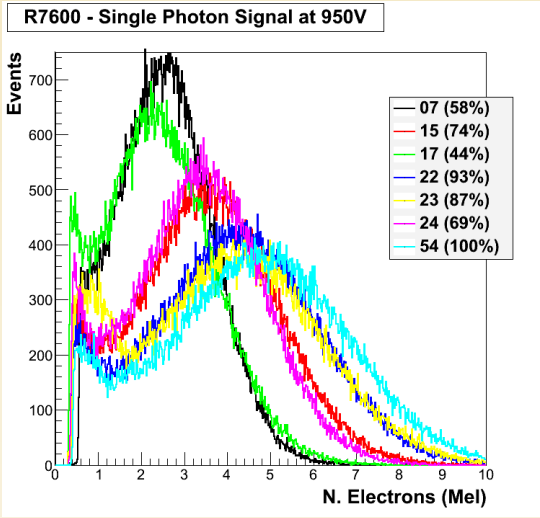
RICH upgrade.

Change of photon detector :

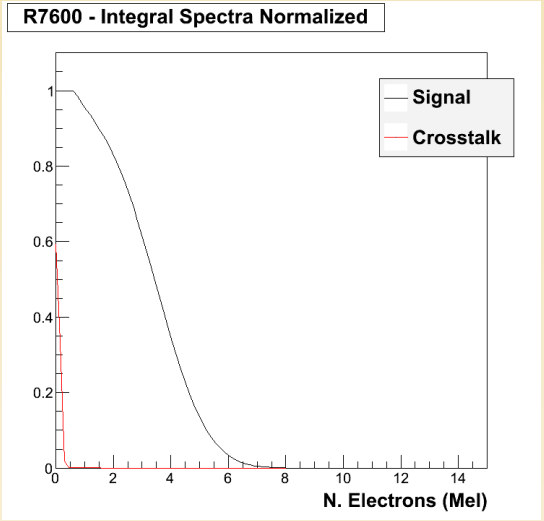
32×32 pixels
Pixel size 2.5×2.5 mm2

8×8 pixels
Pixel size 2×2 mm2

Larg pixel gain variation.
=> Electronic gain must be adjustable per pixel.



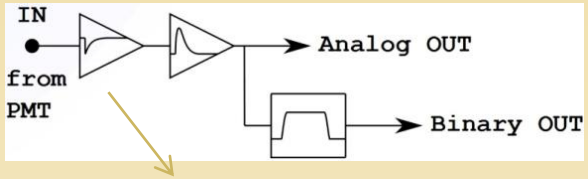
Inter-pixel crosstalk in R7600 is much less than in previous models :

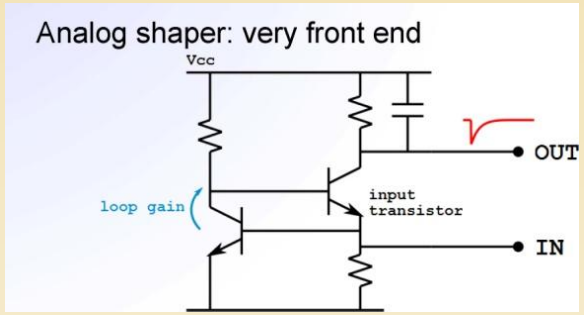


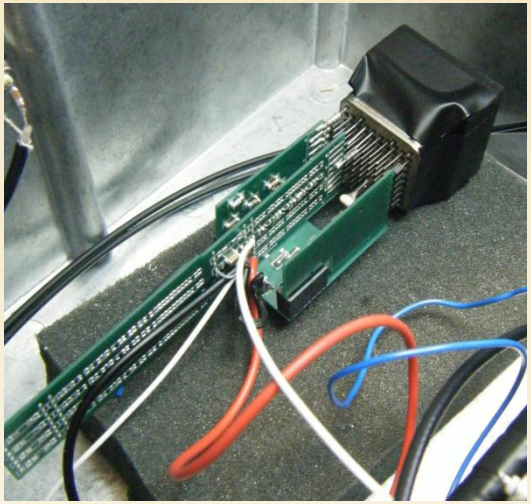
RICH upgrade.

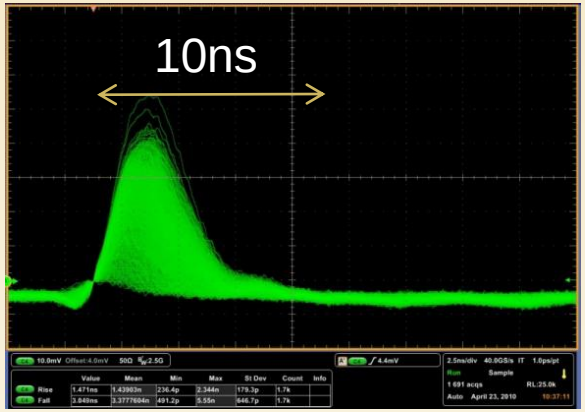
Discrete component prototyping:

- 8-channel PCB
- Using SiGe npn transistors.
- Total power dissipation < 10 mW/channel
- Low noise ~2.2nV/√Hz
- rise-time =1.4 ns, fall-time = 4ns
- Next:
  - Start design of asic version.
  - Prototype of digital functionality in FPGA.



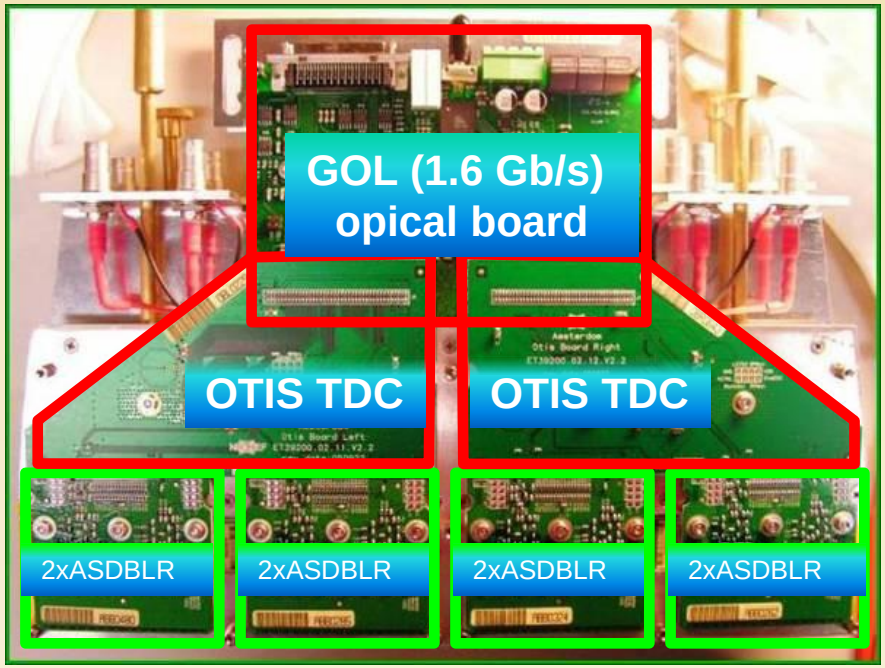


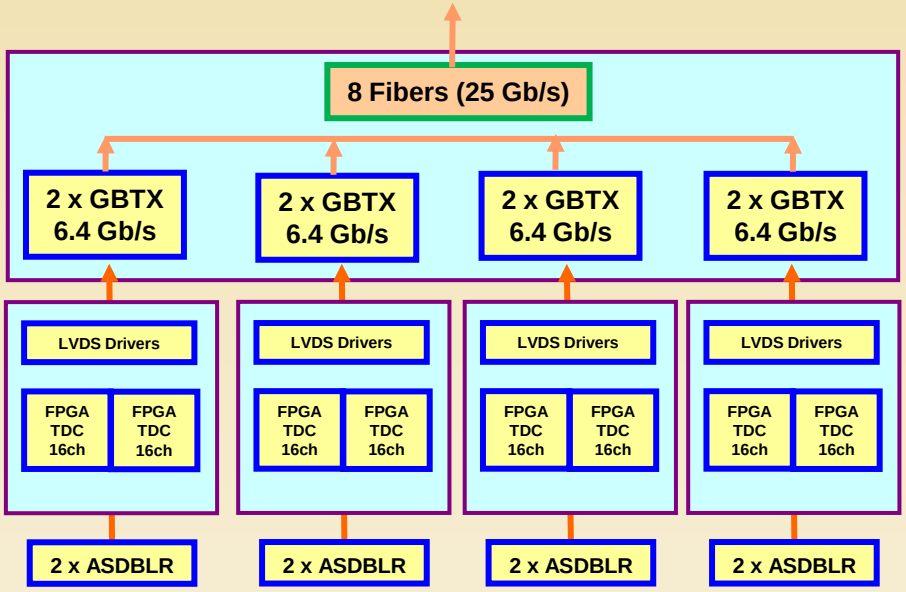




Outer Tracker upgrade.

Current FE boards (432) → Upgrade



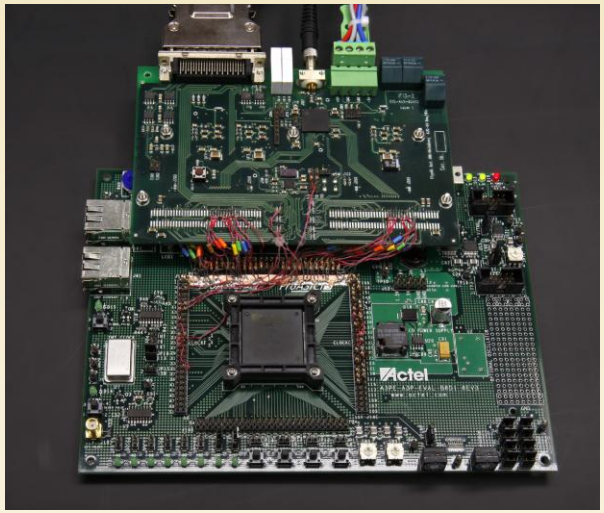


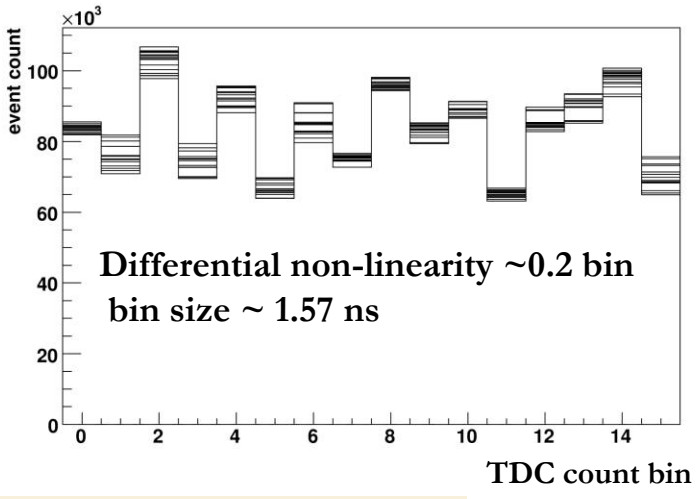
- ASDBLR boards are reused.
- OTIS TDC replaced by FPGA TDC.
- 1GOL replaced by 8 GBT

Outer Tracker upgrade.

- All logic is implemented in ACTEL Proasic3E FPGA for radiation tolerance .
  - 16 Channel 4 bit TDC design finished.
    - INL and DNL checked.
    - Good temperature stability checked.
  - Zero Suppression and data formatting.
  - Output on parallel bus (20 bit @ 160 MHz) to GBT.
  - I2C interface for configuration.

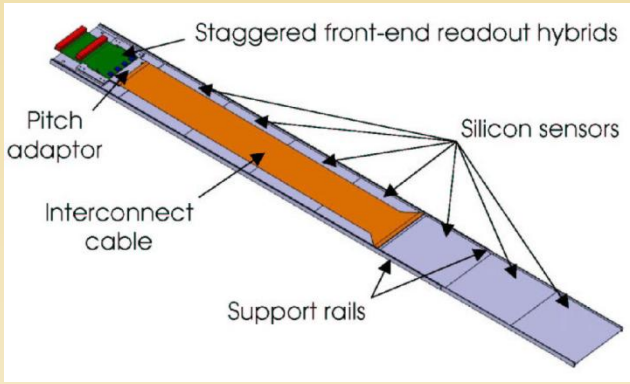
Prototyping :

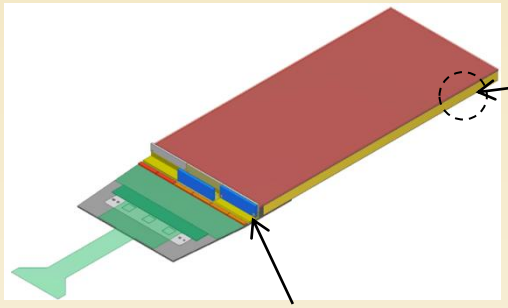




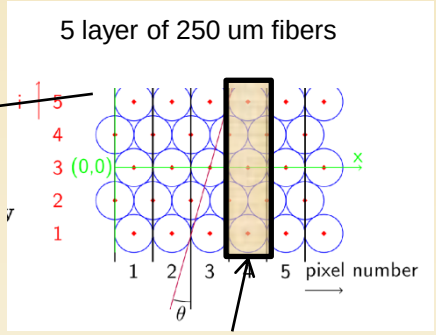
Inner Tracker upgrade.

- Option1 : reuse Si strip ladders. ⟶
  - Need to develop a new rad-hard, binary ASIC (cfr ATLAS) with 40MHz readout… not yet started.
- Option 2 : Scintillating fibers with SiPM readout.



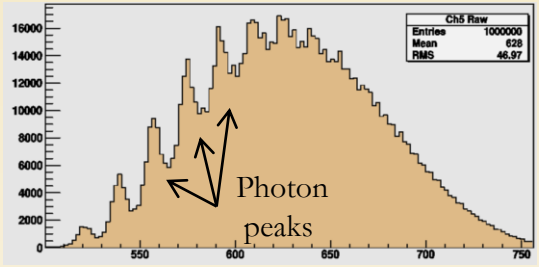


128 SiPM array



SiPM cell coverage

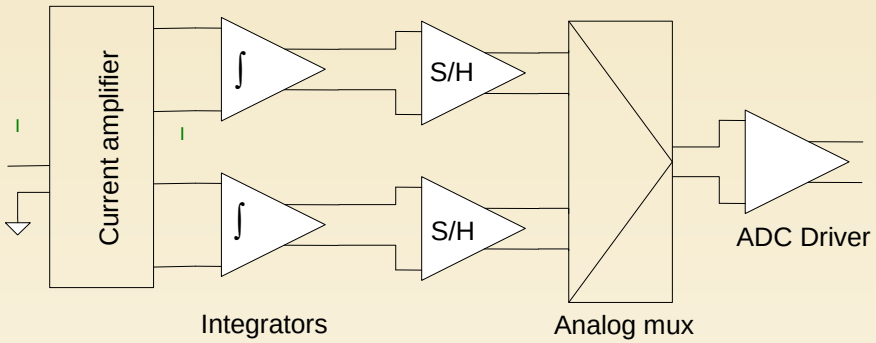
MIP spectrum measured with Beetle ASIC : S/N ~30.



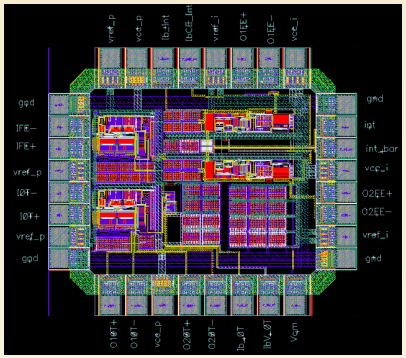
Radiation hardness for 10^{10} neutron/cm^2 ? under study.…

Calorimeter upgrade.

- The HV (and PMT gain) has to be decreased by a factor 5 to avoid premature ageing.
  - ->the preamplifier input equivalent noise must be decreased accordingly.
- A new frontend asic is being designed.
  - The signal is alternated every 25 ns between two integrators. The non-ative integrator is reset.

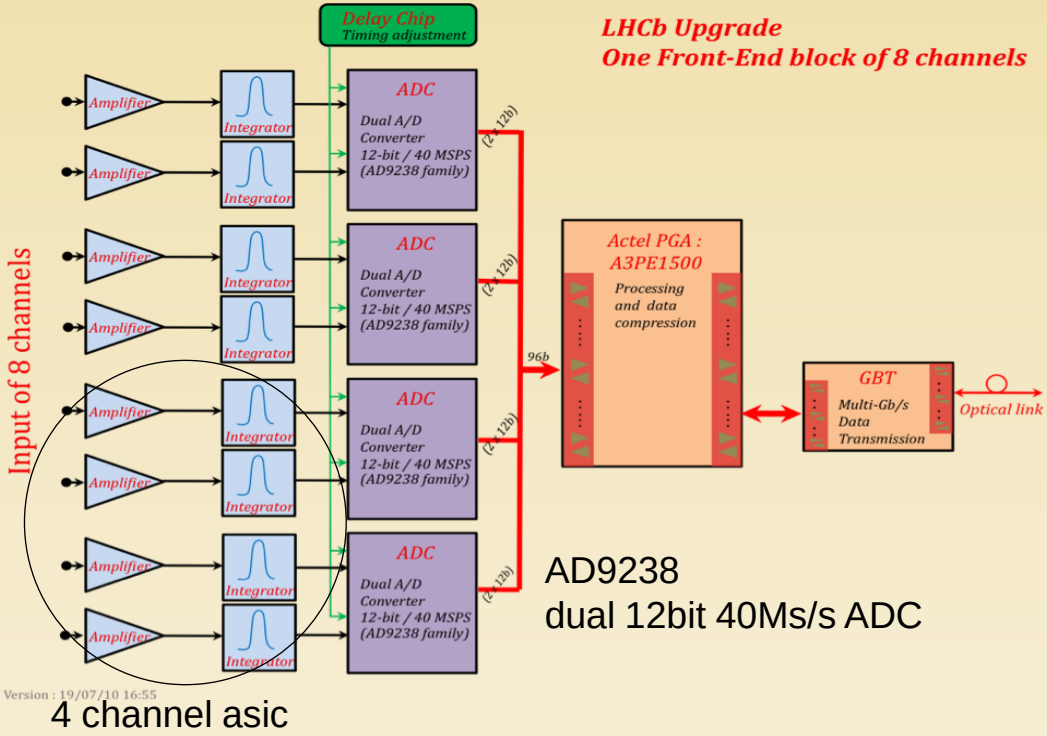


A first prototype of preamplifier and switched integrators has been designed and submitted in AMS 0.35 um SiGe BiCMOS.



Calorimeter upgrade.

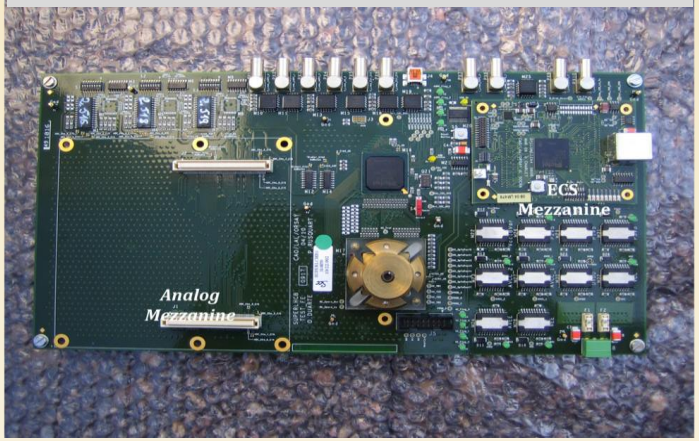
- New front end cards : 32 PMT signals
  - Extensive use of FPGA's (AX and APA) for data compression, trigger and ECS



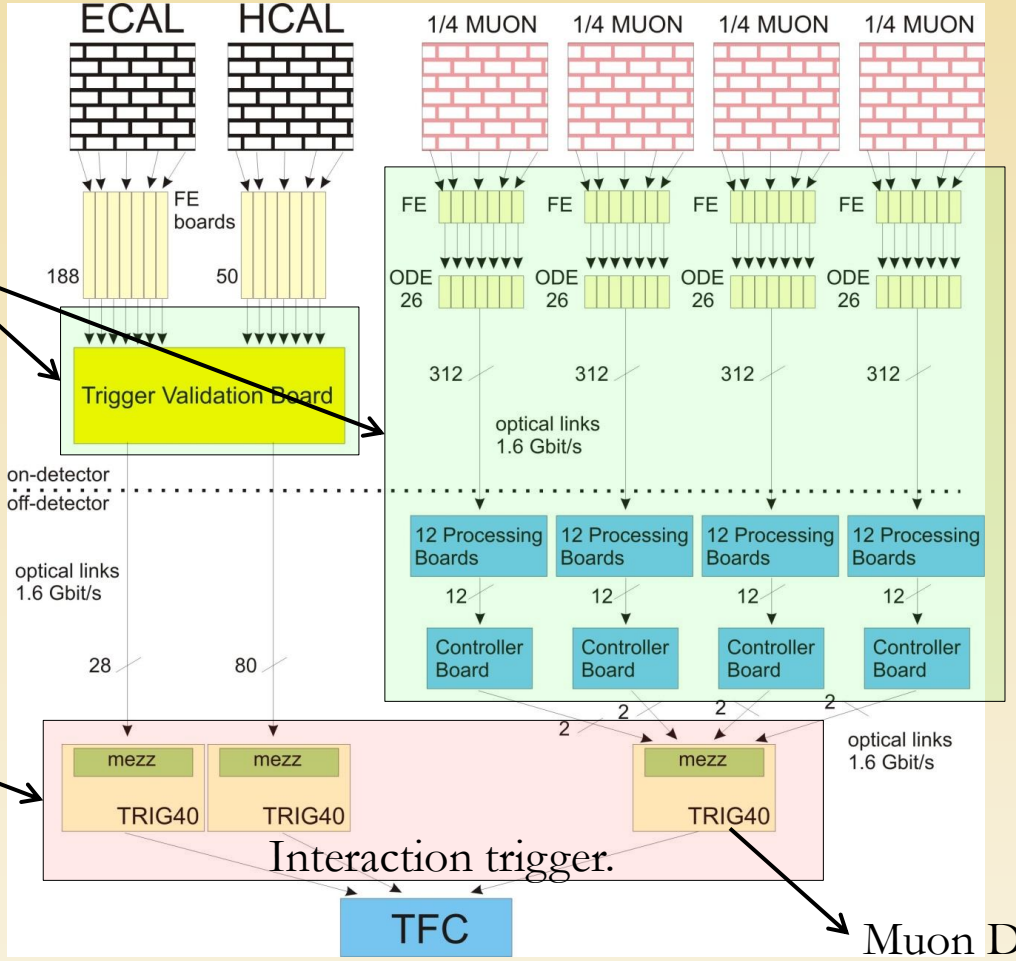
4 channel asic

AD9238
dual 12bit 40Ms/s ADC

Prototype of digital electronics



Muon upgrade & Interaction trigger.



Existing boards.

New 'interface' boards.

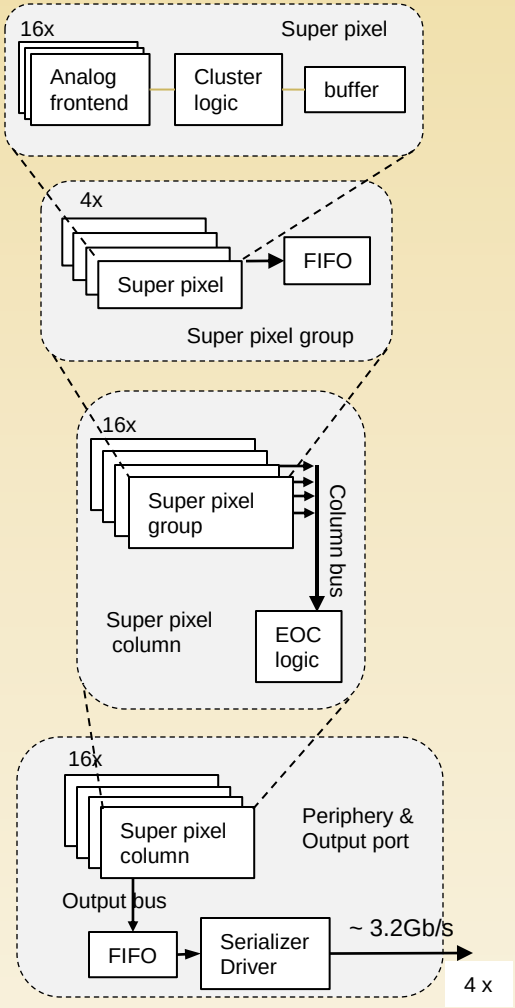
Muon DAQ path.

Summary.

- LHCb has a firm plan for its upgrade in 2016.
- No major detector changes needed, except VELO and RICH.
- All front-end electronics must be adapted or redesigned for 40 MHz readout and zero suppression.
- The subdetectors electronic developments are well underway.
- Extensive use of radiation tolerant FPGA's to avoid ASIC design where possible.

Backup slides

Pixel matrix readout architecture.



- Pixel matrix readout architecture
  - Internal bus speeds:
    - Column bus : 8bit@40MHz
    - Output bus : 16bit@320MHz
  - Total ASIC output : ~12.8 Gb/s.
  - Buffering in :
    - Super pixel : 2 clusters
    - Super pixel group FIFO : ~400 bit
    - Output FIFO: multi kbyte
- Simulation shows losses< 0.5% in highest occupancy conditions.