Design Studies of the ATLAS Muon Level-1 Trigger based on the MDT Detector for the LHC Upgrade

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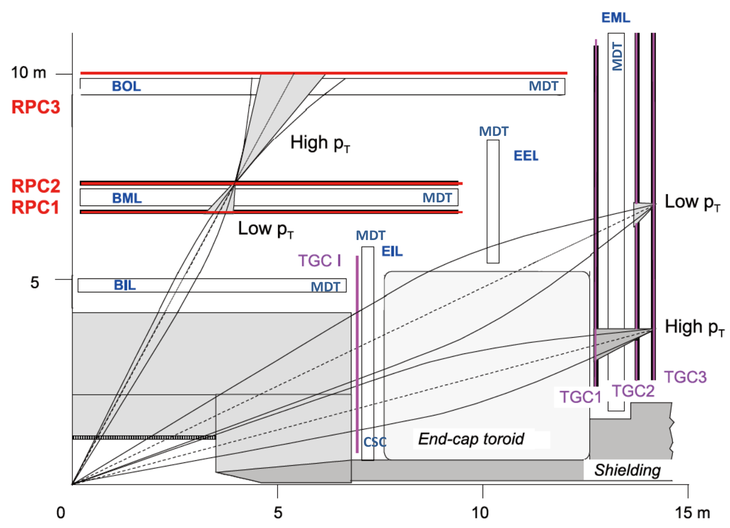
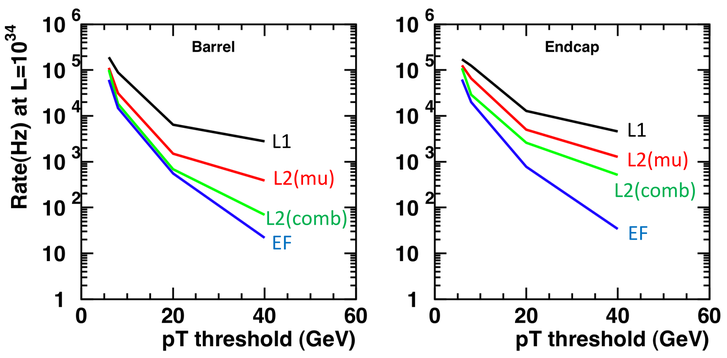
I. ATLAS Muon Level-1 Trigger Overview



The ATLAS muon spectrometer system consists of two types of chambers, which are for the purpose of either the precision momentum measurements of the tracks or the fast track finding for the Level-1 trigger. The monitored drift tube chambers (MDT, 30 mmϕ) and the cathode strip chambers (CSC) in the inner-most endcap region are used as precision-tracking chambers. The Resistive Plate Chambers (RPC) in the barrel and the Thin Gap Chambers (TGC) in the endcap region are dedicated for the triggering. The muon trigger system provides the flag of the muon track with the p_T thresholds in range 6-35 GeV.

II. Present Performance

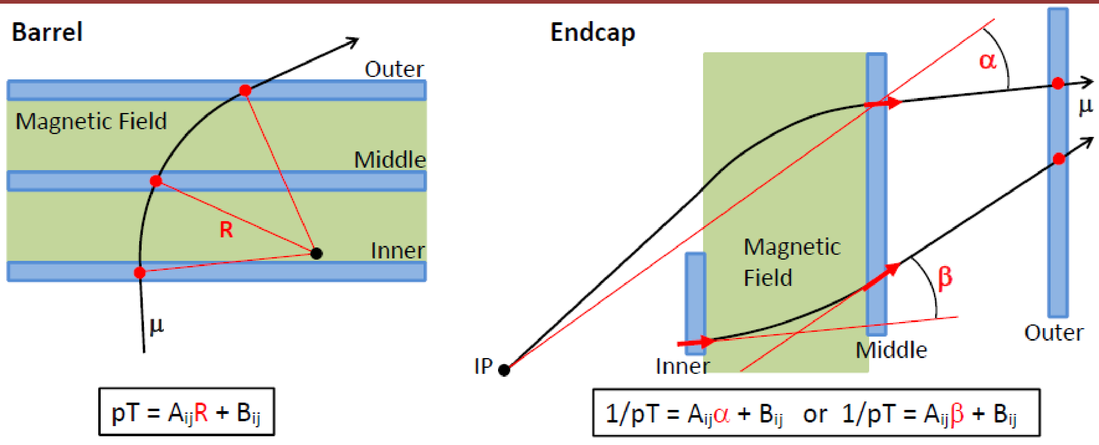


The figures show the simulated trigger rates of Level-1, Level-2 and Event Filter (EF) at L=10^{34} cm^{-2}s^{-1}.

Level-1 is performed by dedicated hardware logics of RPC and TGC.
L2(mu) is performed using MDT data.
L3(comb) is combination of trackings from the MDT and the Inner Detector.
EF is full tracking using all the data.

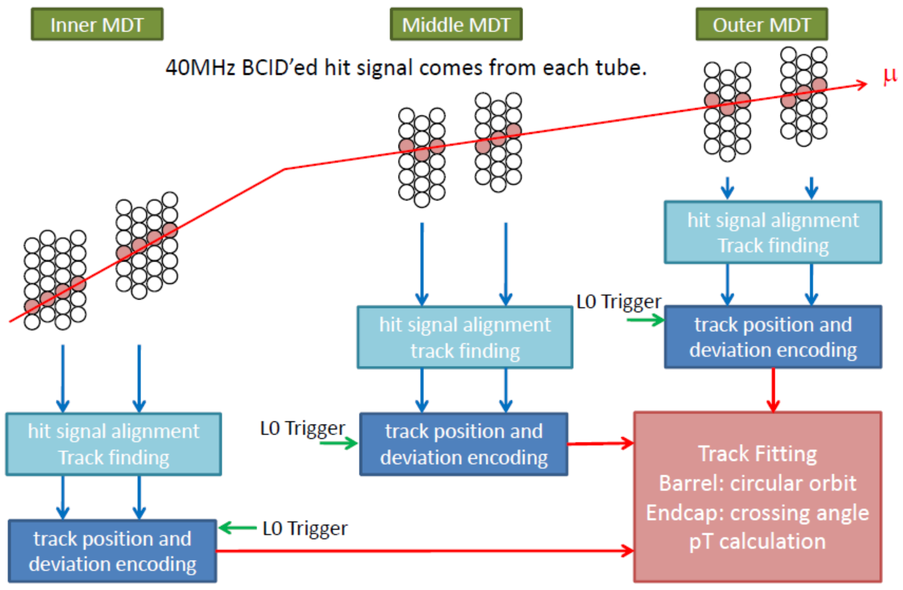
The trigger chambers and their trigger circuits satisfy the requirements of the L=10^{34} cm^{-2}s^{-1} operation. In the luminosity upgrade of the LHC, the improvement of the trigger performance would be foreseen for the potential requirement of the additional robustness against the background. According to the simulation studies of the Level-1 muon trigger rate, the sharpness of the p_T threshold curve is a dominant contributor of the rate. The long tail of the threshold curve towards the lower momentum region makes the background rate worse. The detectors having higher momentum resolution for the trigger will make the p_T threshold curve sharper. Additional detectors for the trigger in the inner most regions will also improve the Level-1 trigger rate.

III. Level-2 Algorithm



The replacement of the existing trigger chambers is not a realistic solution. The replacement of the existing trigger electronics does not improve the reduction of the muon trigger rate. If we could implement Level-2 (mu) algorithm using MDT data in Level-1 hardware logic, a factor of ~ 5 reduction for the trigger rate can be expected. Figures show the algorithm of the Level-2 muon tracking (software code "muFast"). The straight-line track fit is made in each MDT station (Inner, Middle and Outer). In the barrel, the hit position at the center of each station is derived. The fitting of the circular orbit is made from three hit positions and then its radius R gives the p_T momentum. In the endcap, the crossing angle α between the track slope measured in Middle and the infinite momentum track from the IP, or angle difference β between track slopes in Inner and Middle are measured.

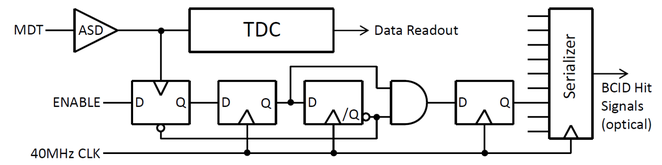
IV. MDT Based Level-1 Trigger Overview

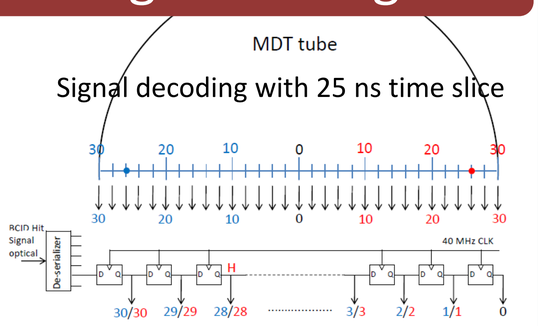


The signals from all the MDT tubes are BCID'ed with 40 MHz LHC clock and sent to the counting room. The straight-line track finding in each MDT station is made in parallel. The outputs from the finding are information about the track position and its deviation from the the infinite p_T track. The Level-0 signals from TGC and RPC will assist the track finding. The track information from each stations is combined and the p_T momentum is calculated.

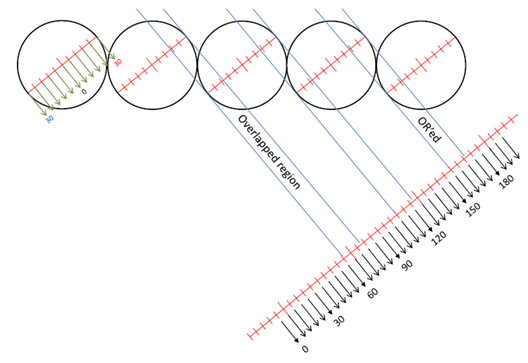
V. Front-end and Time/Spatial-aligned hit signals

Leading edge detection and BCID circuits in front-end





Spatial-aligned hit signals at 40° incidence

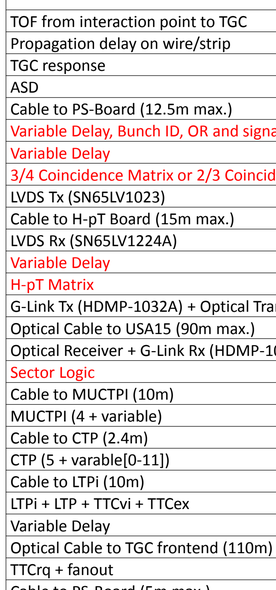


Leading edges of the hit signals from the ASD's are detected in each bunch (25 nsec), which corresponds to 0.5 mm spatial resolution. The BCID hit signals are serialized and transmitted to the counting room via high speed optical links. Each MDT tube has a 31-stage shift register, which decodes the BCID hit signal to Time/Spatial-aligned hit signals (25 ns timing and 0.5mm spatial-aligned). One BCID hit signal is converted to 61 hit signals [30,29,28,,1,0,1,,28,29,30] . A "hit signal" is shifted from 30/30 to 0 at 40MHz. One of colors (blue or red) is a true hit and the other shows a ghost hit. Decoded hit signals from each layer are projectively aligned in accordance with the expected incidence angle. Hit signals from the overlapped region of neighboring tubes are OR'ed.

VI. Station (6/8-layer) Coincidence Logic

Aligned hit signals from each layer (1,2,3,4 and 5,6,7,8-layer) : 0.5 mm step

0 1 2 3 4 5 ..... n n+1 n+2 n+3 n+4 n+5 Level-0



Aligned hit signals from each layer are fad to the track finding block. The p_T threshold is larger than 20 GeV.

Inner layers
The expected track deviations from infinite p_T muons is less than ±1° , so that one can restrict the track finding window within very narrow area. 3-out-of-4 coincidence is made in each super-layers individually. Information of position and deviation from both super-layers are combined.

Middle/Outer layers
Make the track finding from aligned hit signals of all the 6 layers. The expected track deviation is less than ±2.5°, the track finding window is expanding in very wide area. The algorithm for the track finding is being studied.

The Level-0 trigger signal from TGC/RPC assists the track finding and the BCID. The track information is sent to the next block, where p_T values are derived. The Algorithm based on LUT's is envisaged.

Track position/deviation | Track position/deviation | Track position/deviation

VII. Latency Estimation (<3.2 μsec)

Present TGC Level-1 Trigger

	nsec	CLK	Total CLK
TOF from interaction point to TGC	65	2.5	2.5
Propagation delay on wire/strip	15	1	3.5
TGC response	25	1	4.5
ASD	10	0.5	5
Cable to PS-Board (12.5m max.)		2.5	7.5
Variable Delay, Bunch ID, OR and signal routing		2	9.5
Variable Delay		1	10.5
3/4 Coincidence Matrix or 2/3 Coincidence Logic		2	12.5
LVDS Tx (SN65LV1023)		1	13.5
Cable to H-pT Board (15m max.)		3	16.5
LVDS Rx (SN65LV1224A)		2	18.5
Variable Delay		1	19.5
H-pT Matrix		2	21.5
G-Link Tx (HDMP-1032A) + Optical Transmitter		1.5	23
Optical Cable to USA15 (90m max.)		18	41
Optical Receiver + G-Link Rx (HDMP-1034A)		2.5	43.5
Sector Logic		7	50.5
Cable to MUCTPI (10m)		2	52.5
MUCTPI (4 + variable)		11	63.5
Cable to CTP (2.4m)		0.5	64
CTP (5 + varable[0-11])		6	70
Cable to LTPi (10m)		2	72
LTPi + LTP + TTCvi + TTCex		2	74
Variable Delay		2	76
Optical Cable to TGC frontend (110m)		22	98
TTCrq + fanout		3	101
Cable to PS-Board (5m max.)		1	102
			2.55μsec

MDT Muon Track Trigger

	nsec	CLK	Total CLK
TOF from interaction point to TGC	65	2.5	2.5
Propagation delay along wire	30	1.5	4
MDT drift time (0 - 700 ns)		28	32
ASD	10	1	33
Bunch ID		2	35
Serializer (TLK2501 @ 80MHz) + Optical Tx		2	37
Optical Fibre Cable (90m)		18	55
Optical Rx + De-serializer (TLK2501 @ 80MHz)		3	58
Shift Register (28-steps, 0 - 700 ns)		0	58
coincidence		1	59
track find		1	60
encoding		1	61
track fitting		2	63
pT calculation (LUT)		2	65
pT encoding		1	**66**
Cable to MUCTPI (10m)		2	68
MUCTPI		11	79
Cable to CTP (2.4m)		0.5	79.5
CTP		6	85.5
Cable to LTPi (10m)		2	87.5
LTPi + LTP + TTCvi + TTCex		2	89.5
Variable Delay		2	91.5
Optical Cable		22	113.5
TTCrq + fanout		3	116.5
Cable to Frontend Electronics		1.5	118
			2.95μsec

VIII. Conclusion

The ATLAS muon Level-1 trigger based on the MDT signals is being studied for the LHC upgrade. We have started R&D works; simulation foreseeing the real hardware scheme.
- hardware oriented algorithm to be able to implemented in FPGA
  track finding and p_T calculation.
- fully synchronized logic with fixed latency (<3.2 μsec in total).
- Optimization of the algorithm to achieve enough performance.
  The tracking efficiency, efficiency holes and the probability of the wrong tacking are to be estimated by the simulation works using real data.

The latency of the MDT based trigger is estimated to be approximately 3 μsec.