Electronics and Mechanics for the Silicon Vertex Detector of the Belle II Experiment

Belle II

HEPHY Institute of High Energy Physics

ÖAW Austrian Academy of Sciences

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C. Irmler*, T. Bergauer, I. Gfall, M. Friedl, M. Valentan

HEPHY, Institute of High Energy Physics, Austrian Academy of Sciences, Vienna (Austria)

ABSTRACT

A major upgrade of the KEK-B factory (Tsukuba, Japan), aiming at a peak luminosity of 8 x 10^{35} $cm^{-2}s^{-1}$), which is 40 times the present value, is foreseen until 2013. Consequently an upgrade of the Belle detector and in particular its Silicon Vertex Detector (SVD) is required. We will introduce the concept and prototypes of the full readout chain of the Belle II SVD. Its APV25 based front-end utilizes the Origami chip-on-sensor concept, while the back-end VME system provides online data processing as well as hit time finding using FPGAs. Furthermore, the design of the double-sided silicon detectors and the mechanics will be discussed.

BELLE II SVD

Belle II silicon vertex detector

- Layers: 4 strip (layers 3 to 6), 2 DEPFET pixels (layers 1 + 2)
- Radii: 1.8 / 2.2 / 3.8 / 8 / 11.5 / 14 cm
- Sensors: 187 rectangular double-sided silicon strip detectors (DSSD), 41 trapezoidal DSSDs for the slanted forward part
- Active area: ~1.2 m^2, ~240 k strips
- Front-end chip: APV25
- Shaping time: 50 ns
- Cooling: CO_2 system (-20°C)

Belle II SVD layout (including 2 pixel layers)

APV25

APV25 front-end chip features

40 MHz operation (nominal)
128 channels
192 cell deep analog pipeline
50 ns shaping time (adjustable)
Modes: peak / deconvolution / multi-peak
0.25 μm CMOS process
Radiation tolerance >100 MRad
Low noise: 250 e + 36 e/pF

Simplified schematics of one (out of 128) channels of the APV25

SENSOR DESIGN

Belle II DSSD specification

The Belle II SVD will consist of three different types of double sided silicon strip detectors, two with rectangular shape for the cylindrical barrel part and one trapezoidal type for the slanted forward region. In order to reduce the number of required sensors and thus readout channels, all types will be made from 6" wafers. Prototypes of the rectangular sensor have been produced by Hamamatsu Photonics (HPK), the Japanese company that also provided the DSSDs of the currently installed SVD. Samples of the trapezoidal type were ordered from Micron Semiconductor (UK). First samples of both designs were recently delivered. Characterization and intensive testing has already been started and some of the sensors will be used to build prototype modules.

	Barrel sensors		Forward sensors
Layer	3	4 to 6	4 to 6
Shape	rectangular		trapezoidal
# strips p-side	768	768	786
# strips n-side	768	512	512
# intermeditate strips p-side	767	767	767
# intermeditate strips n-side	767	511	511
Pitch p-side	50 µm	75 µm	75 … 50 µm
Pitch n-side	160 µm	240 µm	240 µm
Area (total)	5048.90 mm^2	7442.85 mm^2	6382.6 mm^2
Area (active)	4737.80 mm^2 (93.8%)	7029.88 mm^2 (94.5%)	5890 mm^2 (92.3%)
Base material	Si n-type 8 kΩcm		
Full depletion voltage (FD)	~ 60V (<120V)		40 V (typ.), 70 V (max.)
Polysilicon resistor	4 MΩ (min.), 10 M Ω (typ.)		10 MΩ (min.), 15 ±5 MΩ (max.)

Specification of the three DSSD types

CV measurements of the first batch of rectangular HPK sensors for layer 4 to 6

Microscope image of a corner of the first trapezoidal sensor.

First prototype module with a trapezoidal sensor.

FRONT-END ELECTRONICS

Origami chip-on-sensor concept

Belle II will run at relatively low energies of 4 GeV and 7 GeV for e+ and e-, respectively. Hence, material budget has to be kept low to constrain multiple scattering. On the other hand, the APV25 chips needs to be placed as close as possible to the sensors strips to minimize noise.

The so-called Origami chip-on-sensor concept, where the APV25 chips, together with a 3-layer flexible hybrid circuit, sit on the top of the senor, fulfills both requirements. The strips on the top side of the sensor (n-side) are connected by a pitch adapter, which is made as a separate two-layer piece. The channels of the opposite side (p-side) are attached by small flexible fanouts wrapped around the edge of the sensor, hence the name Origami. Since the readout chips of both sides are arranged in a row, they can be cooled by a single thin pipe.

In the Belle II SVD the Origami concept will be used to read out the inner sensors of layer 3 to 5, while conventional hybrids, located outside the acceptance, are foreseen at the edge sensors.

a) Top view:

b) Side view (cross section):

Top and side views of the Origami chip-on-sensor conept for a 6" DSSD. Only the fraction of the hybrid containing the readout chips is depicted. Depending on the location in the Belle II SVD, the flex circuit is extended either to the left or the right end of the ladder, where connectors are located outside the acceptance.

MECHANICS

Mechanical support structure

The sensors are arranged on ladders, which are cylindrically mounted on endrings. Each ladder is supported by two carbon fiber reinforced plastic sandwich ribs, in order to achieve lowest possible material budget at high mechanical strength. The sandwich consists of a 3 mm thick Airex (low mass rigid foam) core, reinforced by a 64 μm unidirectional carbon fiber layer on each side. The stability of the ribs results from the combination of core thickness and fiber strength. It has been proven by a finite element calculation for the outermost ladder (layer 6), which has a length of 645 mm. First prototypes of the ribs are already available and will soon be used to build a mockup.

3D rendering of the Belle II SVD

Top and bottom view of the ladder of layer 6. It consists of four rectangular and one trapezoidal (slanted) DSSD

ORIGAMI MODULE ASSEMBLY

Assembly of an Origami module

Aligning pitch adapters (PA1, PA2) to sensor strips on jig1

Lift up PA1 and PA2 using vacuum chucks

Apply glue and place back onto sensor

Wire bonding between PAs and p-side strips after curing of glue

Align and fix CF ribs on jig2

Apply glue on mountpoint of ribs

Put ribs together with jig2 onto jig1 and flip the module

The module is now ready for processing of the n-side (top)

Attaching APV25 chips (gluing, wire bonding)

Align hybrid to sensor and lift up using jig3

Apply glue onto hybrid and put it back onto sensor

After curing of glue the module is ready for wire bonding between integrated pitch adapter (PA0) and n-side strips

After wire bonding of n-side strips, the pitch atapters PA1 and PA2 are bent around the edge of the sensor, aligned to the APV chips and glued onto the hybrid, using a customized micro-positioner tool.

Wire bonding between PAs and APV chips

Final module is lifted and put into a frame for beam test.

Bottom view (p-side) of the final module

Top view (n-side) of the final module

BACK-END ELECTRONICS

Readout chain

The readout chain consists of an APV25 based front-end, connected to a juction box, which is located inside the detector, but outside the acceptance of the SVD. Its purpose is to avoid overlong, statically routed cables between front-end and back-end electronics, which are about 12 m apart. The box further contains radiation-hard voltage regulators to supply the front-end hybrids and protect them from transient overvoltages.

Schematic view of the Belle II SVD readout chain

The **FADC+PROC** is a 9U VME board with 24 input channels used to digitize and process the data of the APV25 chips. It further contains level translation from the bias voltage down to ground-bound low voltages for both analog and digital signals, respectively. The core functions of data processing are implemented in FPGAs and thus can easily be adapted by modifying the firmware. A dedicated data processing chain is forseen for each input, performing APV25 header detection, strip reordering, pedestal subtraction, a two-pass common mode correction, zero suppression and hit time reconstruction. Finally, position, pulse height and timing information of a hit are encoded in a single 32 bit wide word and transmitted to the global data aquisition system by an optical data link.

Thanks to the pipelined design with several FIFOs and a 64 bit wide local bus, data can be processed continously as long as they are fetched by the downstream DAQ system without congestion. The acceptable trigger rate is about 50 kHz, limited only by the time needed to read out the samples from the APV25 chips.

Prototypes of the existing repeater (REBO) and FADC boards and a sketch of the future composite FADC+PROC module (9U VME) with integrated voltage level translation.

In the existing prototype of the back-end electronics, the level translation part is implemented as a separate repeater board (REBO), to be mounted close to the front-end. However, there are space and radiation issues in the Belle II front-end. The differential APV output has been proven to be strong enough to drive cables with a length of 12 m. Hence, level translation can be done outside the detector and thus the REBO part can be added onto the future FADC+PROC module, which will be located on top of the detector.

* Email: christian.irmler@oeaw.ac.at