

Electronics and Mechanics for the Silicon Vertex Detector of the Belle II Experiment



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A major upgrade of the KEK-B factory (Tsukuba, Japan), aiming at a peak luminosity of 8 x 10³⁵ cm⁻²s⁻¹), which is 40 times the present value, is foreseen until 2013. Consequently an upgrade of the Belle detector and in particular its

Silicon Vertex Detector (SVD) is required. We will introduce the concept and prototypes of the full readout chain of the Belle II SVD. Its APV25 based frontend utilizes the Origami chip-on-sensor concept, while the back-end VME system provides online data processing as well as hit time finding using FPGAs. Furthermore, the design of the double-sided silicon detectors and the mechanics will be discussed.

Belle II silicon vertex detector

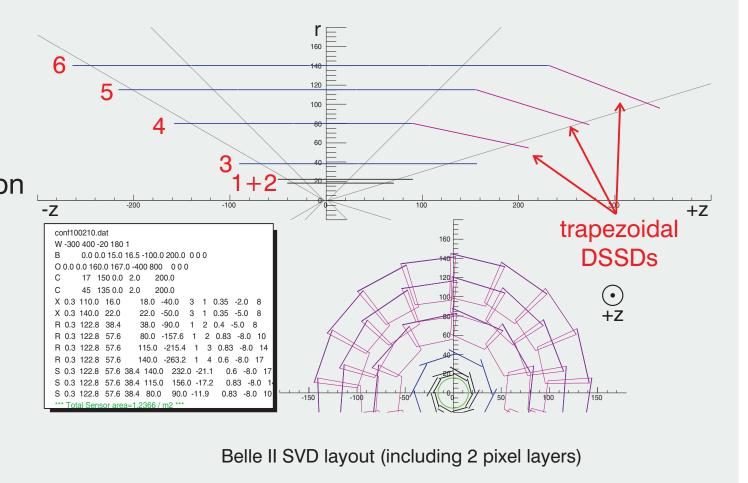
4 strip (layers 3 to 6) Layers: 2 DEPFET pixels (layers 1 + 2) Radii: 1.8 / 2.2 / 3.8 / 8 / 11.5 / 14 cm

187 rectangular double-sided silicon strip detectors (DSSD) 41 trapezoidal DSSDs for the slanted forward part

 \sim 1.2 m², \sim 240 k strips Active area:

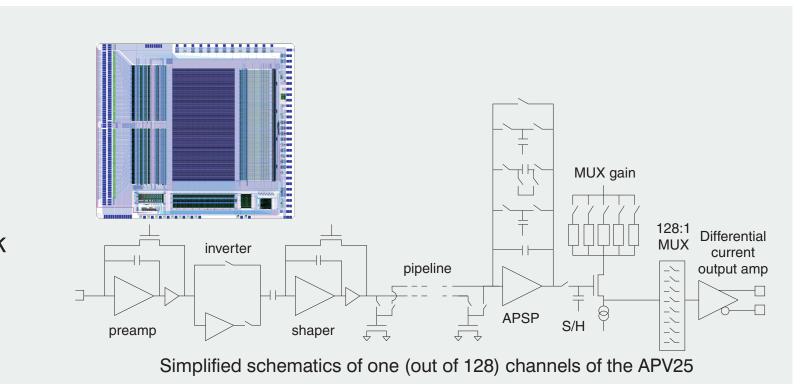
Front-end chip: APV25 Shaping time: 50 ns

Cooling: CO₂ system (-20°C)



APV25 front-end chip features

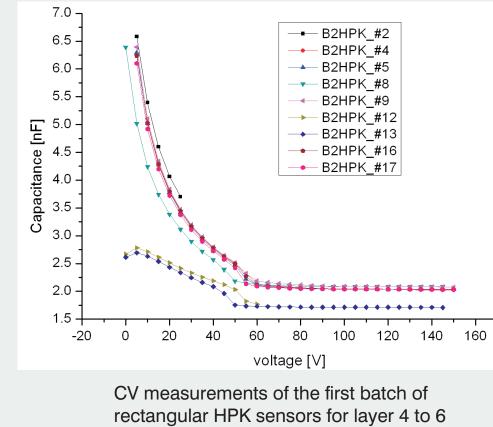
40 MHz operation (nominal) 128 channels 192 cell deep analog pipeline 50 ns shaping time (adjustable) Modes: peak / deconvolution / multi-peak $0.25 \,\mu m$ CMOS process Radiation tolerance > 100 MRad Low noise: 250 e + 36 e/pF



Belle II DSSD specification

The Belle II SVD will consist of three different types of double sided silicon strip detectors, two with rectangular shape for the cylindrical barrel part and one tarpezoidal type for the slanted forward region. In order to reduce the number of required sensors and thus readout channels, all types will be made from 6" wafers. Prototypes of the rectangular sensor have been produced by Hamamatsu Photonics (HPK), the Japanese company that also provided the DSSDs of the currently installed SVD. Samples of the trapezoidal type were ordered from Micron Semiconductor (UK). First samples of both designs were recently delivered. Characterization and intensive testing has already been started and some of the sensors will be used to build prototype modules.

| | Barrel sensors | | Forward |
|-------------------------------|---------------------------------|---------------------------------|---|
| | | | sensors |
| Layer | 3 | 4 to 6 | 4 to 6 |
| Shape | rectangular | | trapezoidal |
| # strips p-side | 768 | 768 | 786 |
| # strips n-side | 768 | 512 | 512 |
| # intermeditate strips p-side | 767 | 767 | 767 |
| # intermeditate strips n-side | 767 | 511 | 511 |
| Pitch p-side | 50 μm | 75 µm | 75 50 μm |
| Pitch n-side | 160 µm | 240 µm | 240 µm |
| Area (total) | 5048.90 mm ² | 7442.85 mm ² | 6382.6 mm ² |
| Area (active) | 4737.80 mm ² (93.8%) | 7029.88 mm ² (94.5%) | 5890 mm ² (92.3%) |
| Base material | Si n-type 8 kΩcm | | |
| Full depletion voltage (FD) | ~ 60V (<120V) | | 40 V (typ.), 70 V (max.) |
| Polysilicon resistor | 4 MΩ (min.), 10 M Ω (typ.) | | 10 M Ω (min.), 15 ±5 M Ω (max.) |



First prototype module with

a trapezoidal sensor.

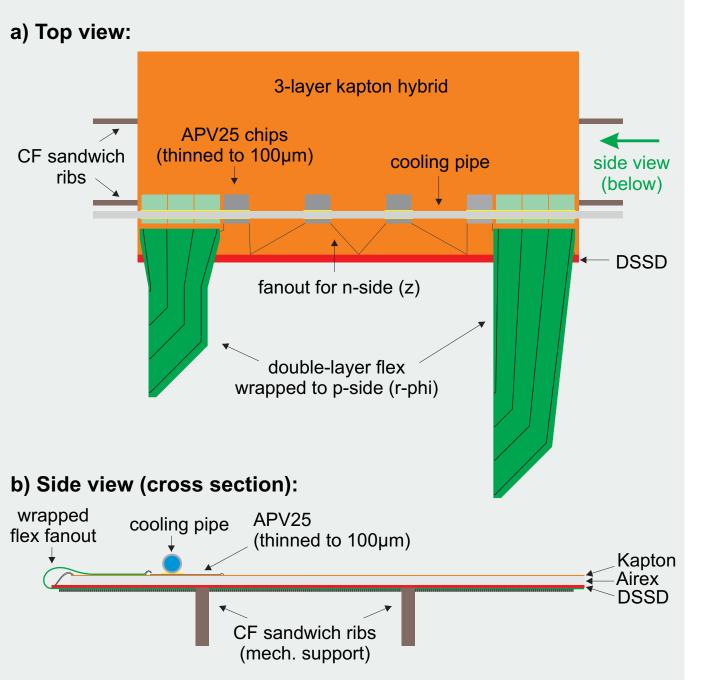
Specification of the three DSSD types

Origami chip-on-sensor concept

Belle II will run at relatively low energies of 4 GeV and 7 GeV for e+ and e-, respectively. Hence, material budget has to be kept low to constrain multiple scattering. On the other hand, the APV25 chips needs to be placed as close as possible to the sensors strips to minimize noise.

The so-called Origami chip-on-sensor concept, where the APV25 chips, together with a 3-layer flexible hybrid circuit, sit on the top of the senor, fulfills both requirements. The strips on the top side of the sensor (n-side) are connected by a pitch adapter, which is made as a separate twolayer piece. The channels of the opposite side (pside) are attached by small flexible fanouts b) Side view (cross section): wrapped around the edge of the sensor, hence the name Origami. Since the readout chips of both sides are arranged in a row, they can be cooled by a single thin pipe.

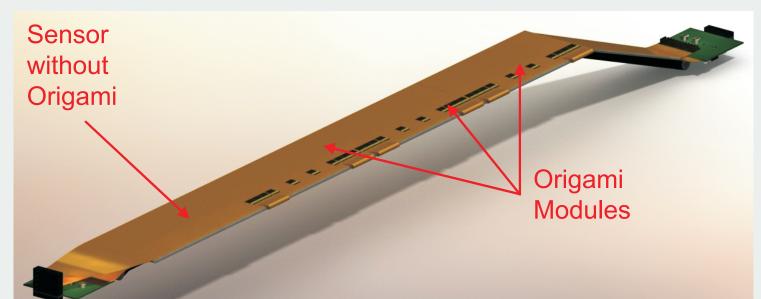
In the Belle II SVD the Origami concept will be used to read out the inner sensors of layer 3 to 5, while conventional hybrids, located outside the acceptance, are foreseen at the edge sensors.

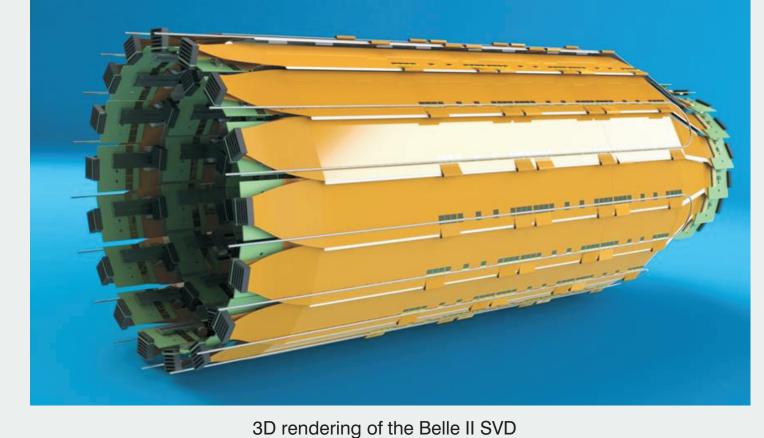


Top and side views of the Origami chip-on-sensor conept for a 6" DSSD. Only the fraction of the hybrid containing the readout chips is depicted. Depending on the location in the Belle II SVD, the flex circuit is extended either to the left or the right end of the ladder, where connectors are located outside the acceptance

Mechanical support structure

The sensors are arranged on ladders, which are cylindrically mounted on endrings. Each ladder is supported by two carbon fiber reinforced plastic sandwich ribs, in order to achieve lowest possible material budget at high mechanical strength. The sandwich consists of a 3 mm thick Airex (low mass rigid foam) core, reinforced by a 64 μ m unidirectional carbon fiber layer on each side. The stability of the ribs results from the combination of core thickness and fiber strength. It has been proven by a finite element calculation for the outermost ladder (layer 6), which has a length of 645 mm. First prototypes of the ribs are already available and will soon be used to build a mockup.





Origami Mount Structure **Hybrid Board** Sensor CF Ribs

Top and bottom view of the ladder of layer 6. It consists of four rectengular and one trapezoidal (slanted) DSSD

Assembly of an Origami module



MODULE A

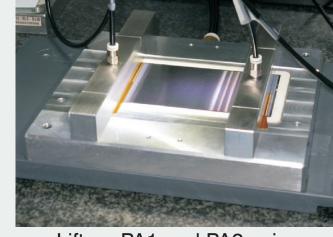
to sensor strips on jig1



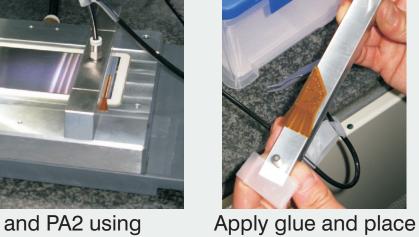




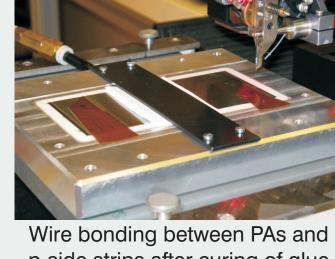
Align and fix CF ribs on jig2



Lift up PA1 and PA2 using vacuum chucks



back onto sensor



p-side strips after curing of glue





Apply glue on mountpoint of ribs



Put ribs together with jig2 onto jig1 and flip the module



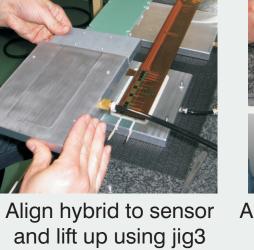
The module is now ready for processing of the n-side (top)

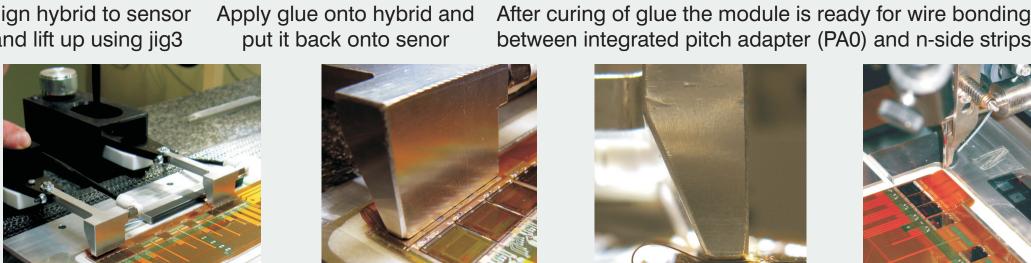
Wire bonding between PAs and APV chips

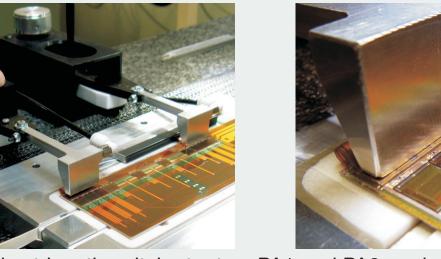
between integrated pitch adapter (PA0) and n-side strips

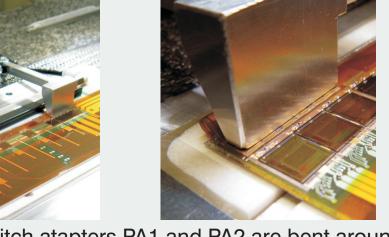


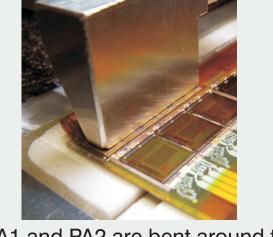
Attaching APV25 chips (gluing, wire bonding)

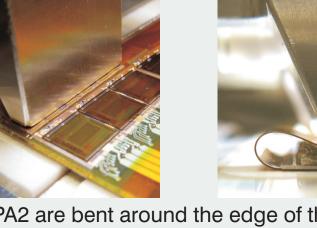


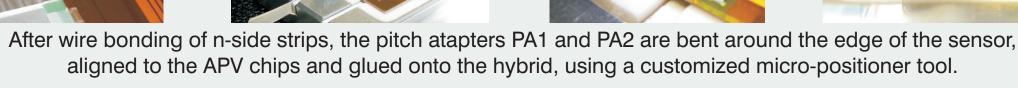


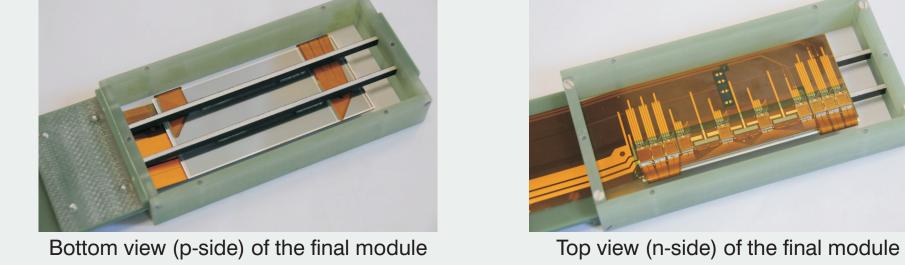






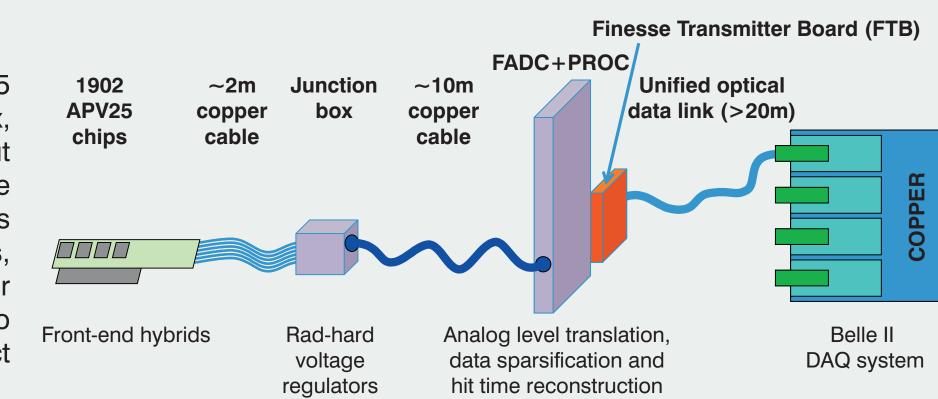






Readout chain

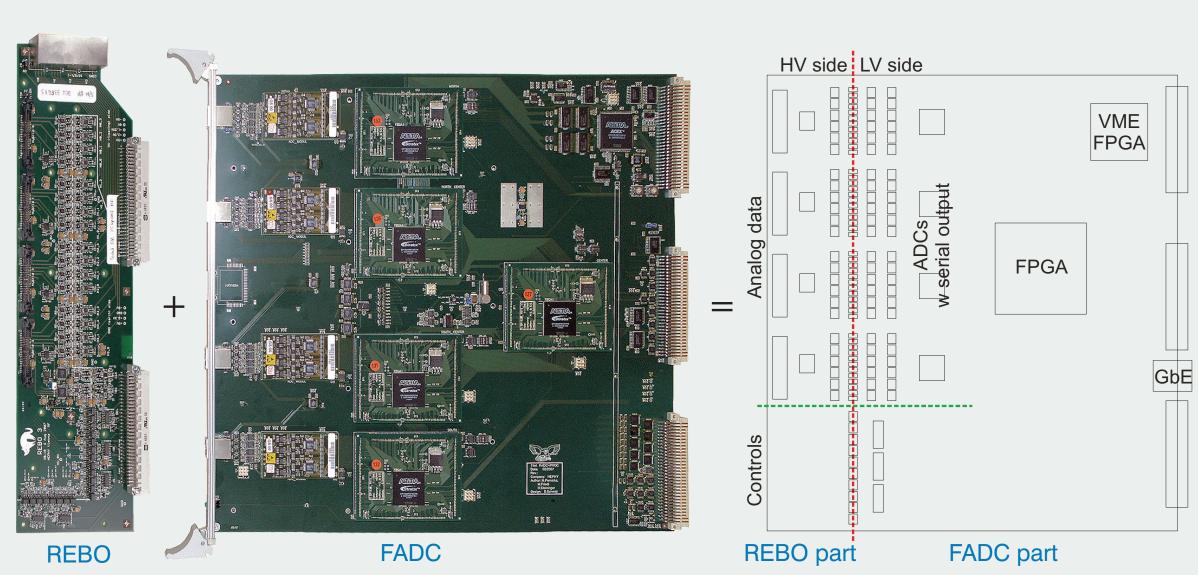
The readout chain consists of an APV25 based front-end, connected to a juction box, which is located inside the detector, but outside the aceptance of the SVD. Its purpose is to avoid overlong, statically routed cables between front-end and back-end electronics, which are about 12 m apart. The box further contains radiation-hard voltage regulators to supply the front-end hybrids and protect them from transient overvoltages.



Schematic view of the Belle II SVD readout chain

The FADC+PROC is a 9U VME board with 24 input channels used to digitize and process the data of the APV25 chips. It further contains level translation from the bias voltage down to ground-bound low voltages for both analog and digital signals, respectively. The core functions of data processing are implemented in FPGAs and thus can easily be adapted by modifying the firmware. A dedicated data processing chain is forseen for each input, performing APV25 header detection, strip reordering, pedestal subtraction, a two-pass common mode correction, zero suppression and hit time reconstruction. Finally, position, pulse height and timing information of a hit are encoded in a single 32 bit wide word and transmitted to the

global data aquisition system by an optical data link. Thanks to the pipelined design with several FIFOs and a 64 bit wide local bus, data can be processed continously as long as they are fetched by the downstream DAQ system without congestion. The acceptable trigger rate is about 50 kHz, limited only by the time needed to read out the samples from the APV25 chips.



Prototypes of the existing repeater (REBO) and FADC boards and a sketch of the future composite FADC+PROC module (9U VME) with integrated voltage level translation.

In the existing prototype of the back-end electronics, the level translation part is implemented as a separate repeater board (REBO), to be mounted close to the front-end. However, there are space and radiation issues in the Belle II front-end. The differential APV output has been proven to be strong enough to drive cables with a length of 12 m. Hence, level translation can be done outside the detector and thus the REBO part can be added onto the future FADC+PROC module, which will be located on top of the detector.

Final module is lifted and put into a frame for beam test.