A 4.9-GHz Low Power, Low Jitter, LC Phase Locked Loop

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Introduction

The upgrade from Large Hadron Collider (LHC) to super-LHC (sLHC) puts new challenges on the ATLAS Liquid Argon Calorimeter readout system. As a key part of the readout system, the optical data links must operate at the data rate of about 100 giga-bit per second (Gbps) per front–end board (FEB), 60 times higher than the present whereas power consumption of each FEB must be kept the same as the present. The serializers used in the present optical data link system cannot meet the upgrade requirements on data rate and power consumption. Due to the radiation tolerant requirement, no commercial serializer is available for the upgrade of the optical data links. A radiation tolerant, high speed, and low power serializer Application-Specific Integrated Circuit (ASIC) has to be developed for the upgrade of the optical data links.

We have successfully designed a 16:1 serializer ASIC operating at 5 Gbps with a ring oscillator based phase locked loop (PLL) [1]. Our next prototype aims at the data rate of 8 – 10 Gbps. Correspondingly, we have to develop a PLL operating at 4 – 5 GHz. The ring oscillator based PLL cannot be used due to its limits on speed, jitter, and power consumption.

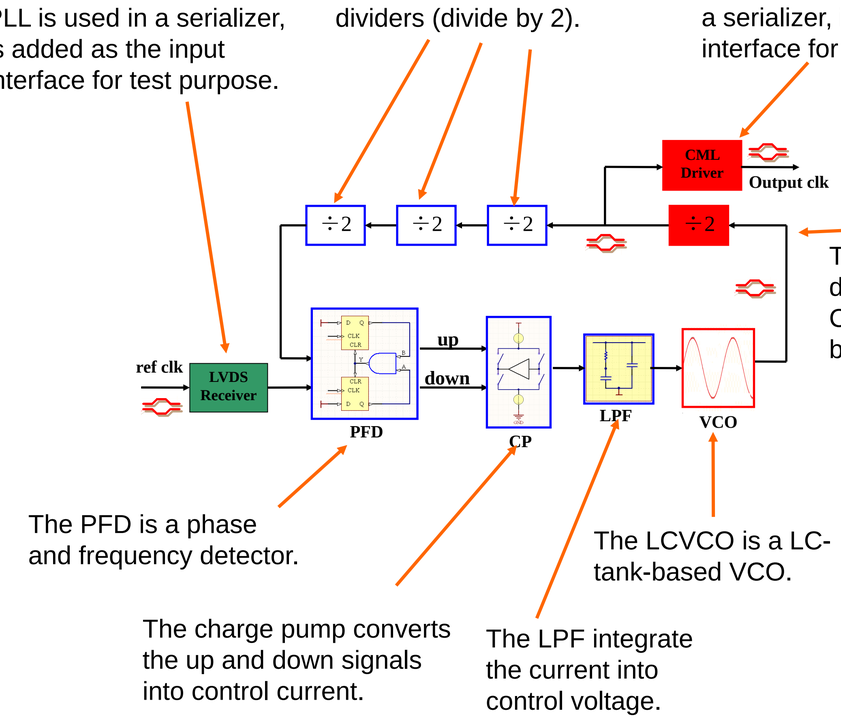
We present a high speed, low jitter, and low power LCPLL. The design goal is to operate in the 4 – 5 GHz range with low jitter and low power consumption, providing the clock for the future 8 –10 Gbps serializer [2]. We choose a commercial 0.25-μm SoS CMOS technology because of its high speed, low power, absence of radiation-induced latch-up, and availability of high quality analog devices like inductors. The PLL has been fabricated and tested. The design and test results are presented in this poster.

Design

An LVDS receiver, which will be removed when the PLL is used in a serializer, is added as the input interface for test purpose.

The last three stages of the divider chain are CMOS dividers (divide by 2).

A CML driver, which will be removed when the PLL is used in a serializer, is added as the output interface for test purpose.



The first stage of the divider chain is a CML divider (divide by 2).

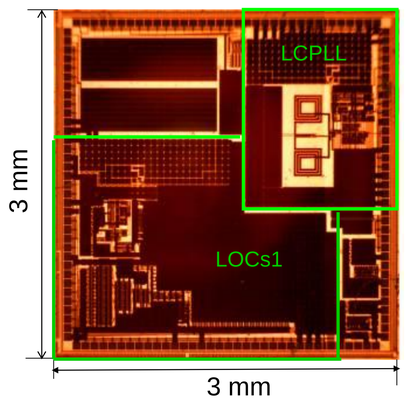
The PFD is a phase and frequency detector.

The charge pump converts the up and down signals into control current.

The LPF integrate the current into control voltage.

The LCVCO is a LC-tank-based VCO.

Micrograph

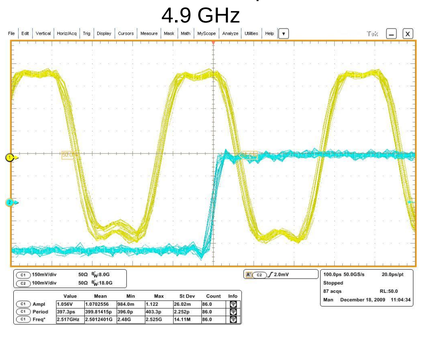


Simulated results

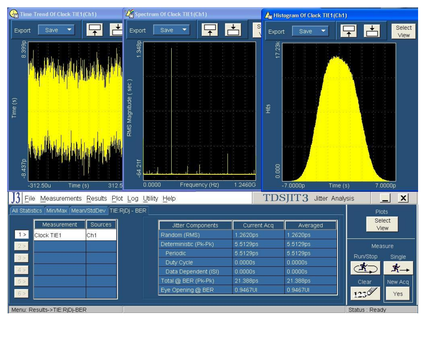
Tuning range (GHz)	3.8 – 5.1
Power consumption of core PLL (mW)	104
Random Jitter from VCO (RMS, ps)	< 1
Deterministic jitter (peak-peak, ps)	2
Acquisition time (μs)	9

Test Results

The output clock locks to its input clock when the PLL operates at 4.9 GHz



The jitter analysis at 4.9 GHz



Measured results at lower and upper tuning range

	lower limit				higher limit			
Board ID	1	2	3	4	1	2	3	4
VCO frequency (GHz)	4.752	4.616	4.480	4.744	4.984	5.008	4.968	4.992
input freq (MHz)	297.0	288.5	280.0	296.5	311.5	313.0	310.5	312.0
output freq (GHz)	2.38	2.29	2.24	2.37	2.50	2.51	2.484	2.50
Ampl (pos – neg) (V)	1.06	1.22	1.30	0.98	1.07	1.21	1.30	0.98
rise time (ps)		66.2	47.0	67.1		67.2	42.1	66.1
fall time (ps)		64.6	46.5	68.5		66.8	41.9	66.4
Random jitter RMS (ps)	1.28	2.49	2.05	1.81	1.26	1.06	1.08	1.83
Deterministic jitter (ps)	12.61	11.00	13.95	15.46	5.51	5.10	16.63	8.43

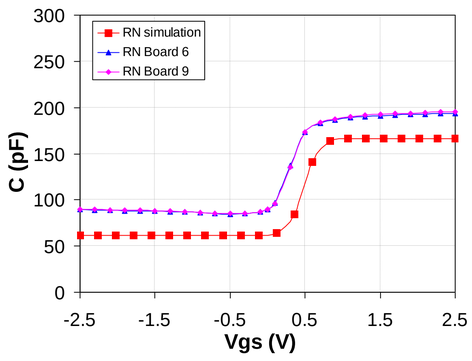
Measured results

- Tuning range: 4.7 to 5 GHz. Simulation: 3.79 to 5.01 GHz.
- Power consumption: 121 mW at 4.9 GHz. Compare: ring oscillator based PLL, 173 mW at 2.5 GHz
- Random jitter: 1 - 2.5 ps (RMS)
- Deterministic jitter: < 17 ps (pk-pk)
- A 200-MeV proton test was conducted in June 2010. Post-radiation measurements will be performed and compared with pre-radiation measurements when safety is allowed.

Narrow Tuning Range Investigation

Varactors

Measured and simulated capacitance-voltage curve of a varactor based on a RN MOSFET

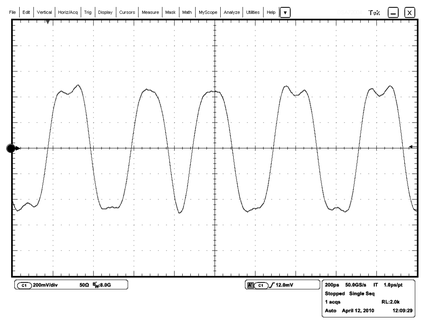


- A varactor is not a standard supported device in the technology we use.
- The varactor used in the design is a standard NMOSFET with its source and drain terminals connected together.
- Measured C-V curve of the varactors demonstrates that a MOSFET-based varactor behaves as it is expected though the measured values deviate from what are simulated. The deviation will be investigated.
- The measurement rules out that inaccuracy of varactor model causes the narrow tuning range.

The first stage of Divider

Measured Waveform of the Divider

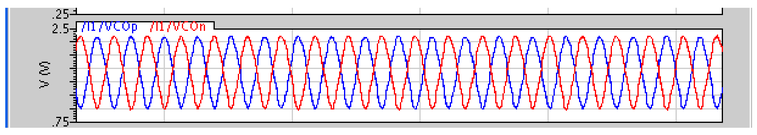
The output waveform exhibits an abnormal cycle when the control voltage (Vctrl) of the LCVCO is 1.5 V.



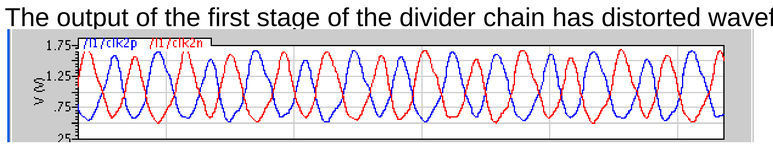
- **The failure mechanism is understood.** When the control voltage to the VCO decreases, the common mode voltage of VCO output increases. Consequently, the leakage current of CML latches in hold mode in the divider increases and causes the CML latches become unstable, resulting in spikes in the divider output.
- **This problem will be corrected in the next submission.**

Simulated Waveforms of the Divider

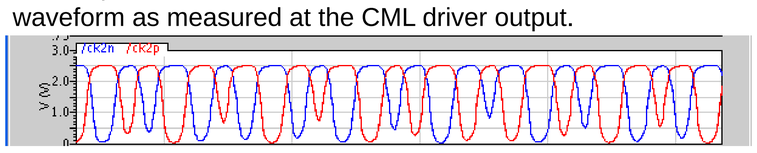
LCVCO output waveform is perfectly ok when Vctrl = 1.5 V.



The output of the first stage of the divider chain has distorted waveform.



The output of the CML to CMOS converter exhibits the same waveform as measured at the CML driver output.



Conclusion

An LC phase locked loop ASIC, fabricated in a commercial 0.25-μm Silicon-on-Sapphire CMOS technology, has been characterized in lab. Random jitter and deterministic jitter are less than 2.5 ps and 17 ps, respectively. The power consumption at 4.9 GHz is 121 mW. The measured tuning range, from 4.7 to 5.0 GHz, is narrower than the simulated values of from 3.8 to 5.0 GHz. The narrow tuning range has been investigated and traced to the first stage of the divider chain. This problem will be corrected in the next submission.

References

1. A 16:1 Serializer ASIC for Data Transmission at 5 Gbps, Datao Gong on behalf of the ATLAS Liquid Argon Calorimeter Group, presented at the topical workshop on electronics in particle physics (TWEPP), Aachen, Germany, Sept. 22, 2010.
2. The Design of a High Speed Low Power Phase Locked Loop, Tiankuan Liu et al, presented at the topical workshop on electronics in particle physics (TWEPP), Paris, France, Sept. 24, 2009.

Acknowledgments

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