Front end electronics for silicon strip detectors in 90nm CMOS technology; advantages and challenges

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Outline

- Motivations
- Consequences of technology scaling, advantages and drawbacks
- Methods to improve analogue performance
- Architecture of the front end channel
- Preliminary results from the prototype chip (16x preamplifier/shaper/comparator channels + analogue test channel)
- Conclusions

Motivation

- Can the performance (power vs. noise) of future readout chips be improved by using more advanced technology?
- Project funded by CERN/PH R&D money for LHC detectors upgrade

Setting the specifications

- Project focus on front end electronics for silicon strip detectors to be used at SLHC
- Relatively short strips (<5pF)
- Peaking time 22-25ns
- Low noise (<1000e-) compatible with heavily irradiated detectors
- Low power, low current consumption
- Radiation hardness

Technology scaling, consequences

- Higher transconductance ($K_{a\ NMOS}$ ~800 uA/V^2 *)
- Higher ft (peak ft 105GHz *)
- Degradation of transistor output conductance → lower intrinsic gain (K_V ~18 for transistors in weak inversion*)
- Lower voltage supply (1.2V *)

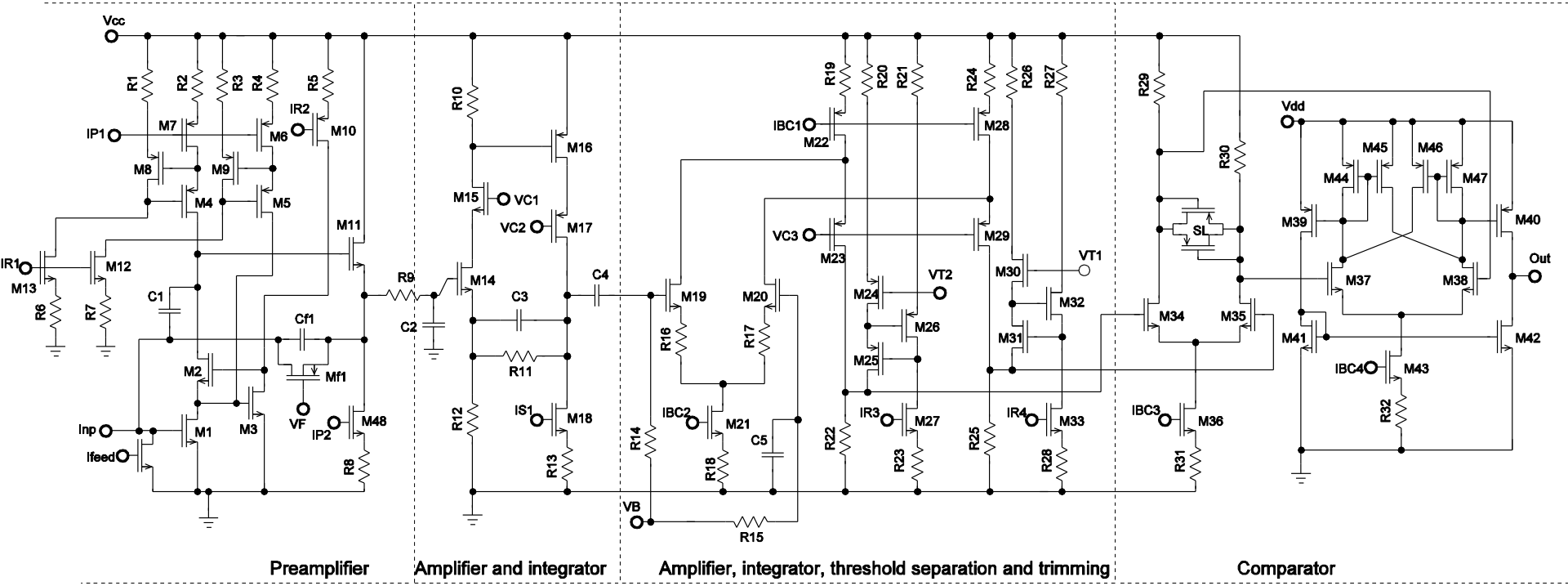
(*) data for 90nm CMOS process available at CERN

Preserving analog performance

- Low output conductance of single transistor impacting open loop gain and PSRR
  - Gain of single transistor ~18V/V – we need 70 to 80dB
  - For 90nm process the use of regulated cascode at the input stage and load can provide open loop gain in the range of 70dB
  - Avoiding source followers as a buffer stage (PSRR)
- Low voltage supply and use of regulated cascodes does not leave too much room for V_{ds} voltage
  - dynamic range limited (still OK for tracking applications)
  - all transistors in weak inversion (lower saturation voltage but potential problem with extra noise contribution from current sources in the input stage)

Architecture of the front end channel

Input transistor (NMOS 200/0.3) bias: 80 to 120uA
Current consumed by remaining stages: 80uA

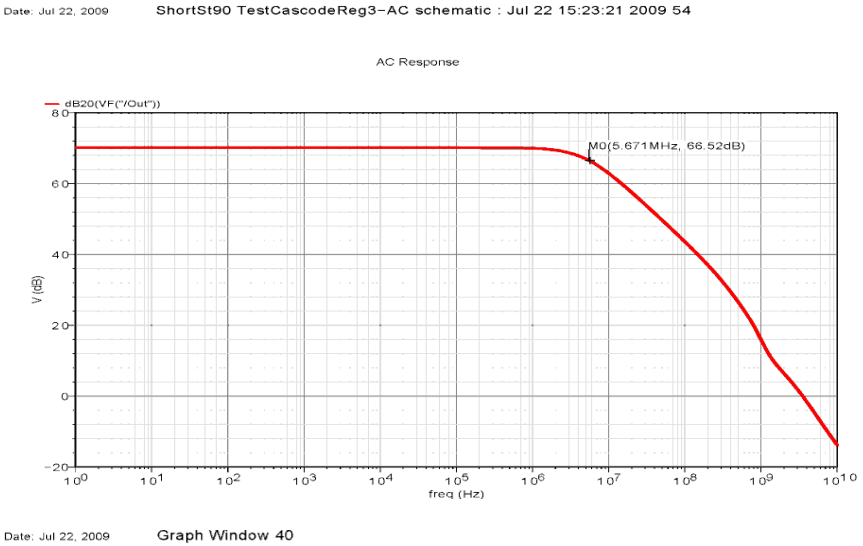


5.5mV/fC
T_{peak} 8ns

30mV/fC
T_{peak} 18ns

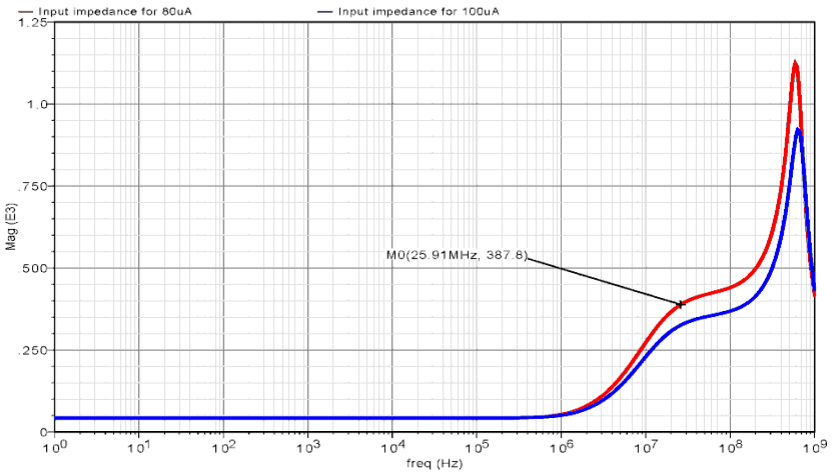
100mV/fC
T_{peak} 22ns

AC parameters of the input stage, simulation



Open loop gain 70dB

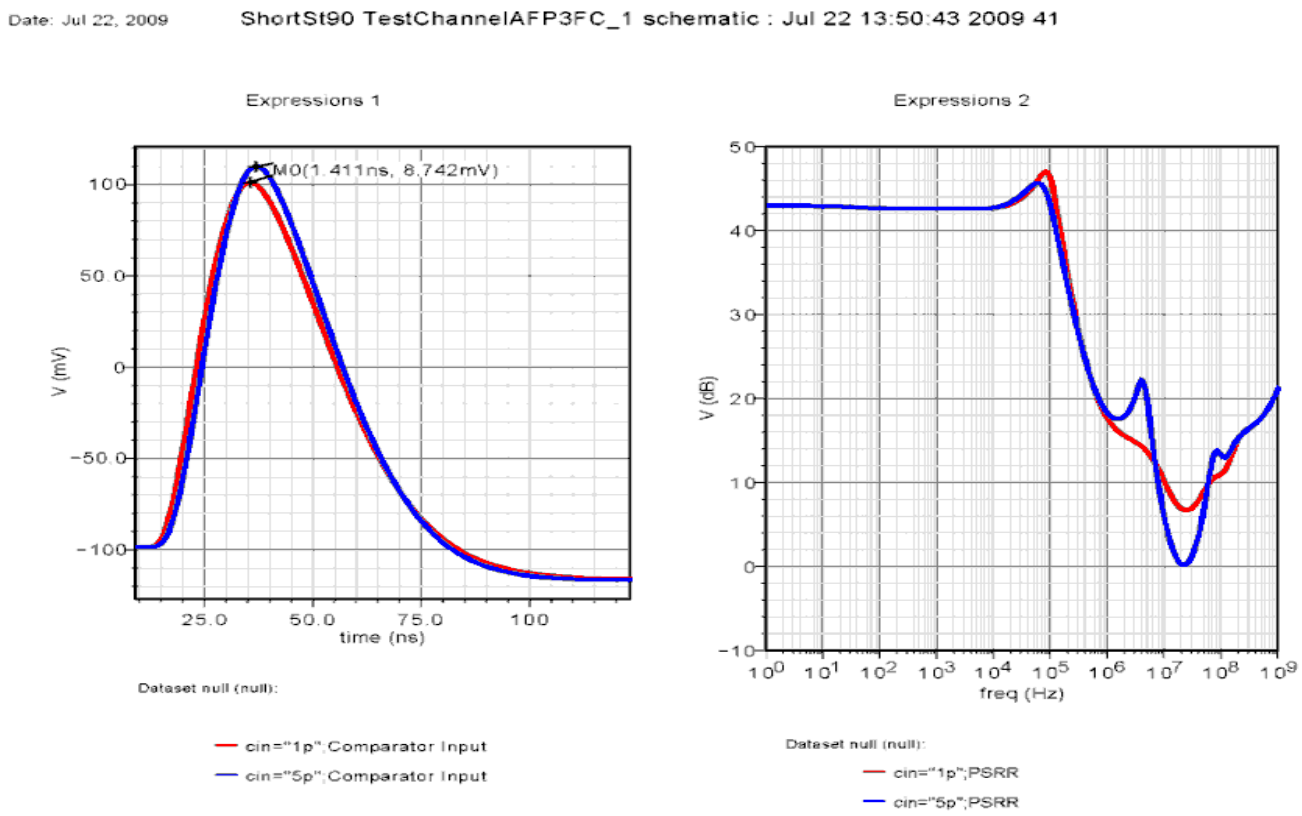
Gain Bandwidth Product 3.5GHz



Input impedance:

- 50 Ohm at low frequencies
- 250 Ohm at 10 MHz (100uA bias)

Analogue parameters of the input stage, simulation



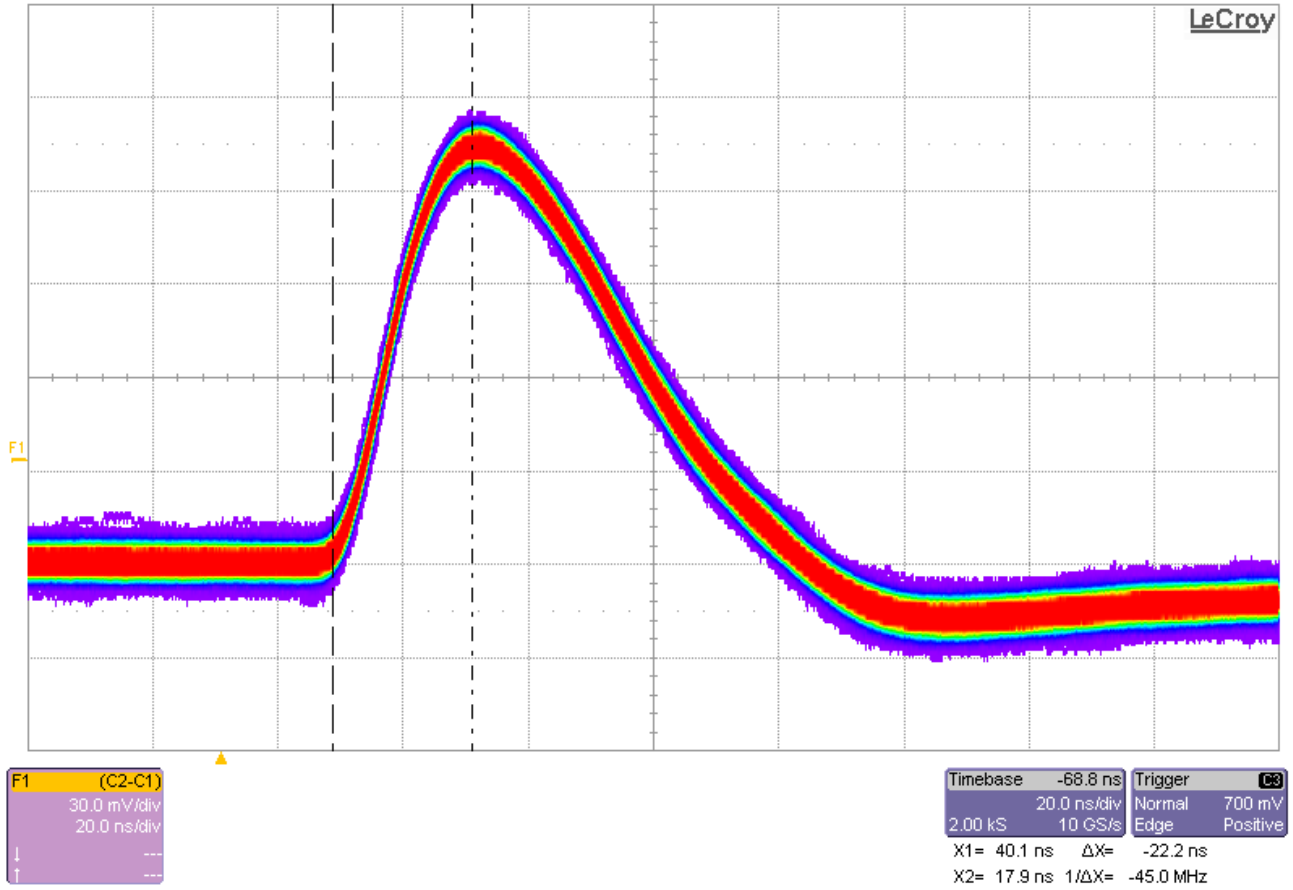
0.35ns/pF variation of peaking time vs. input capacitance

PSRR from 0.5dB to 8dB for input capacitances 5pF to 1pF

Results from the prototype chip

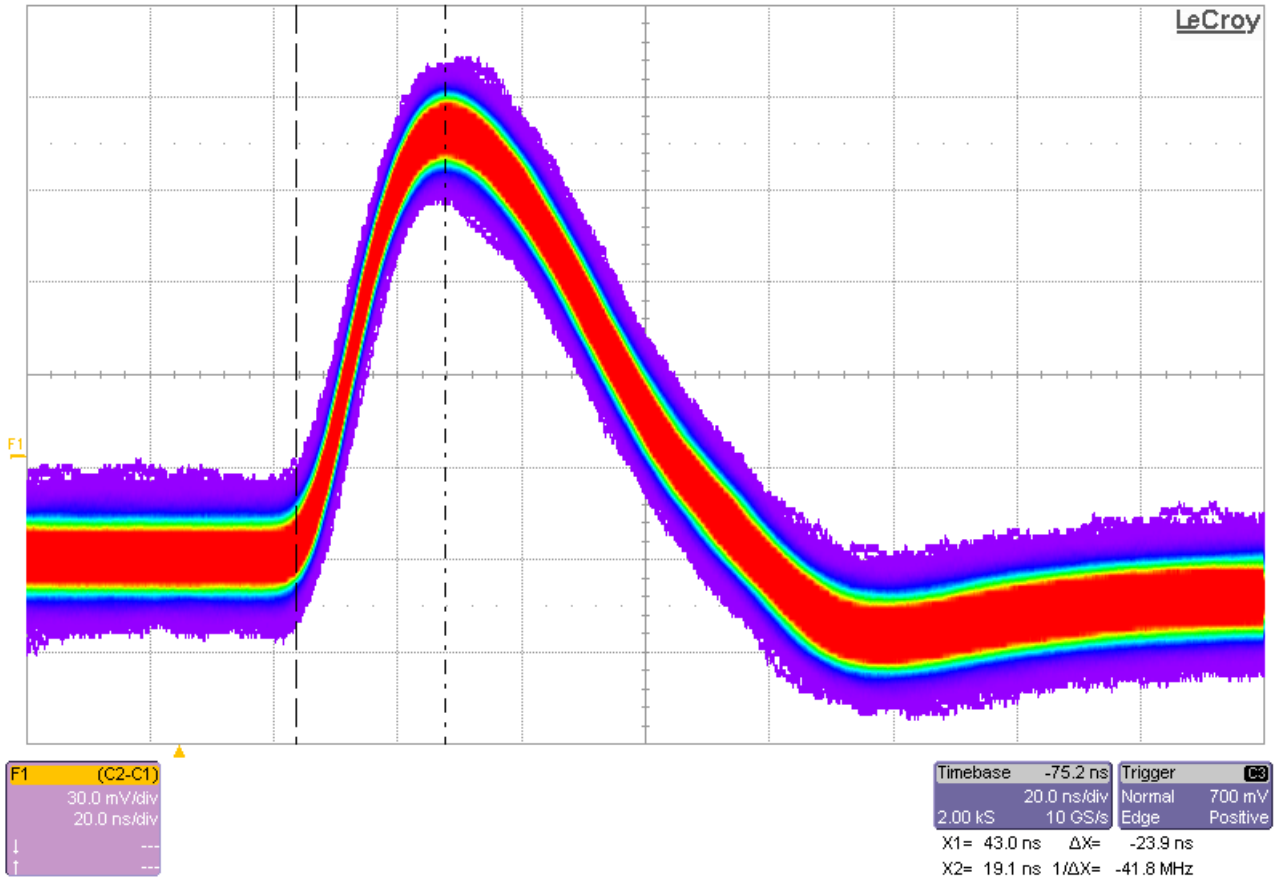
- Analogue measurements done for 80, 100 and 120uA bias of the input transistor and nominal bias condition of the remaining stages
- Nominal voltage power supply (1.2V), measurements have been done at room temperature

Response to 3fC signal, 0.5pF input capacitance, 100uA bias



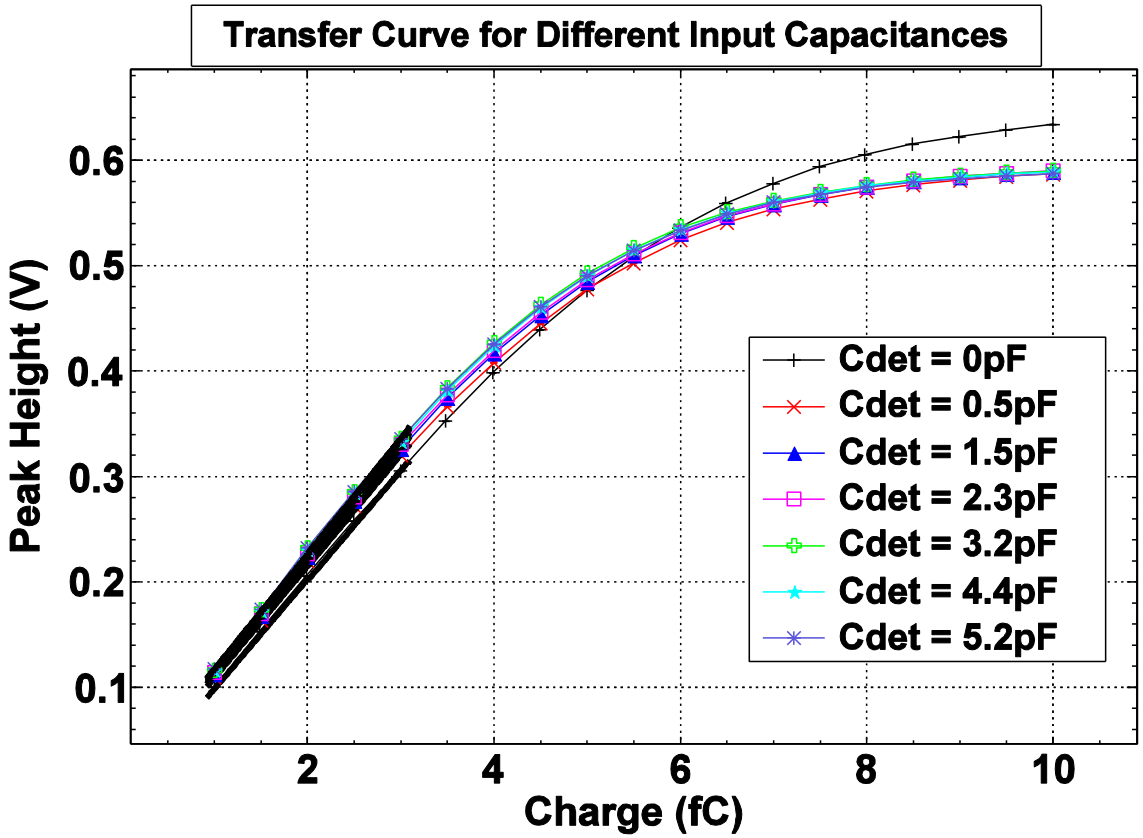
Peaking time ~22ns

Response to 3fC signal, 5pF input capacitance, 100uA bias



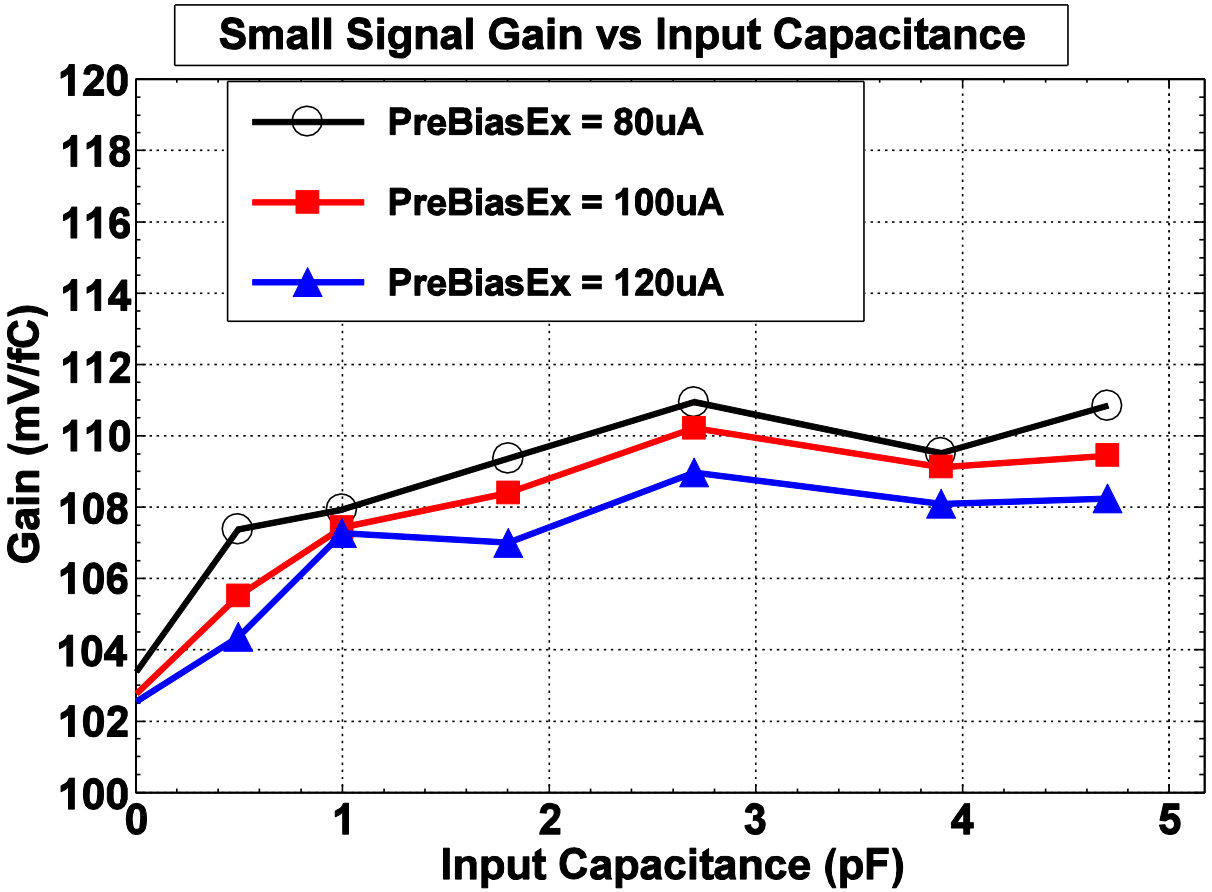
Peaking time ~24ns

Linearity and dynamic range

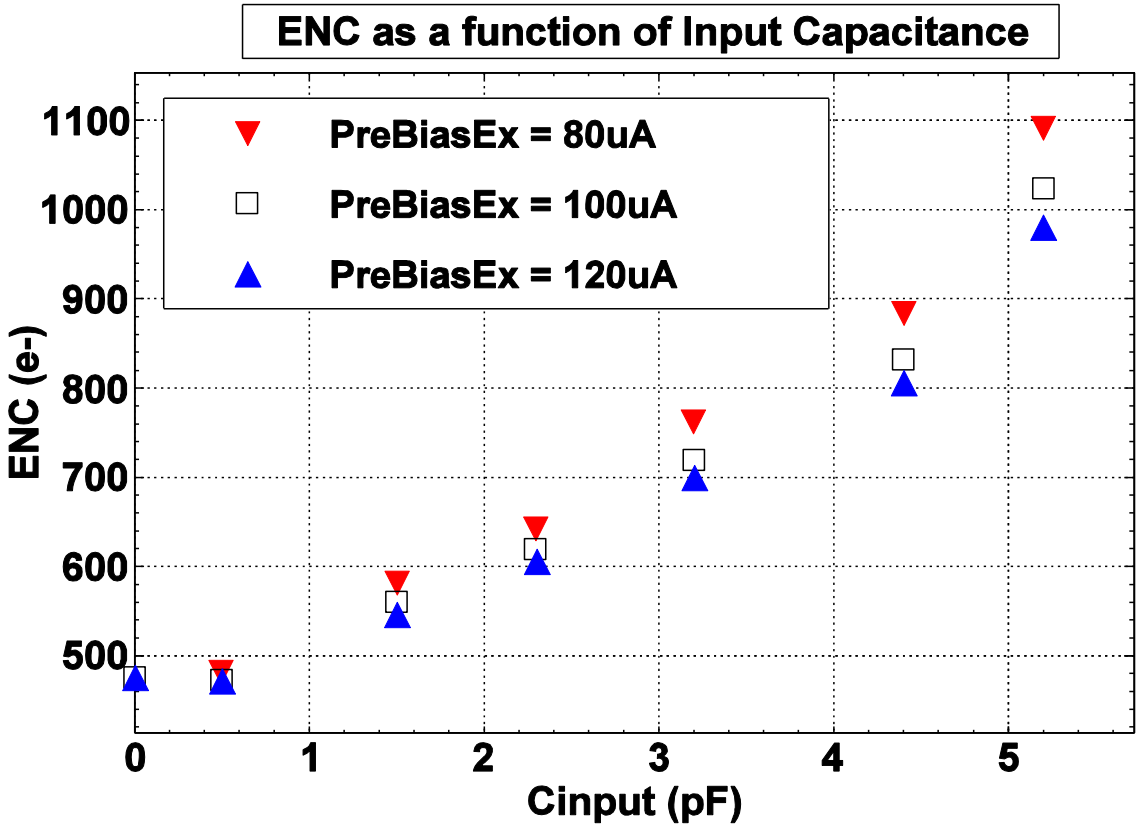


Good linearity up to 4fC (400mV signal range)
Dynamic range up to 6fC (limit set by the bias of the differential stage)

Gain versus input capacitance



ENC versus input capacitance



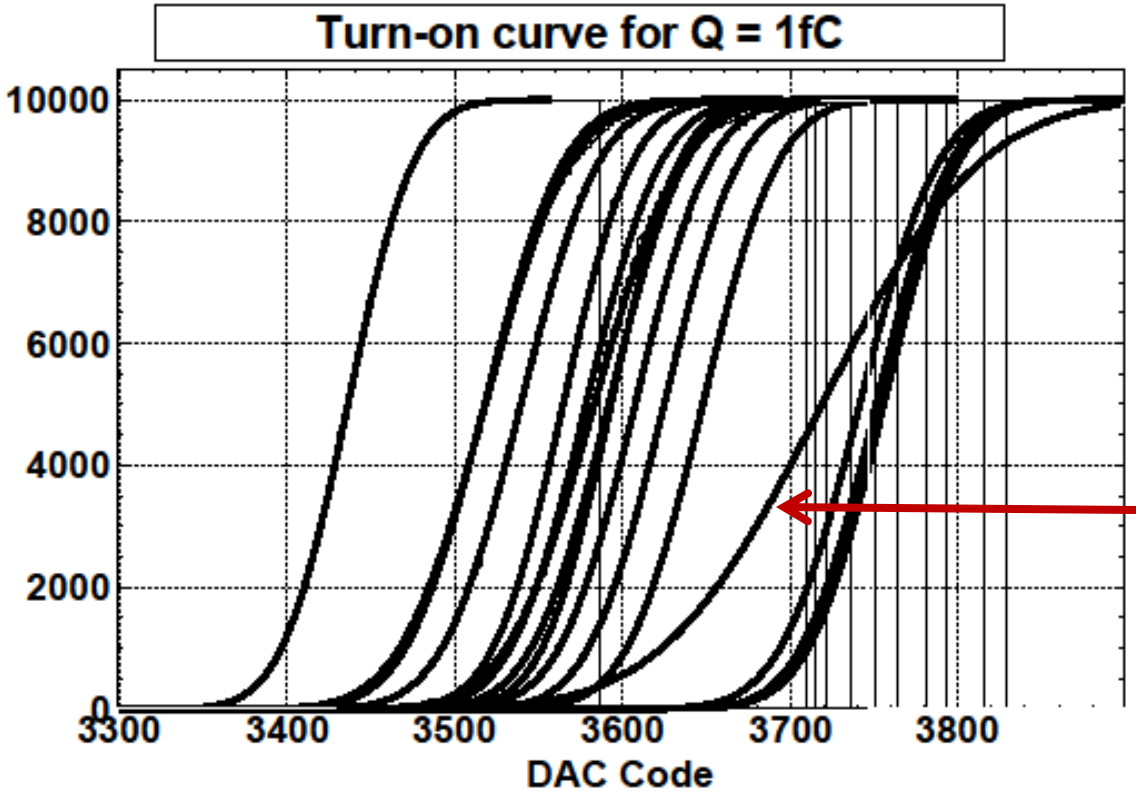
ENC at 0 input capacitance as simulated (470e-)

ENC at 5pF roughly 10% higher than simulated

Preliminary measurement results of full chain

- Gain, offset and ENC extracted from threshold scans for signal charges from 1 to 2.5fC
- Nominal bias condition (100uA in the input transistor)
- Nominal voltage power supply (1.2V), room temperature

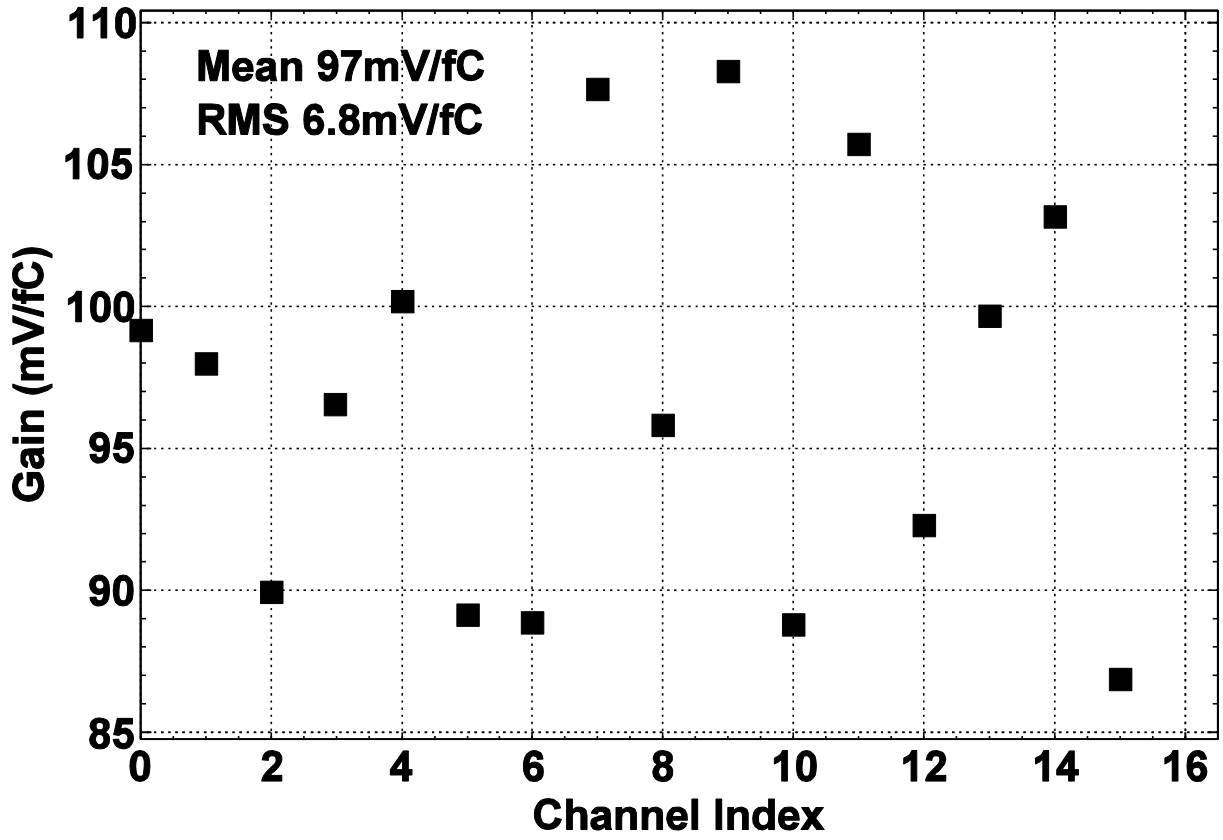
Threshold scans for 1fC signal, raw data



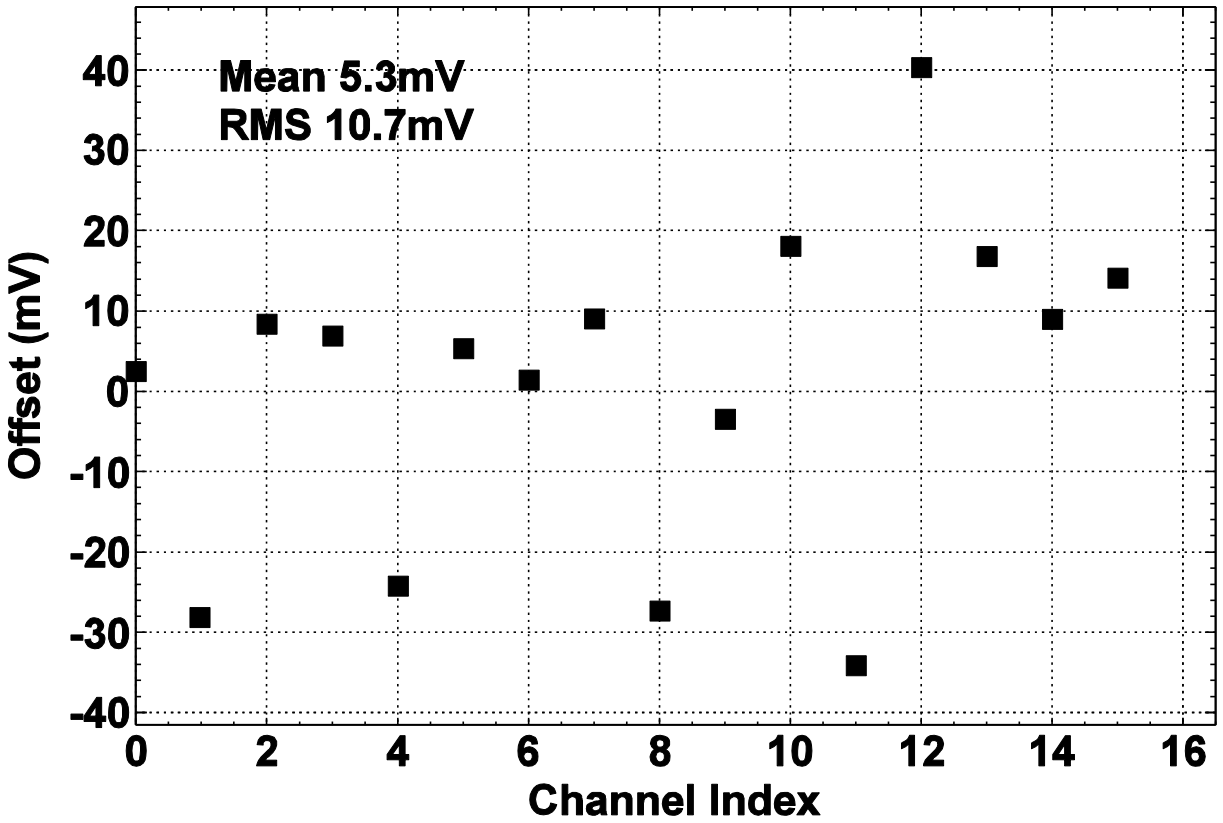
Channel #4 loaded with 5.2pF capacitor

1DAC code equivalent to 0.2mV

Distribution of channel gains



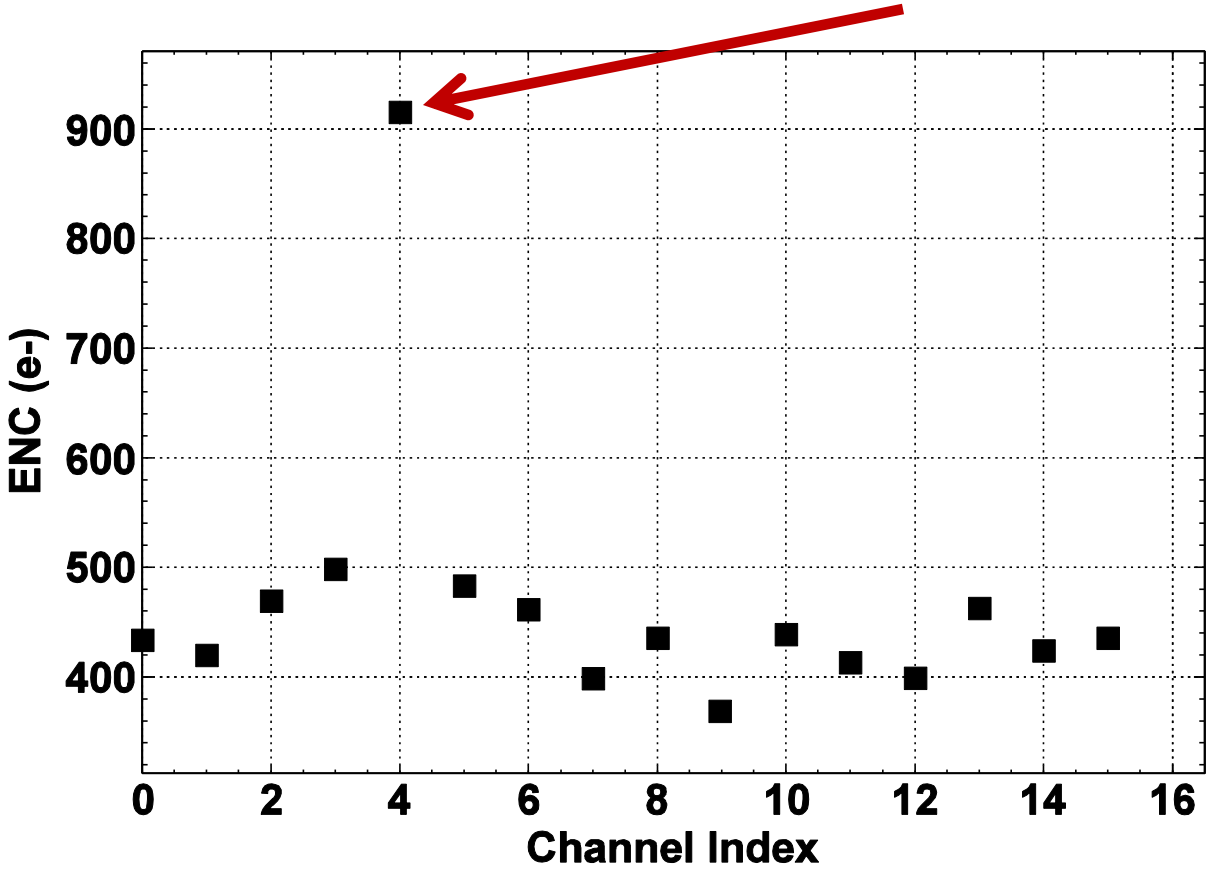
Distribution of discriminator offsets



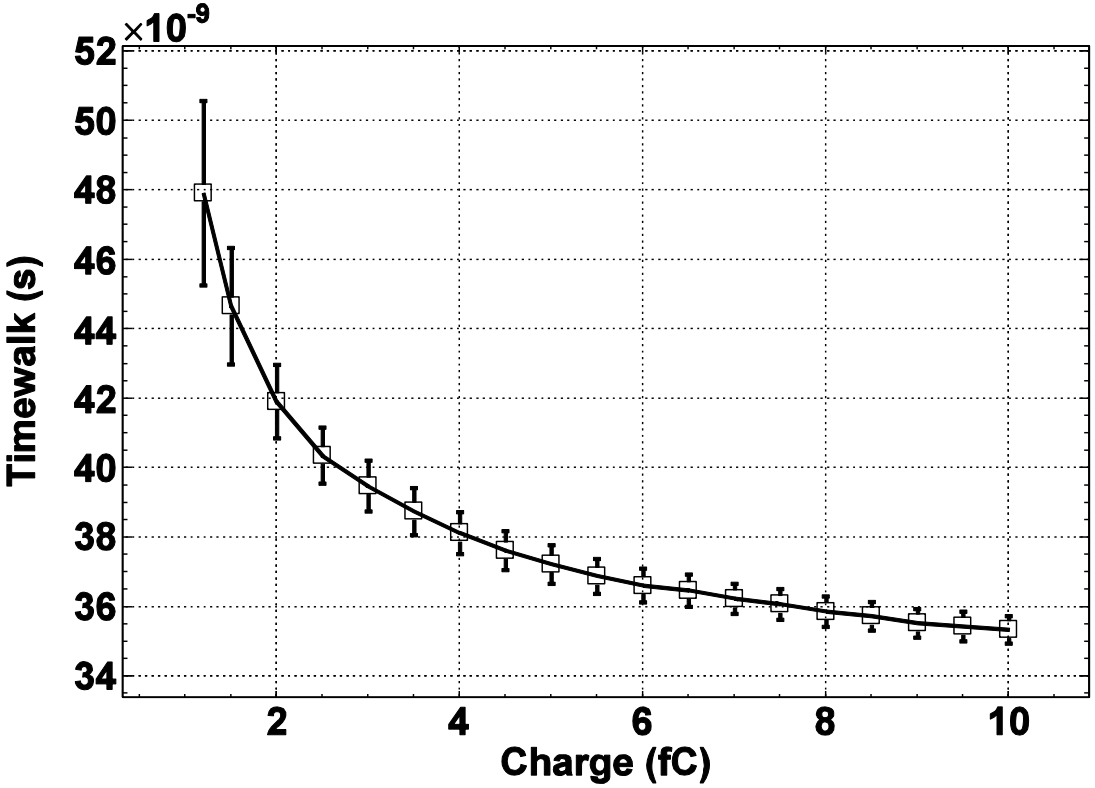
Mismatch 4x higher than simulated numbers

ENC as a function of channel number

Channel #4 loaded with external capacitor (5.2pF)



Time walk



Channel 4 (loaded with 5pF input capacitance)
Threshold 1fC, signal sweep from 1.2 to 10fC
Time walk 12.5ns

Conclusions

- We show that 90nm CMOS process can be used for front end designs optimized for short SSD at SLHC
- Analogue parameters of the front end including ENC at low input transistor biases are close to simulated values (**ENC @ 5pF ~900e-, power consumption@ 1.2V ~220uW**)
- Presented design shows that savings of the power and current consumption in new technologies is feasible (even for more elaborated architectures)
- Thanks to higher ft and GBP of preamplifier designed in new technologies the PSRR parameter is improved with respect to the older processes
- Mismatch of comparator offset and channel gains to be investigated
- Irradiation tests are planned