Level-1 jet trigger hardware for the ALICE electromagnetic calorimeter at LHC

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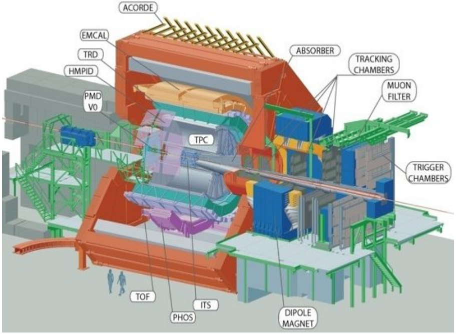
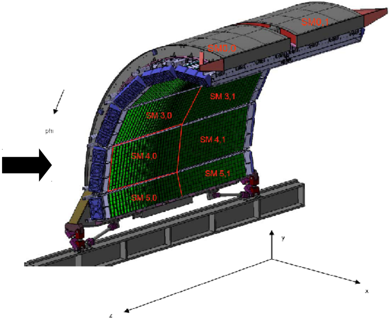
ElectroMagnetic CALorimeter (EMCAL) in ALICE





- ALICE has been upgraded with large acceptance calorimeter (increased the electromagnetic coverage by one order of magnitude)
  - Enhance its capabilities for measuring jet properties
- EMCAL design has been optimised to:
  1. measure the neutral energy component of jets
  2. provide fast and efficient L0, L1 trigger for hard jets

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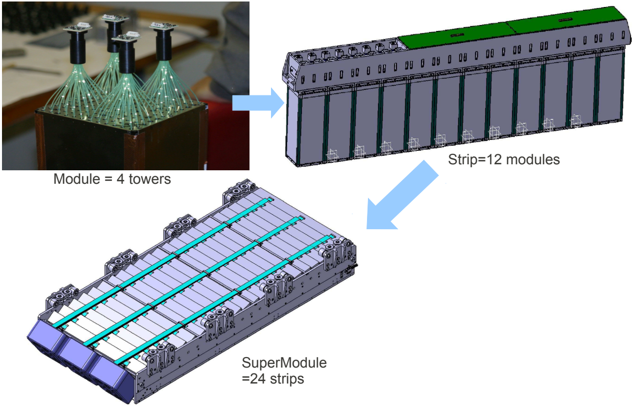
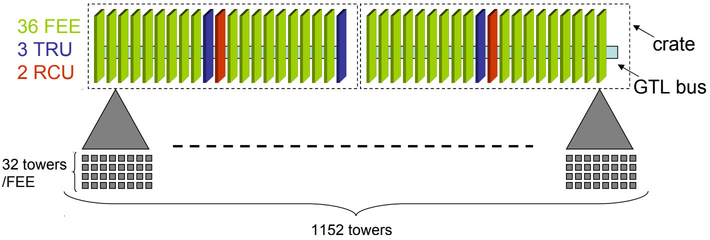


- Towers composed of 77 layers alternating lead and scintillator
- Signal readout via optical fiber + APD
- EMCAL $\rightarrow$ 10 complete SM and two $1/3$ SM
- $\Rightarrow$ 12288 towers to readout

One supermodule electronics



- FEE (Front End Electronics)
  - 32 analogue inputs
  - Generates 8 fastOr for TRU $\rightarrow$ module analogue sum (2×2 tower)
- TRU (Trigger Region Unit)
  - Receives and digitizes 96 fastOR signals from 12 FEE at the machine clock frequency (40.08 MHz)
  - Computes local L0 trigger (to transfer to **C**entral **T**rigger **P**rocessor)
  - Receives forwarded confirmed L0 from RCU
- RCU (Readout Control Unit)
  - Receives trigger sequence from CTP (confirmed L0, L1, L2)
  - Readout of 18 FEE (1/2 SM=1.5 TRU region)
  - Readout of 1 (or 2) TRU

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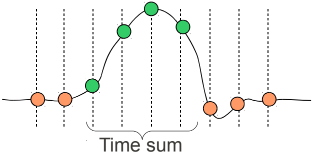
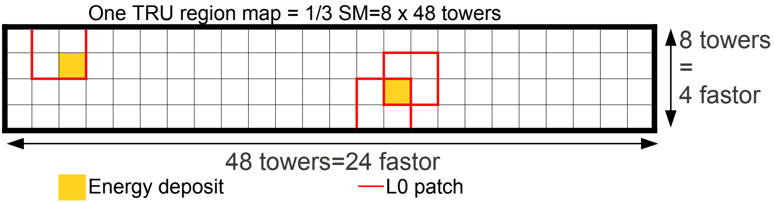
TRU L0 trigger algorithm

1. Fastor signal digitization at LHC clock (40.08 MHz)
2. Digital integration over a time sliding window of 4 samples



   - In preparation for L1: Time integrated values are also stored in a circular buffer

3. Energy summed over sliding window of 4 $\times$ 4 towers (2 $\times$ 2 fastOR) and compared to a minimum level threshold.



This trigger works only inside one TRU region → boundary effects.

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L1 trigger hardware developpement motivations (1/2)

- Reduce data rate to recording manageable rate, required rejection:
  - 10-20 for Pb+Pb (small collision rate, rejection by **H**igh **L**evel **T**rigger)
  - $\sim$3000 for p+p (high collision rate, low event data volume $\rightarrow$ HLT rejection ineffective here, all at L0/L1)
- Maintain L1 triggers efficiency against collision centrality: threshold correction by multiplicity from V0 (2 forward array of scintillators counters (A and C side) serving as centrality detector)

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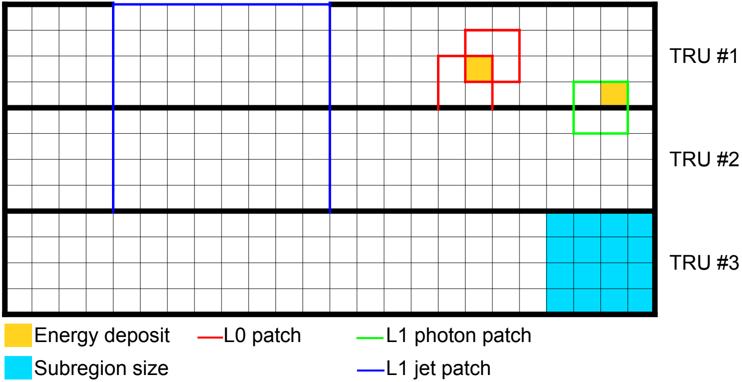
L1 trigger hardware developpement motivations (2/2)

- L0 trigger: OR of the 32 L0 calculated by the TRU
- L1-gamma trigger: Same patches as L0, but no boundary effect
- L1-jet trigger: Energy summed over a sliding window of 2×2 subregions (1 subregion = 4x4 FastOr = 8x8 towers)



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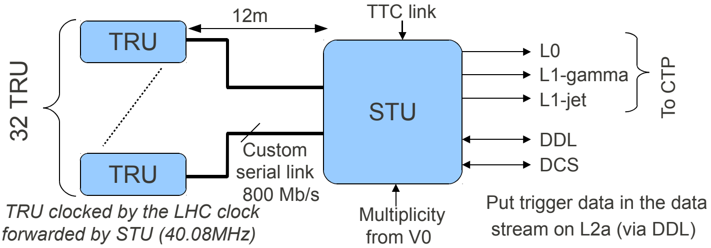
Summary Trigger Unit (1/2)



- STU hardware is FPGA centered (XC5VLX110FF1153)
- Data agregation required → connection to all TRUs (custom serial protocol needed)
- **T**rigger, **T**iming and **C**locking interface: reference clock for experiment synchronisation and trigger messages for readout
- Triggers forwarded to the CTP inputs (L0@1.2 µs, L1@6.2 µs)
- **D**edicated **D**ata **L**ink, optical fiber running at 200 MB/s
- **D**etector **C**ontrol **S**ystem interface via a magnetic less Ethernet interface

Summary Trigger Unit (2/2)

- L1 threshold is computed event per event according to $A.V0^2 + B.V0 + C$, 2^{nd} order fit EMCAL energy=f(V0,HV)
- STU works as a readout subsystem as well
  - Returns triggering indexes and thresholds used on a per event basis.
  - Primitive triggering data can be returned for debugging
  - Multievent buffering is implemented
- DCS used for FPGA configuration and experiment configuration (thresholds, delays, ...)

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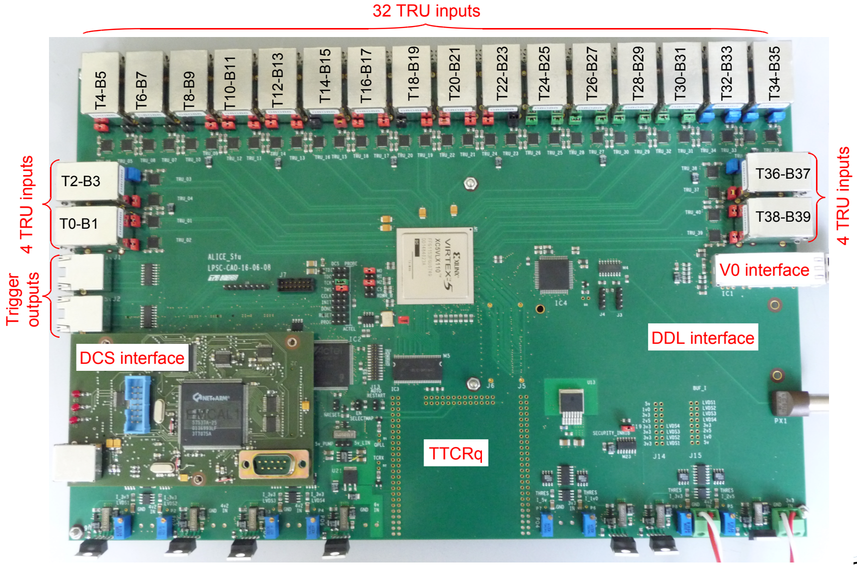
STU board



T0-B1 = **T**op is input 0, **B**ottom is input 1

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Custom serial protocol

Arguments for custom protocol

- Original TRU design equiped with a RJ45 spare connector directly linked to FPGA
- Transmission latency had to be kept low
- Hardware simplicity
  - no optical transceiver
  - single FPGA (ISERDES and IODELAY feature)
- TRU needed low jitter clock from STU and a line to forward local L0

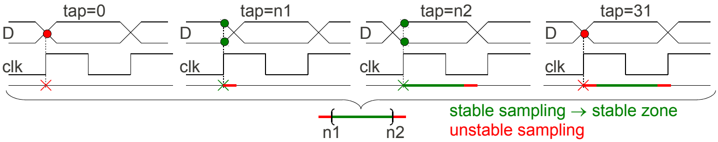
Solution chosen

- 4 pairs LVDS link over CAT7 Ethernet cable: skew$\searrow$, attenuation$\searrow$
  - 1 pair for LHC reference clock to TRU
  - 1 pair for L0 candidate from TRU
  - 2 pairs for data, each pair at 400 Mb/s, MSB first
- DC balancing: interpacket data constantly transmitted
- Interpacket data also used as synchronisation pattern
- Latency: fastOr is coded on 12 bit data $\rightarrow 96 \times 12/800 = 1.44\ \mu s$

Link synchronisation

Links synchronized by FSM in the FPGA before each start of run.

1. Data phase alignement with IDELAY block
   - IDELAY_CTRL uses 4×LHC clock as a reference, period ∼2.5 ns
   - tap value: 2.5 ns/32=78 ps
   - for all tap values, input data is delayed and stable reception is checked → stability zone
   - stability width (∼eye opening) is function of: period, signal degradation, deserializer input setup and hold times, clock jitter
   - data delay applied is the middle value of the stability zone

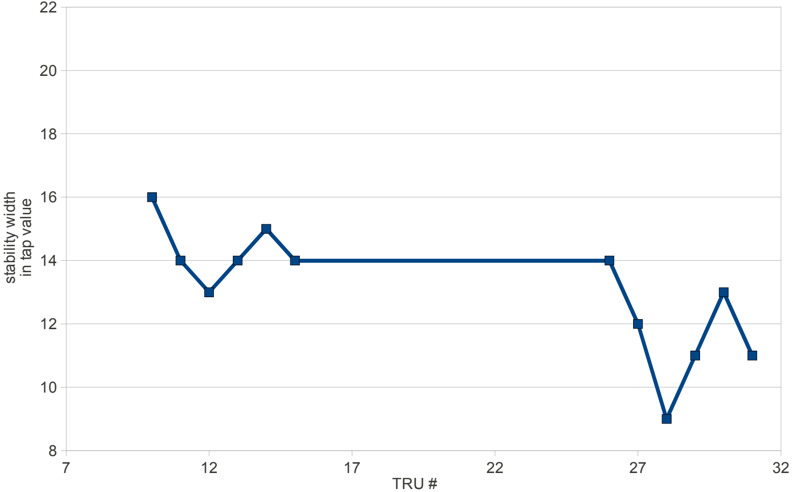


2. Character alignement with BITSLIP feature of ISERDES block
   - Looking for known pattern = 0xC03

MSB	LSB
100001	100001
000011	000011 ← GOOD
000110	000110
001100	001100
011000	011000
110000 ← GOOD	110000

Link performance

- Results obtained in real setup, 4 SM installed (6+6 TRU)



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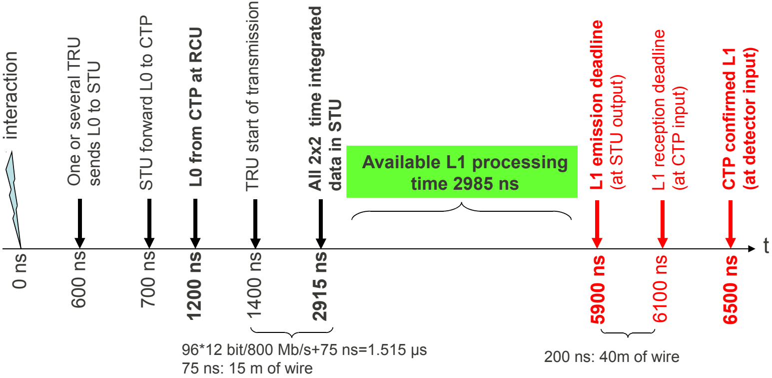
Trigger and timing constraints

- Fixed latency between interaction and trigger → event identification
- ALICE timing values:
  - candidate L0 arrival @ CTP inputs: 800 ns (32 BC!!!)
  - confirmed L0 arrival @ subdetector: 1.2 μs
  - candidate L1 arrival @ CTP inputs: 6.1 μs
  - confirmed L1 arrival @ subdetector: 6.5 μs



⇒Process 2961 photon and 165 jet possible patches in 2965 ns!

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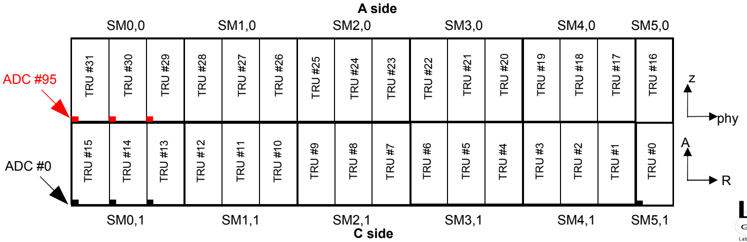
1. Upon confirmed L0 reception, TRUs send approriate time integrated data from circular buffers to the STU. ADC #0 first, ADC #95 last. For 1 region covered by TRU:

Row/col	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92
1	1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69	73	77	81	85	89	93
2	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70	74	78	82	86	90	94
3	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71	75	79	83	87	91	95

2. Slightly after L0, V0 sends its A and C plate information to STU → thresholds computation
3. In preparation for L1 photon processor, data mirroring is applied for data from A side by using data from ADC #95 first, new EMCAL map



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Photon trigger processing

Region of interest

Row/col	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92
1	1	5	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69	73	77	81	85	89	93
2	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62	66	70	74	78	82	86	90	94
3	3	7	11	15	19	23	27	31	35	39	43	47	51	55	59	63	67	71	75	79	83	87	91	95

A

Row/col	0
0	0
1	1
2	2
3	3

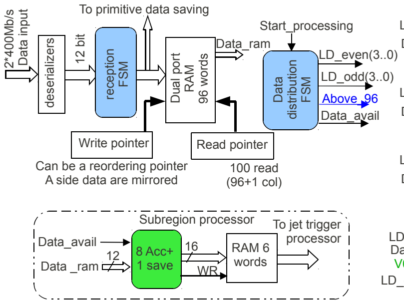
R

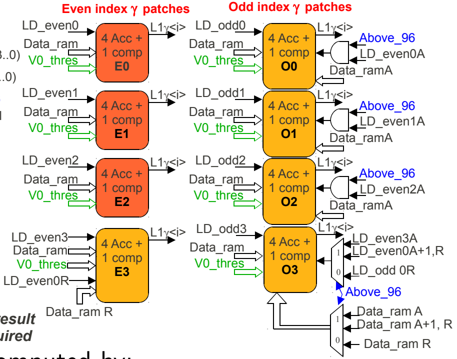
Row/col	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84	88	92

A+1,R

Row/col	0
0	0

- Parallel synchronous processing for each TRU region, data distributed to γ patch processors, only 8 accumulators needed.





Every 4 accumulations, each γ processor compares result to V0 threshold and generate indexed trigger is required

- For instance, a few patches computed by:
  - E0: [0, 1, 4, 5], [8, 9, 12, 13], ..., [88, 89, 92, 93]
  - O1: [5, 6, 9 ,10], [13, 14, 17, 18], ...,[85, 86, 89, 90]

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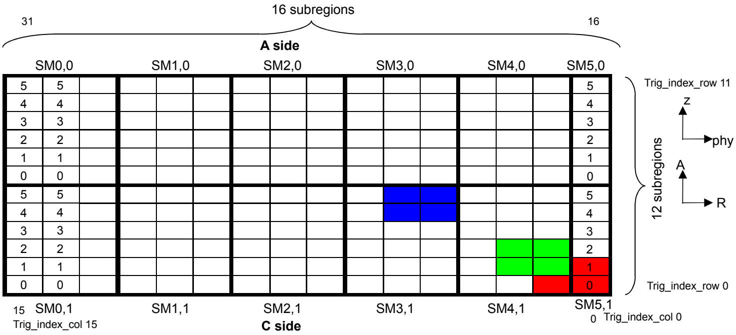
- No major difficulty, starts with a map of subregions instead of fastor



- Jet processor is somewhat similar to one of those described for photons, differences are:
  - 192 subregions to process (1 subregion=8x8 towers)
  - 11 patches of 2×2 in height yields 2 columns of 11 accumulators/comparators

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Conclusion / status

1. STU has been installed for a year
   - System interfaces validated (TTC, DDL, DCS, CTP, TRUs)
   - L0/L1 commissionned
   - Run in p+p with fixed thresholds (A=B=0)
   - Data validation in progress
2. Custom serial protocol validated in real condition with extensive data readout
3. Good tradeoff between parallel and serial computation
   - Internal FPGA logic used at $\sim$50% only! $\rightarrow$ major upgrades remain possible
   - 2961 photon 2×2 patches processing takes 825 ns
   - 165 jet 64×64 patches processing takes 1465 ns
   - Remaining margin 2985-2290=695 ns
4. 2 STUs will be used in DCAL (Di jet CALorimeter)