Study and methodology for decreasing noise emissions of DC-DC converters through PCB layout

Cristián Fuentes Rojas

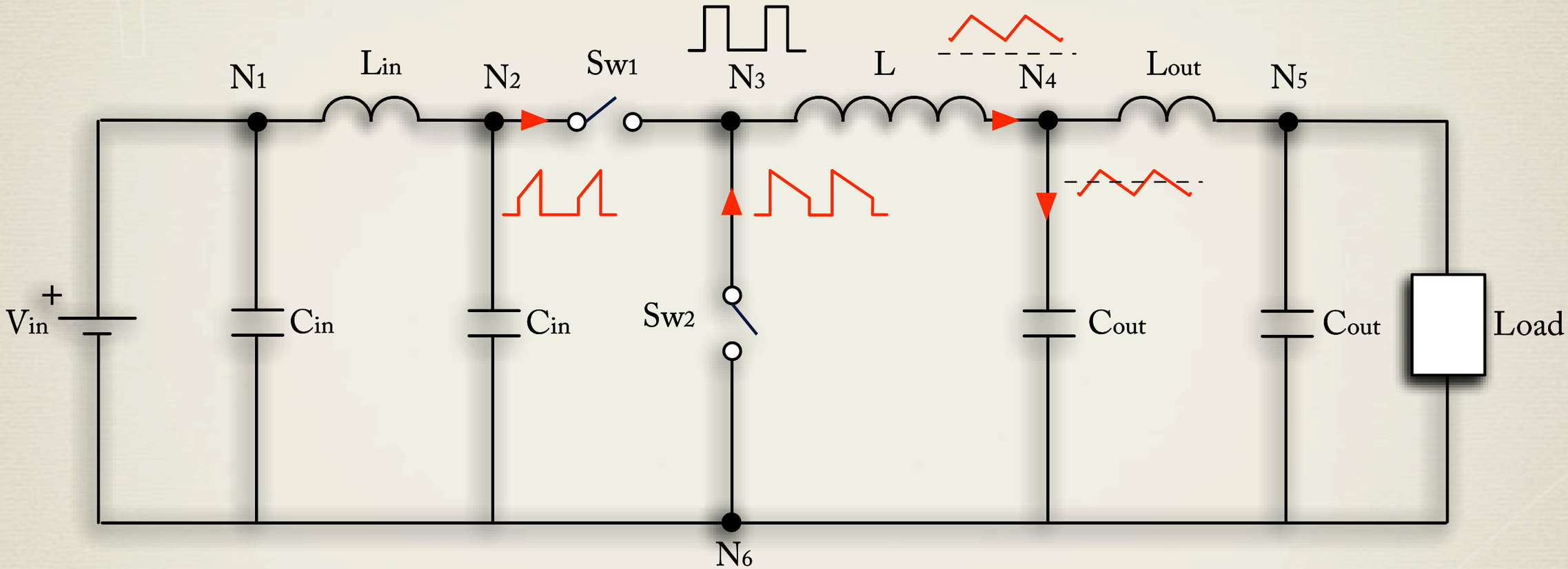
Introduction

- As presented at previous session, studies have been made to decrease the noise of dc-dc converters.
- For being able to decrease the noise through PCB layout, the sources of noise and paths must be identified.
- The sources are due to the switching nature, and their amplitude can be identified through Fourier series of theoretical or measured temporal signals.
- Several paths are not in schematics, and must be found in the real PCB board and setup.

Methodology

1. Modeling the DC-DC converter.
2. Enhancing the model with real parameters.
    - Real behavior passive components
    - Stray capacitances between PCB nodes
    - Inductances from PCB traces
    - Couplings between components
3. Identification of key parameters.
4. Improvement of board layout.

Model of a dc-dc buck converter



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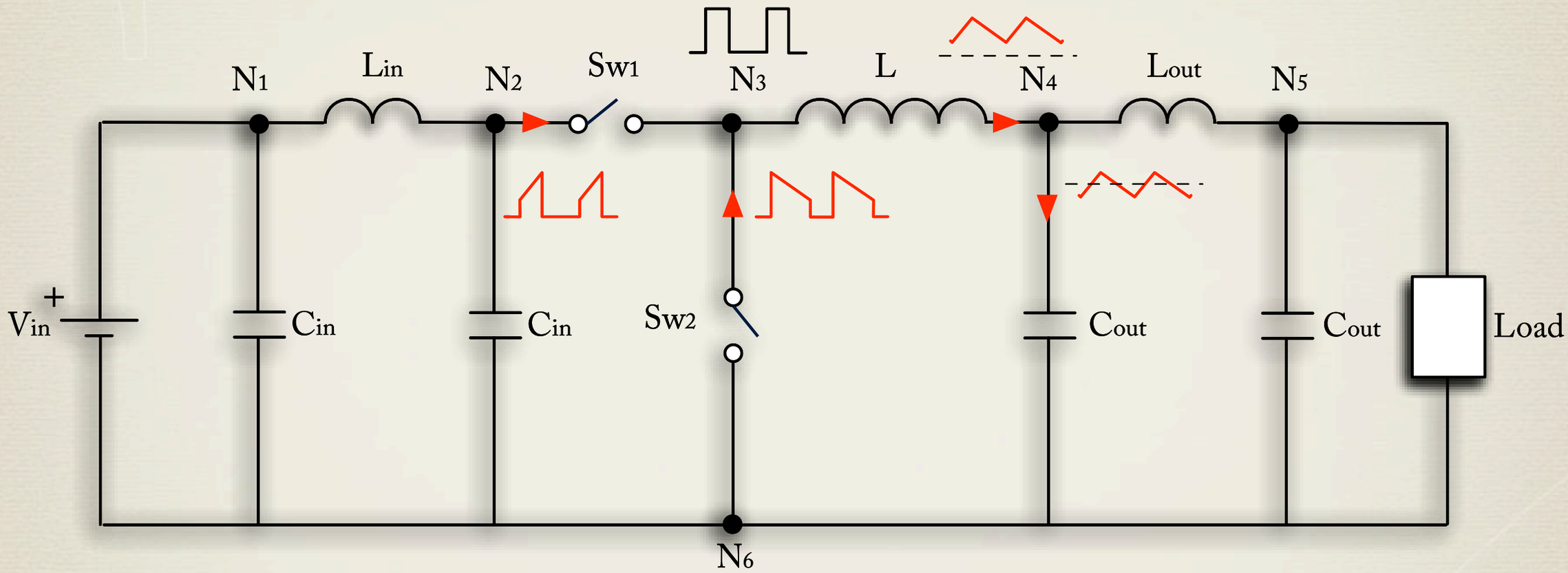
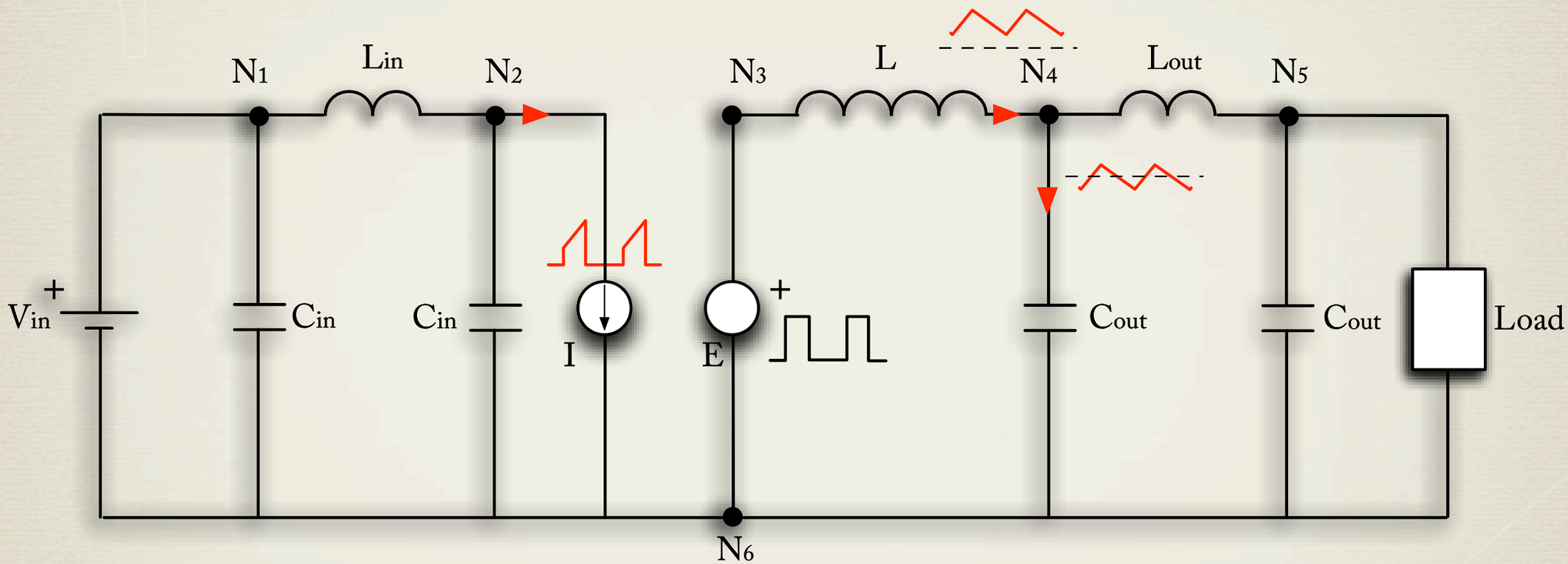


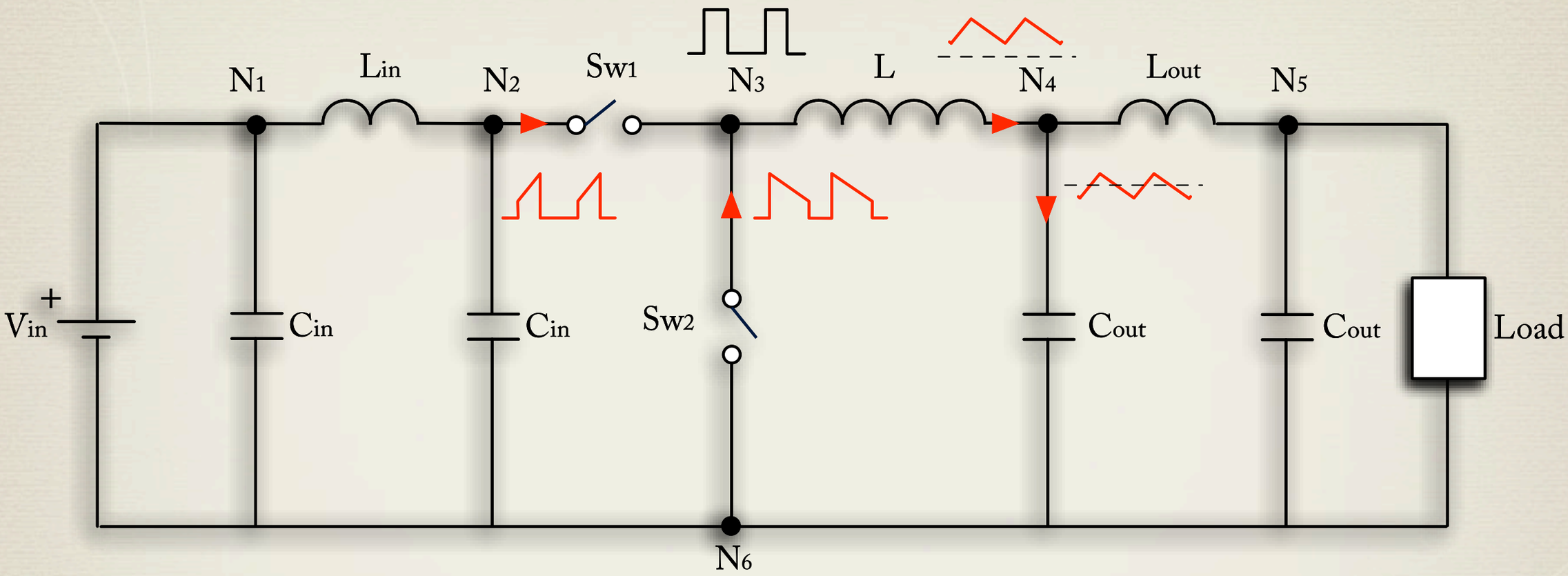
The switches will be replaced by AC voltage and current sources, with the values extracted from the Fourier series of the temporal signals.

Model of a dc-dc buck converter

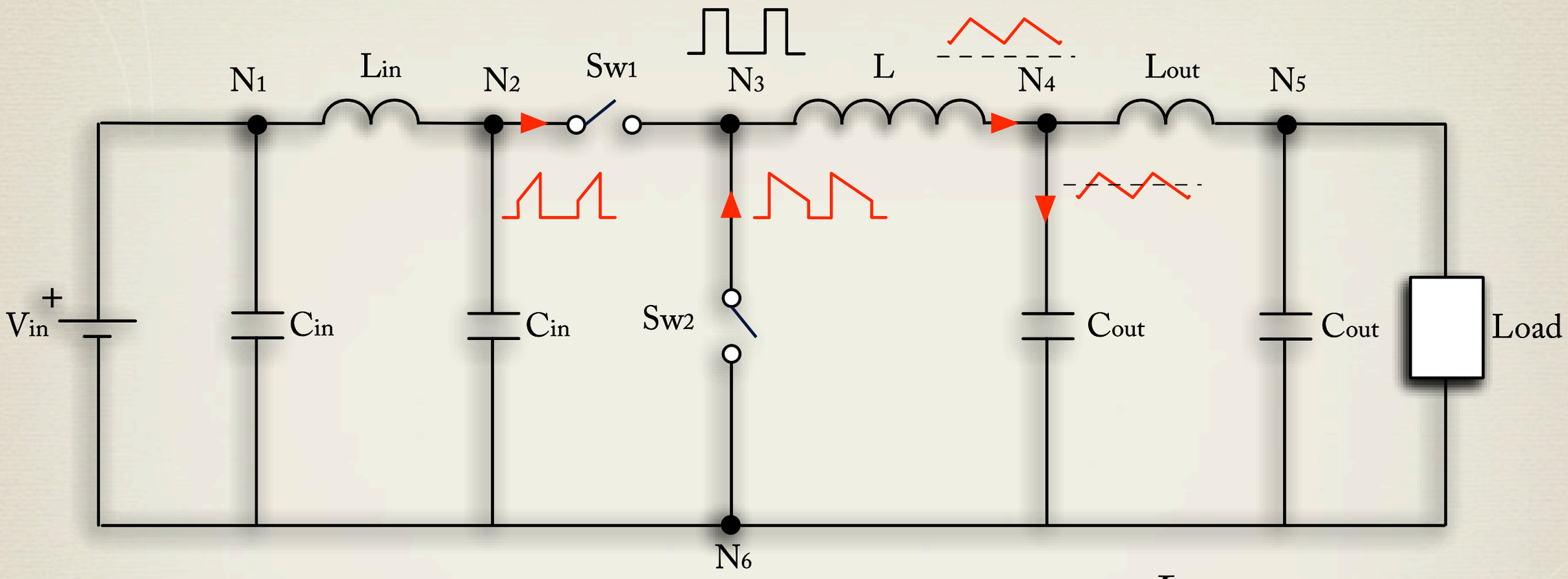


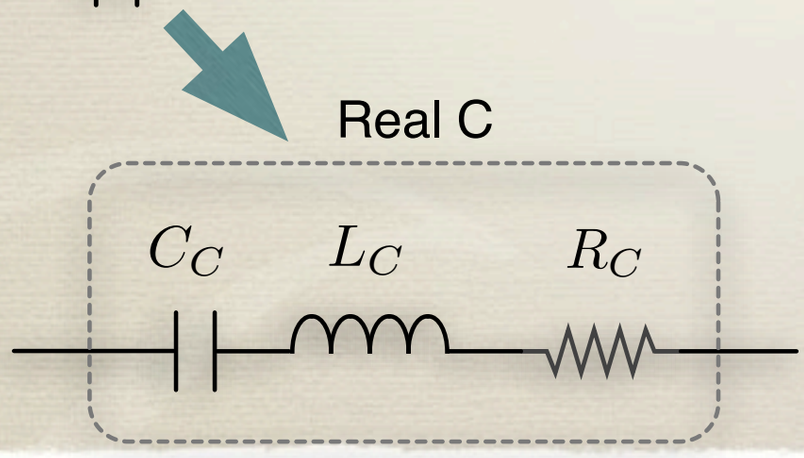
The switches will be replaced by AC voltage and current sources, with the values extracted from the Fourier series of the temporal signals.

1° Real components

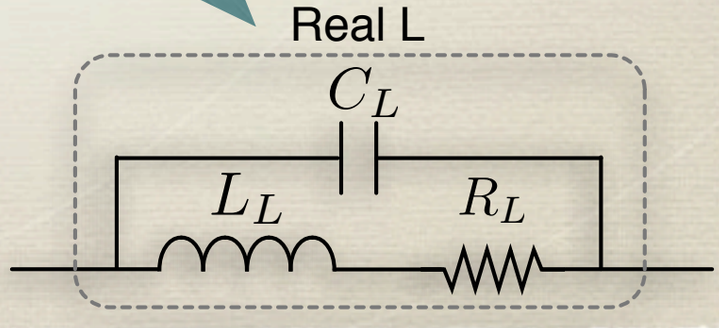


1° Real components





Ideal components
Replaced
by
Real components



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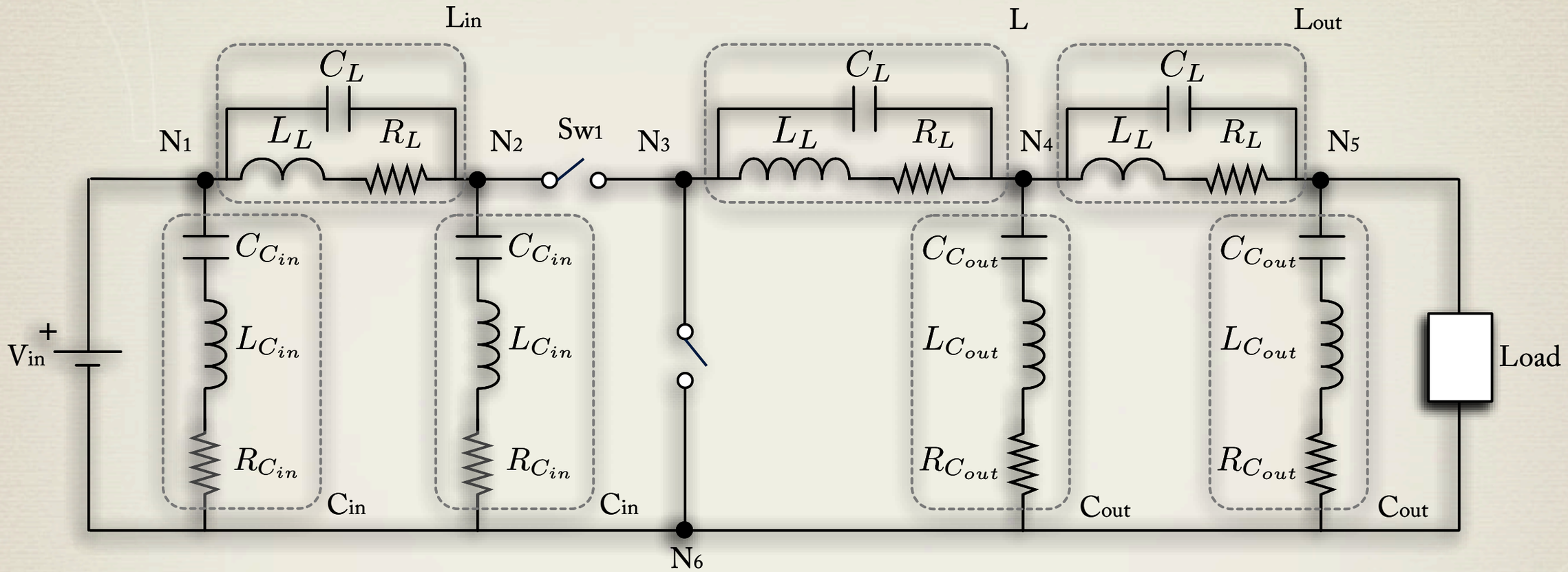

Ideal components

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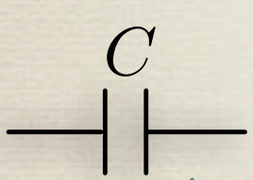
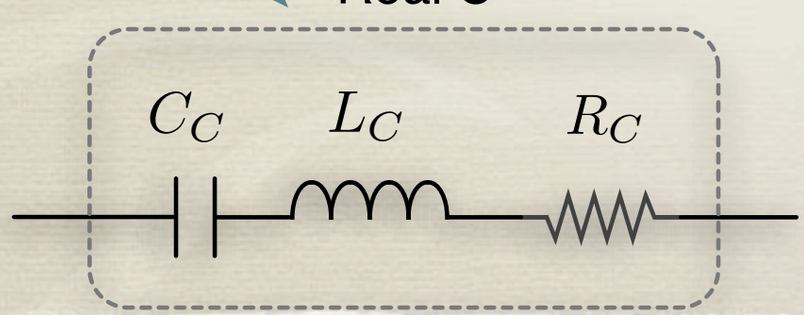
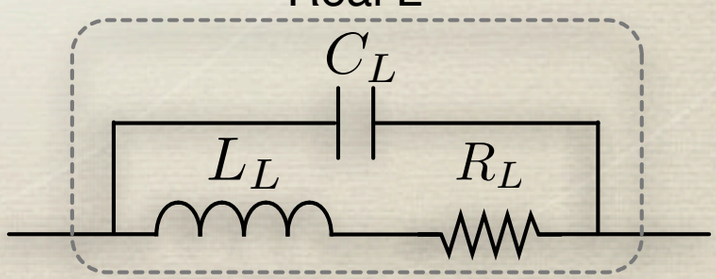


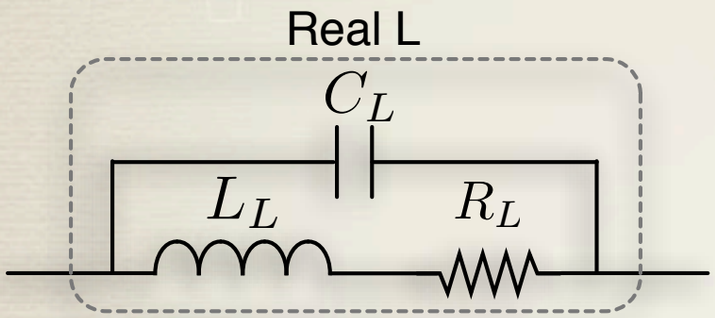
Real C

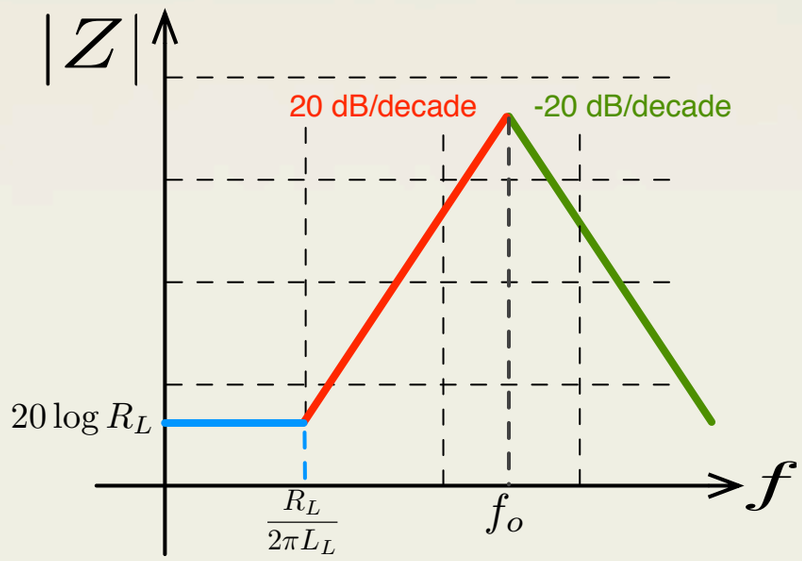


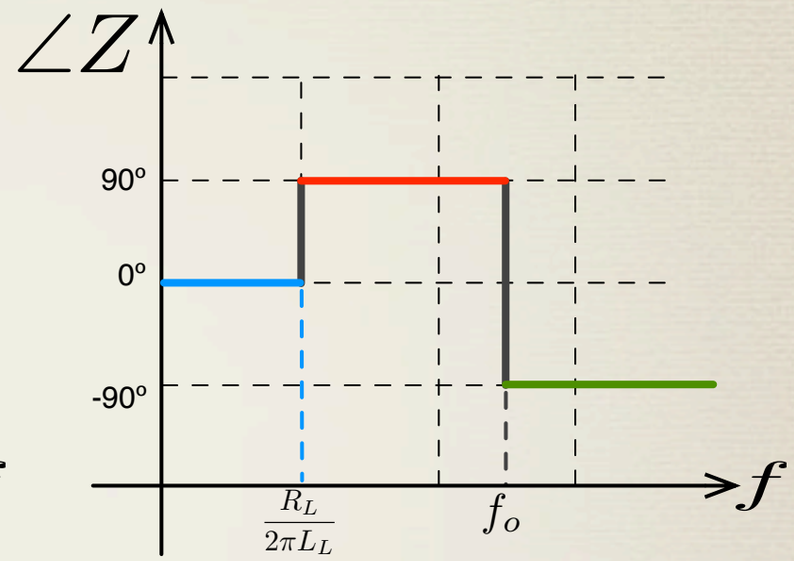
Real L

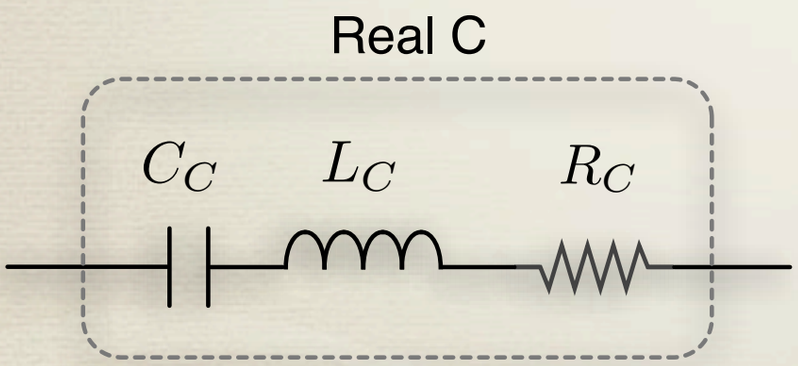


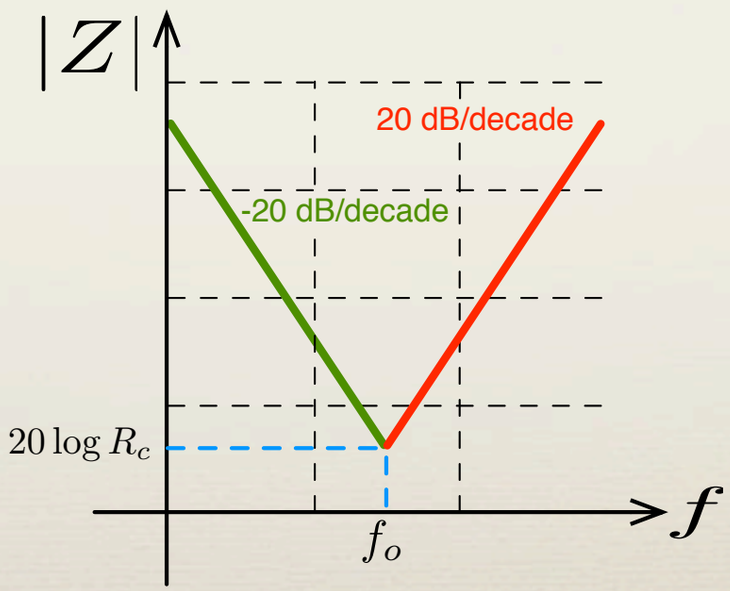
Behavior of real components

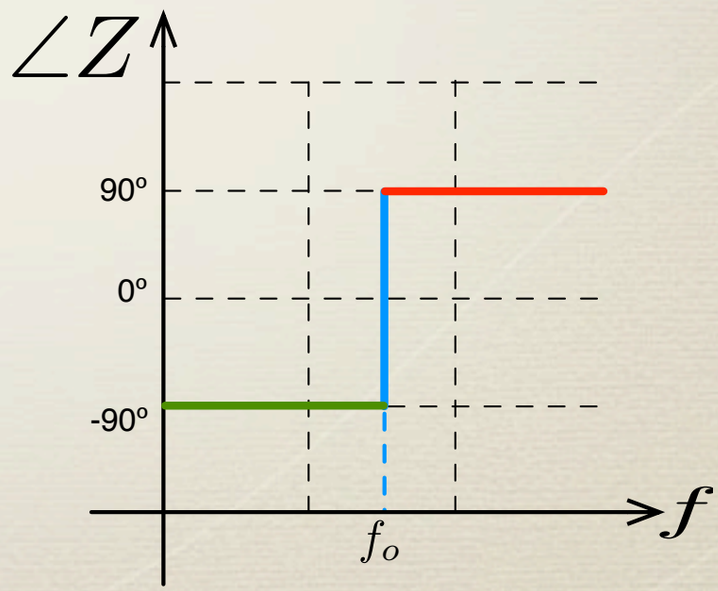








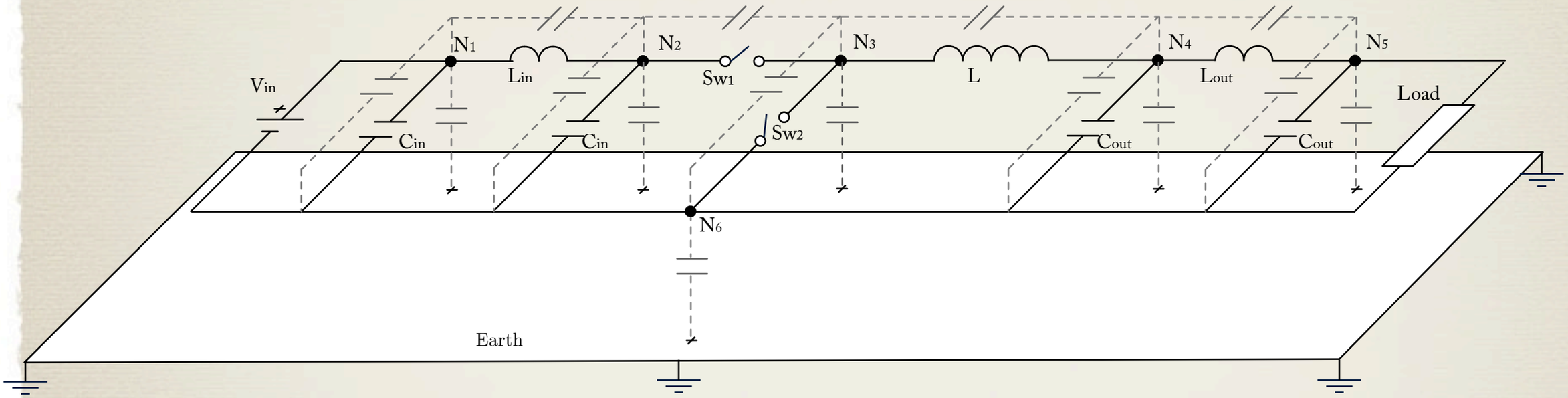




First Design Considerations

- Careful selection of low ESR&ESL components.
- Put capacitors in parallel to decrease total equivalent series inductance (ESL) of decoupling capacitors.
- Proper selection of operation mode:
  - QSW operation: produces lower amplitude AC input currents.
  - Increasing the switching frequency: it reduces the amplitude of the AC currents source but not the AC voltage source.

2º Stray capacitances

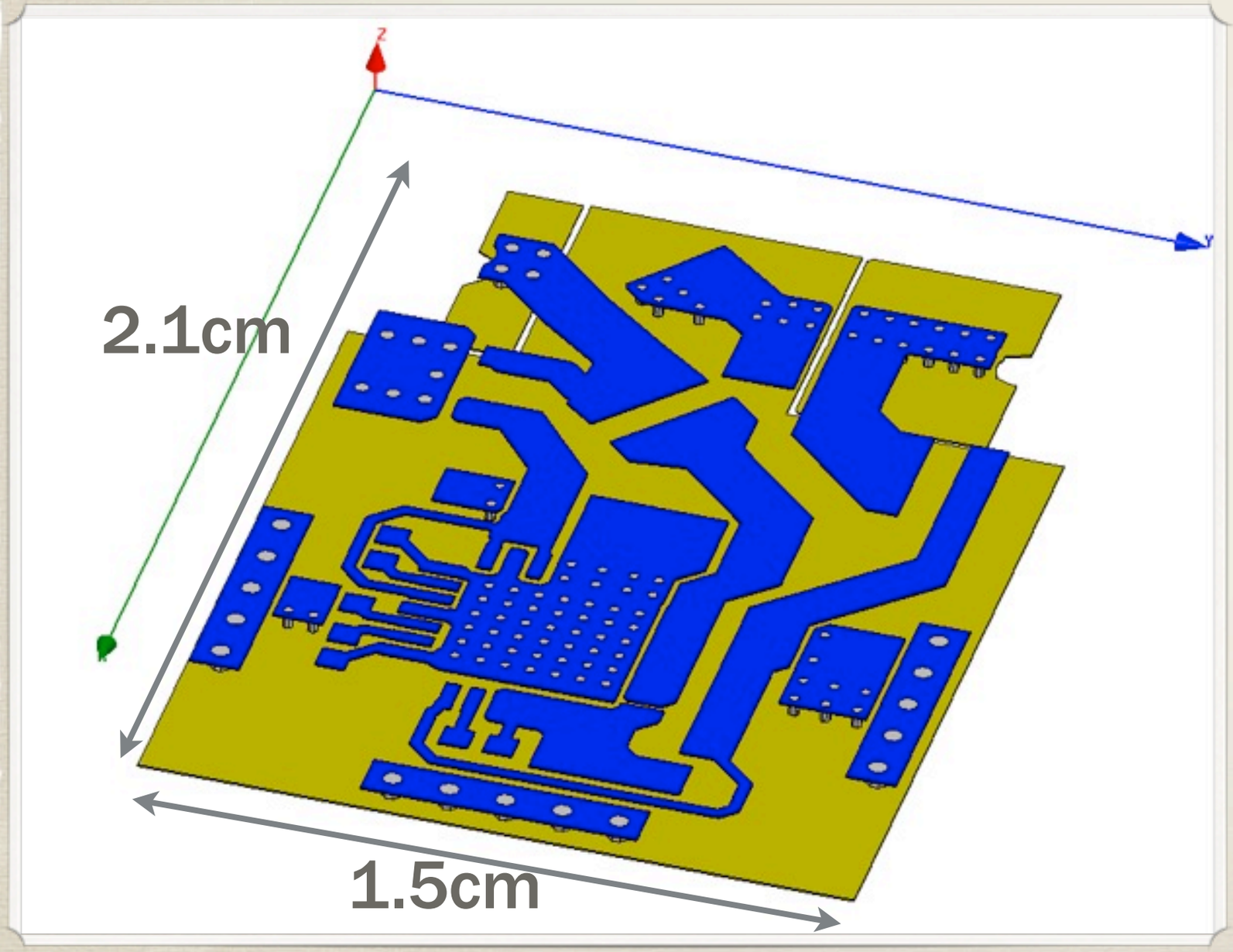


Nº of capacitances: $\binom{n}{k} = \frac{n!}{k! \cdot (n-k)!}$

n: Nºof nodes
k:combinations

$$\binom{7}{2} = 21$$

Obtaining Stray cap values



Softwares allow:

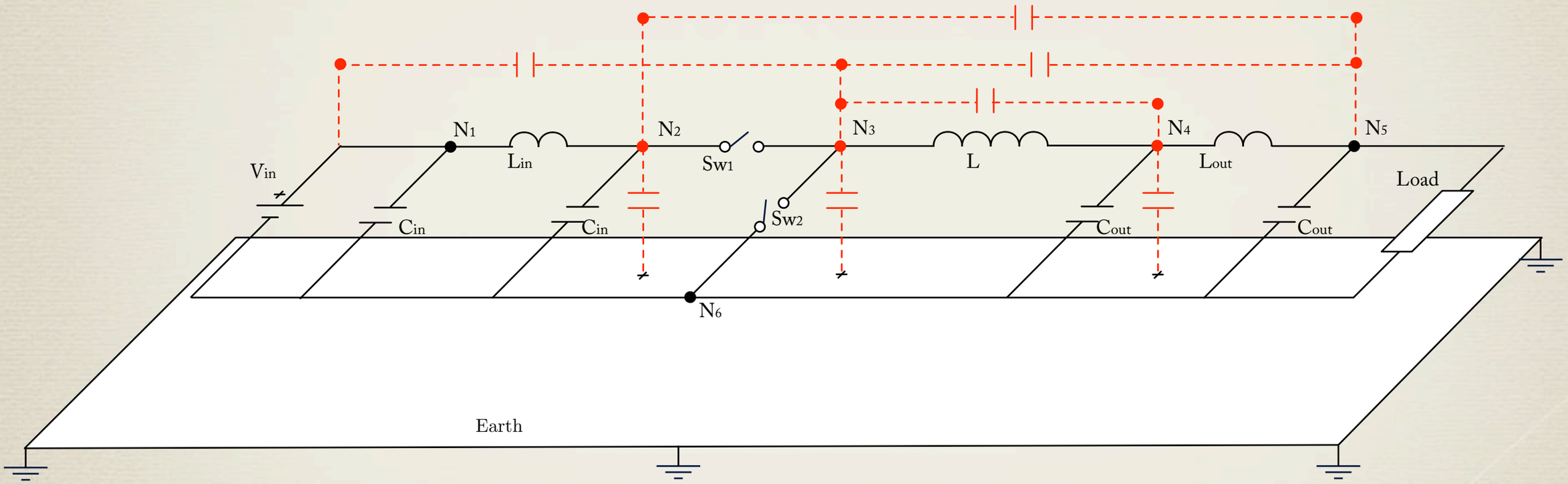
-Q3D:

- Extraction of stray capacitance values.

-Simplorer:

- Sweep their value through parametric simulations.
- Identify the most important capacitances for the noise.

Identifying critical Stray cap



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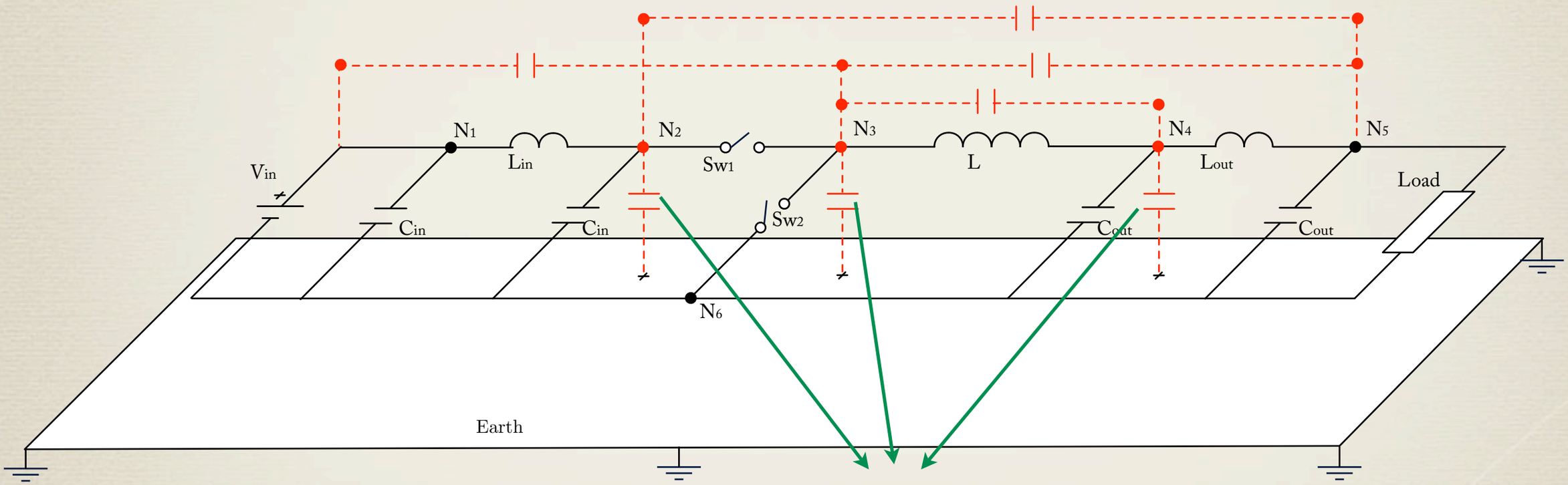
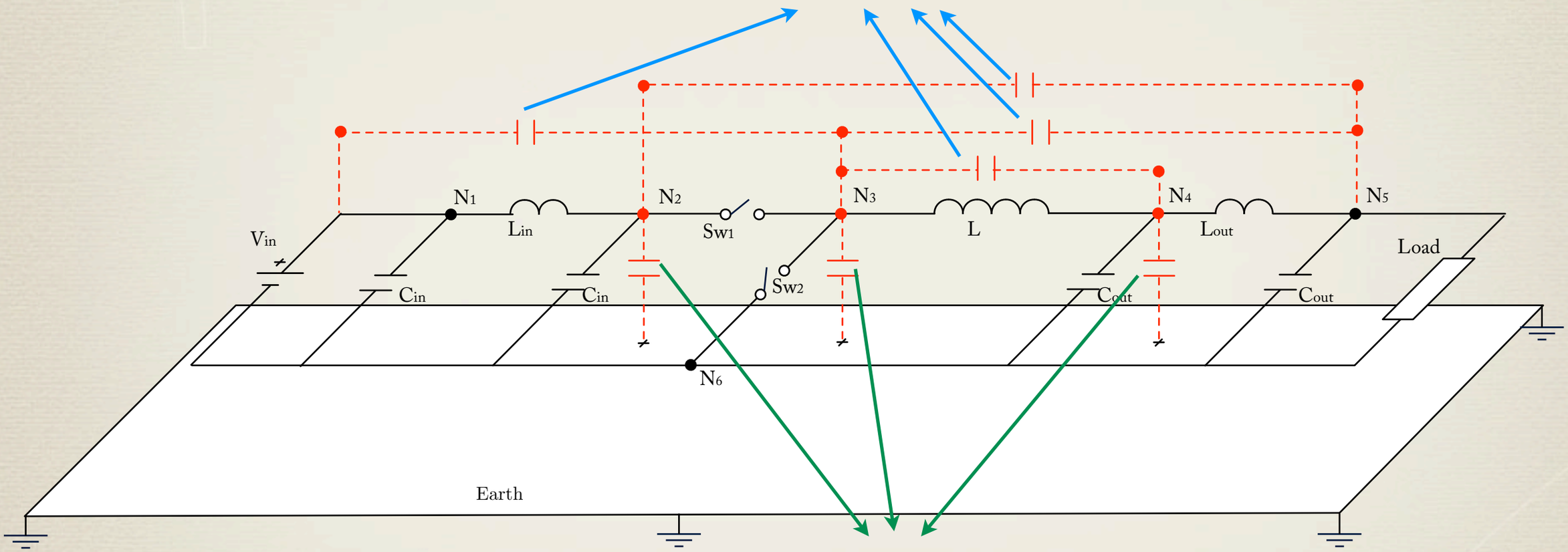


Impact mainly on CM noise

Identifying critical Stray cap

Impact mainly on DM noise



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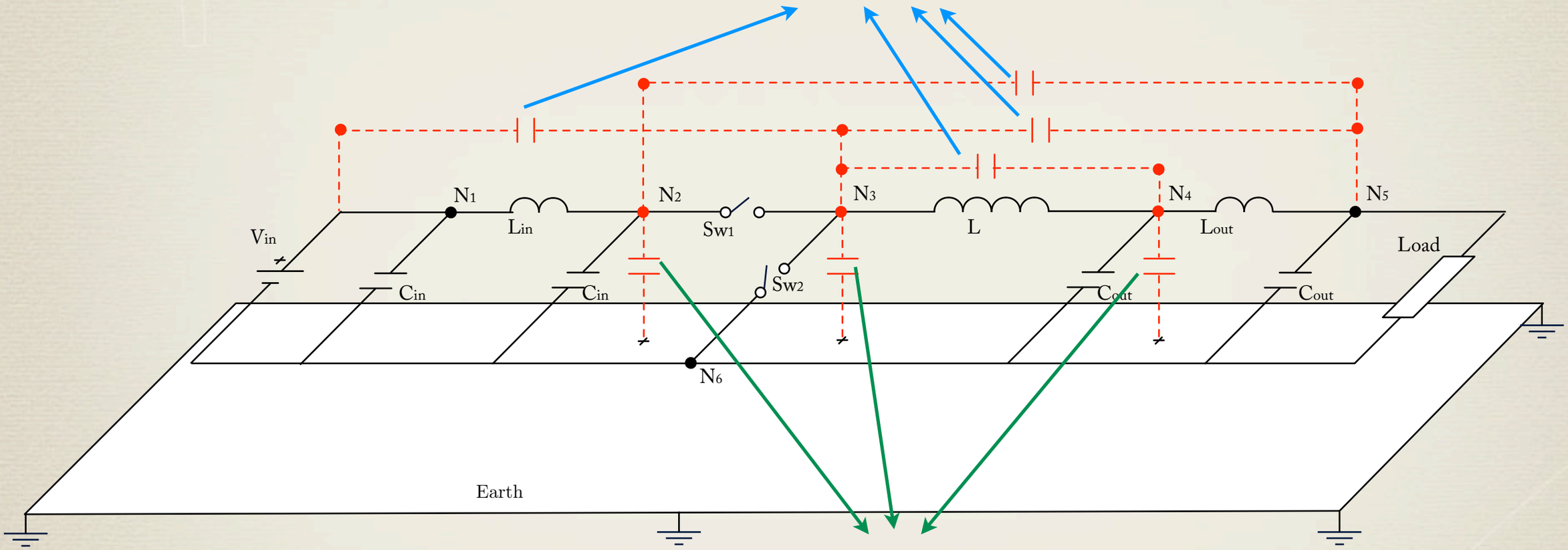


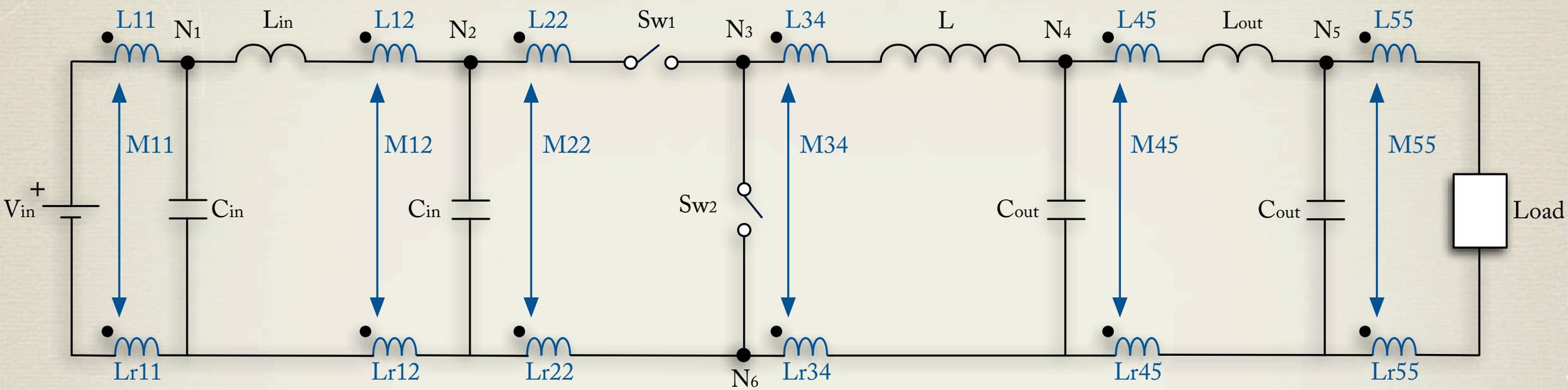
Impact mainly on CM noise

Not surprising that most of them are connected to N3 (phase) node that develops the highest dV/dt.

Second Design Considerations

- Phase node must have the less possible area to minimize the magnitude of the stray capacitances.
- Phase node must be placed as far as possible from input and output passive components, trying to have the less electric coupling between them.

3° Inductance of traces



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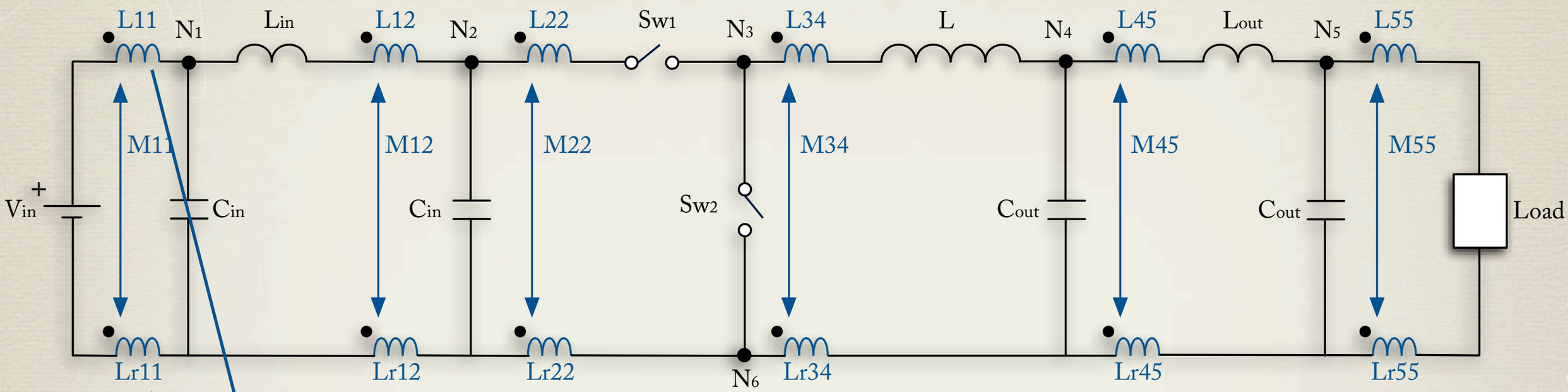
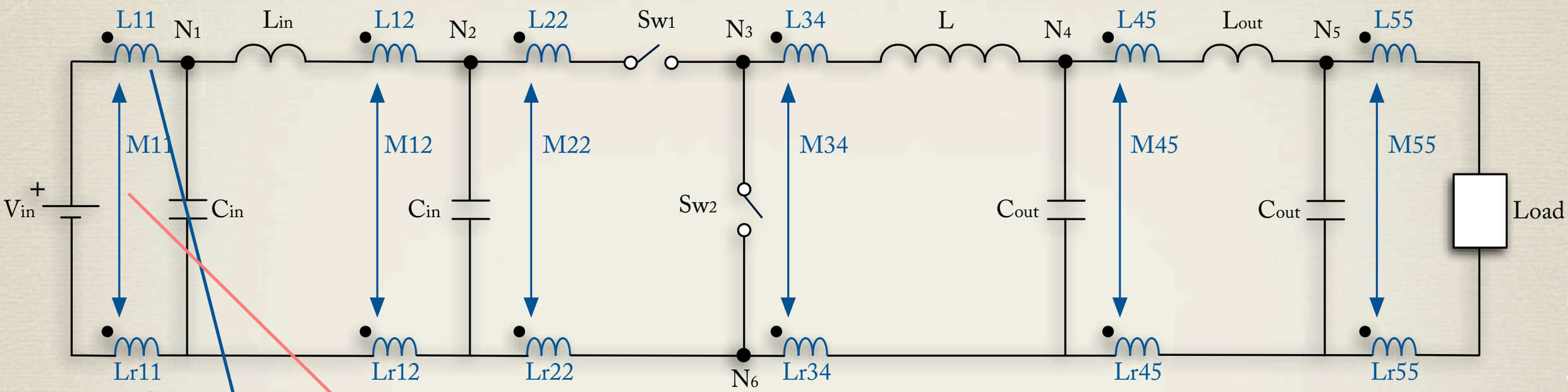


Self Partial Inductance

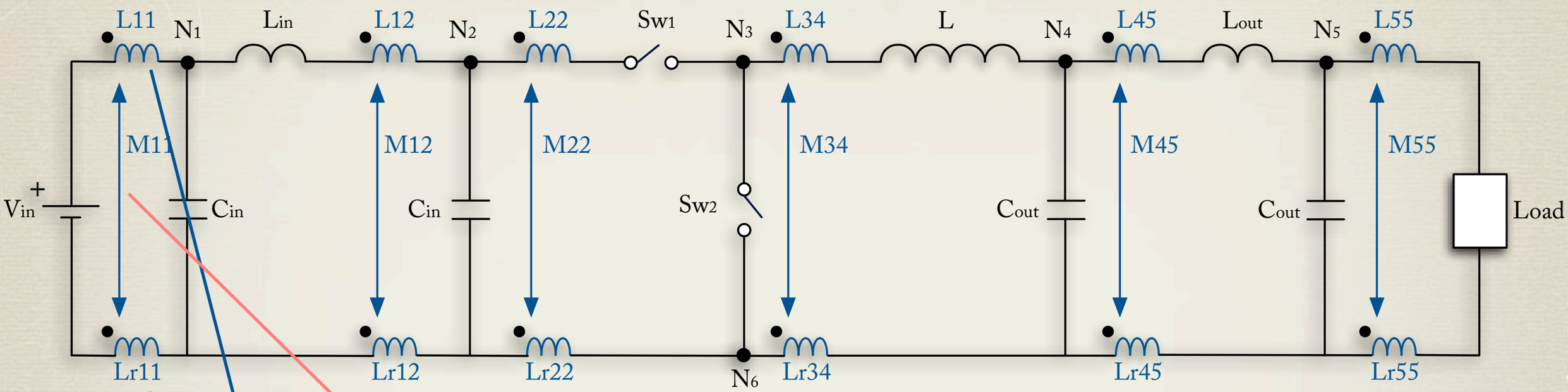
3° Inductance of traces



Mutual Inductance

Self Partial Inductance

3° Inductance of traces

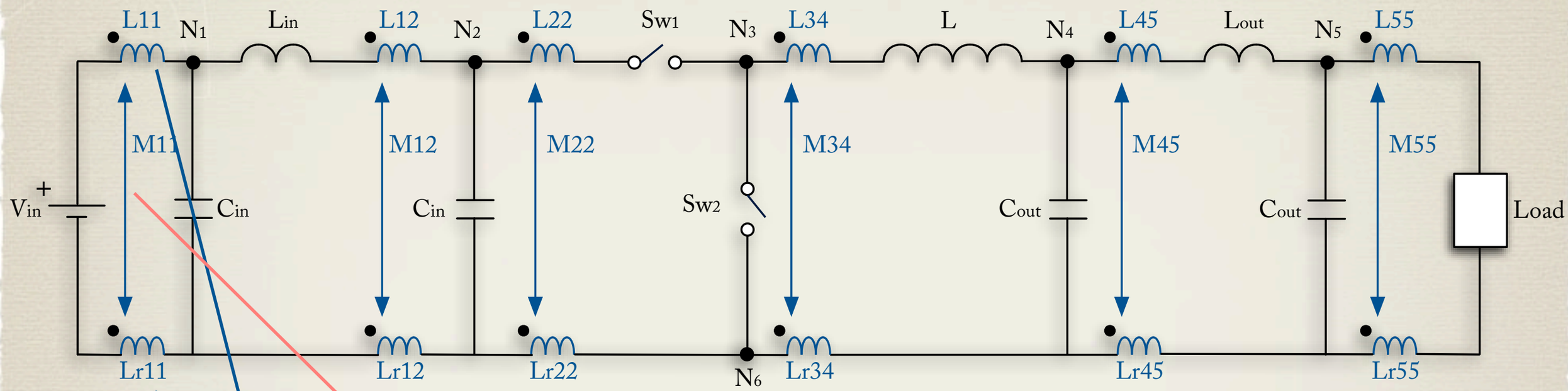


Mutual Inductance

Self Partial Inductance

$$Lr11_{NET} = Lr11_{SELF} - M11$$

3° Inductance of traces



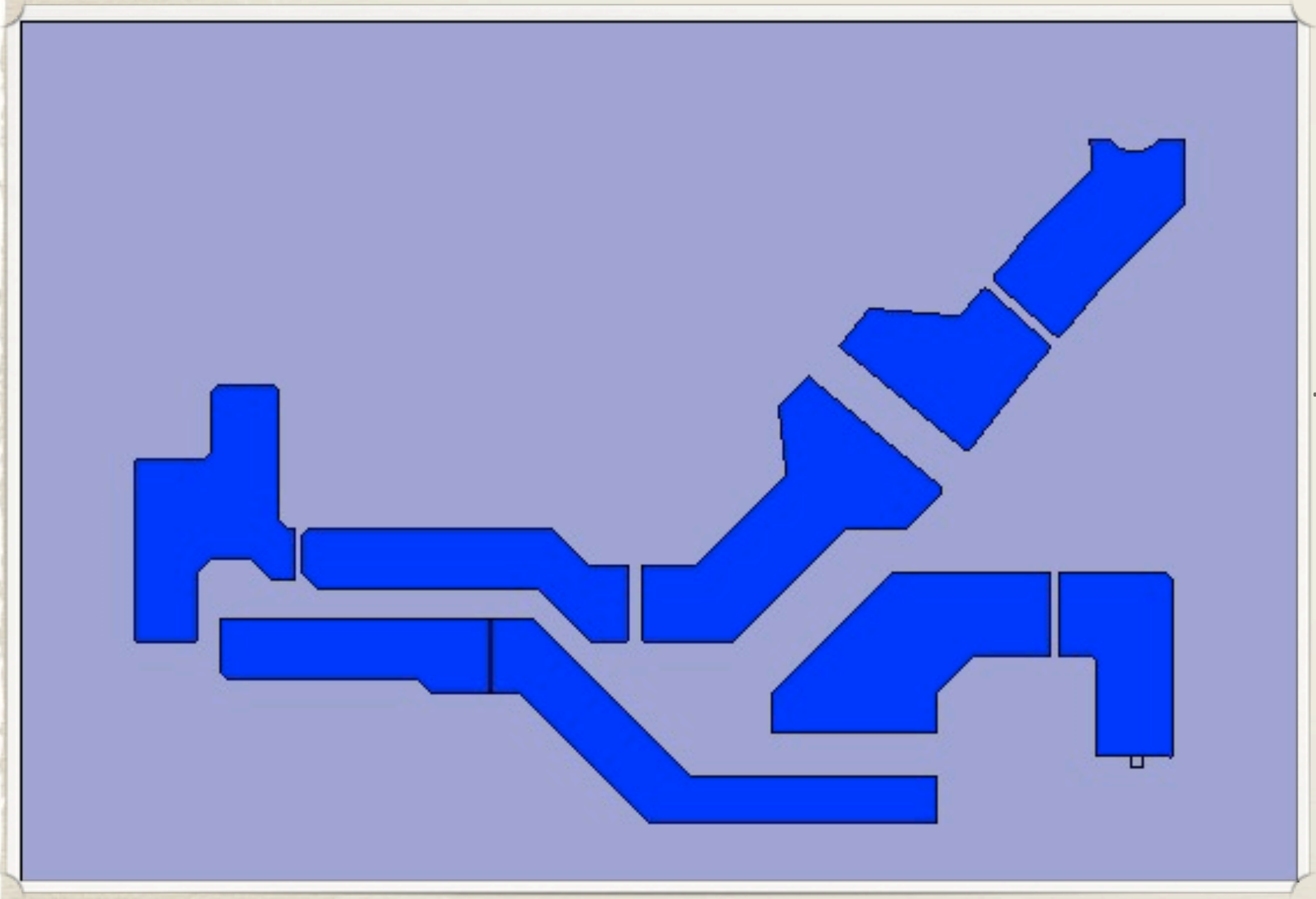
Mutual Inductance

Self Partial Inductance

$$Lr11_{NET} = Lr11_{SELF} - M11$$

The net inductance of a loop is the sum of its Net Partial Inductances

Estimating Inductance values



Softwares allow:

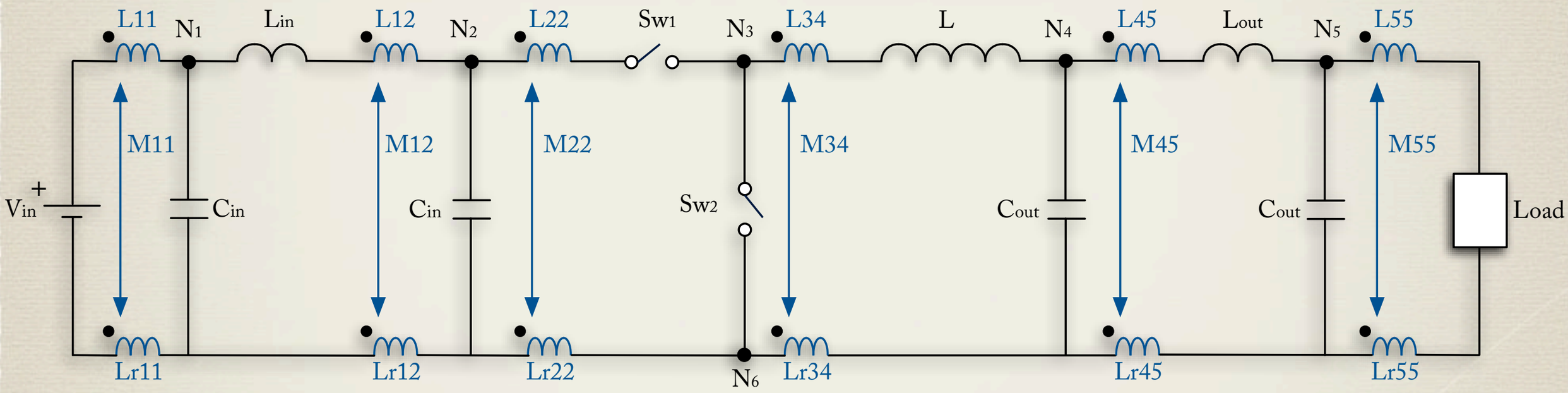
-Q3D (EM simulation):

- Extraction of self and mutual inductance values.

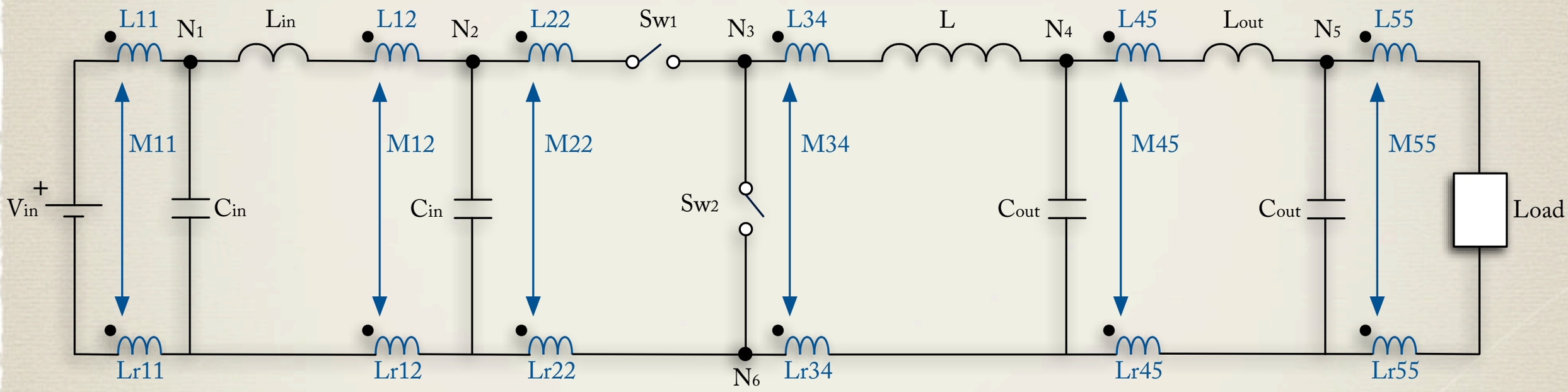
-Simplorer (circuit sim)

- Sweep their value through parametric simulations
- Identify the most critical inductances for the noise

Critical Inductances



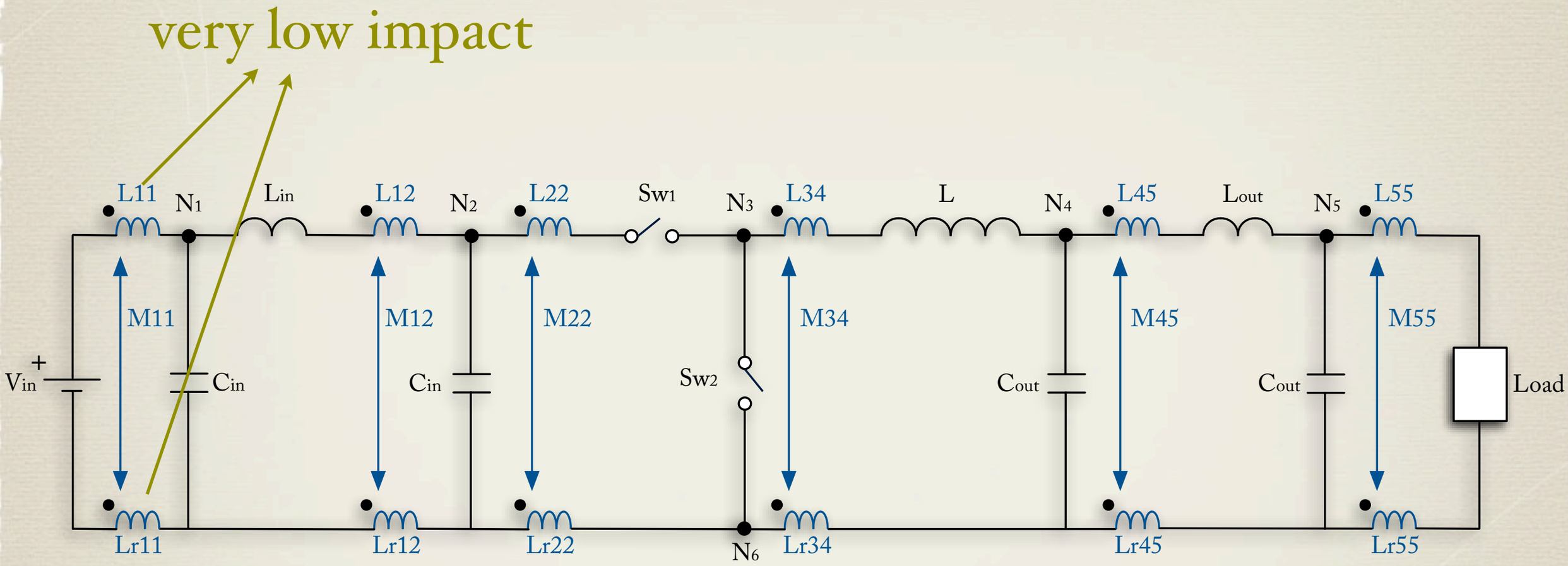
Critical Inductances



Lr22NET & Lr34NET big impact on CM noise

Critical Inductances

very low impact



$Lr22_{NET}$ & $Lr34_{NET}$ big impact on CM noise

Critical Inductances

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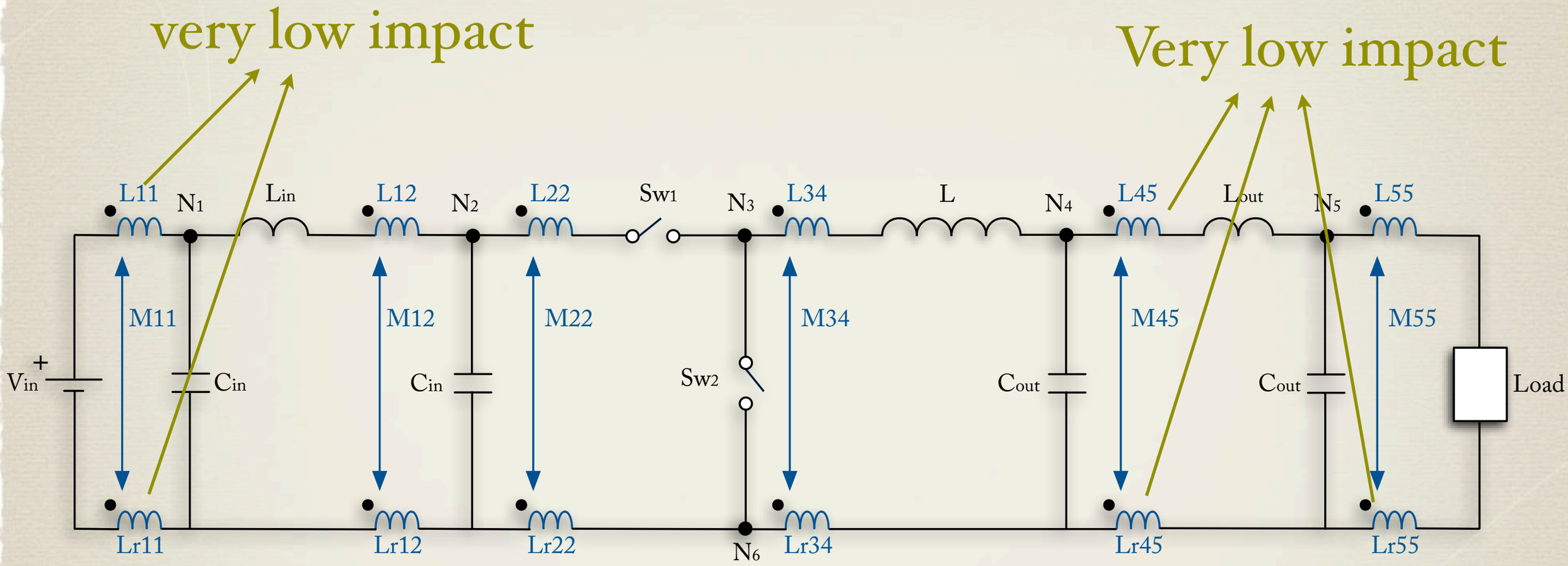
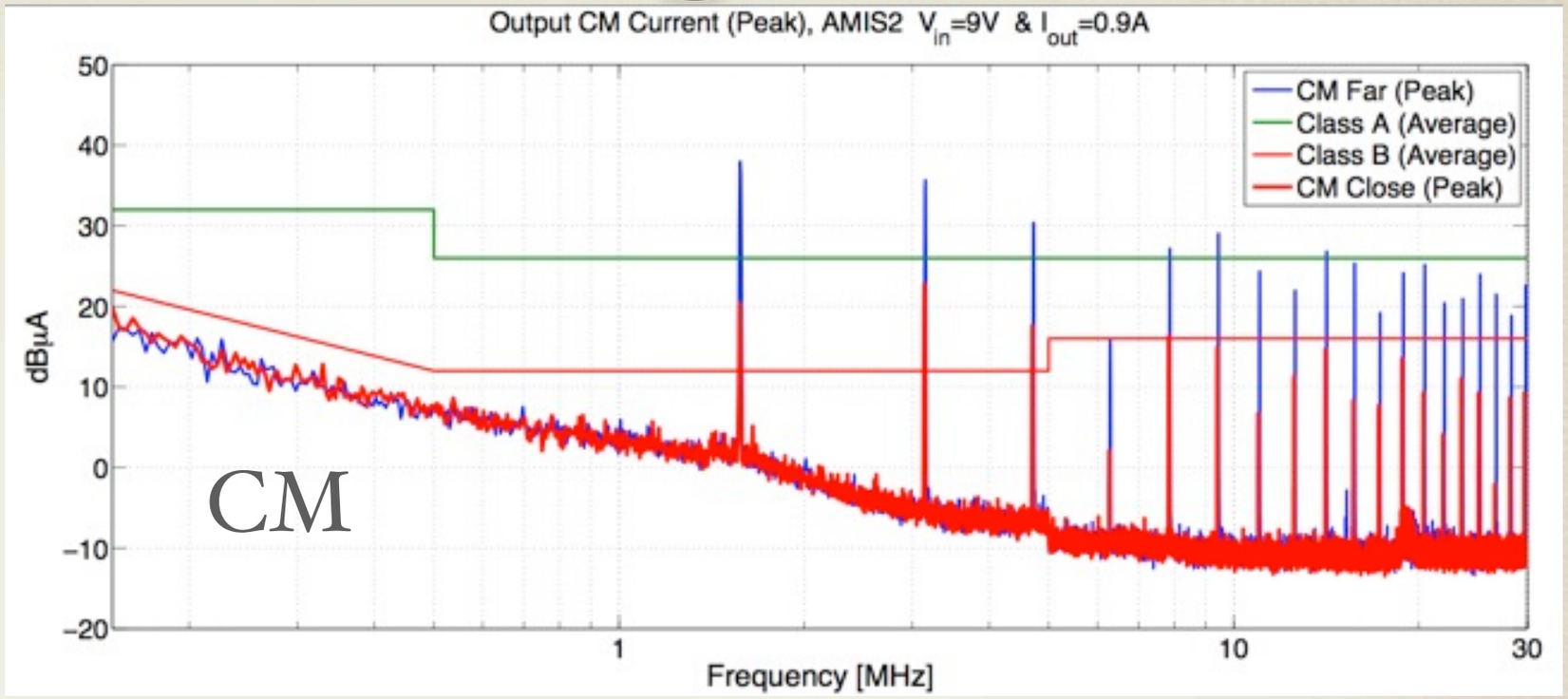
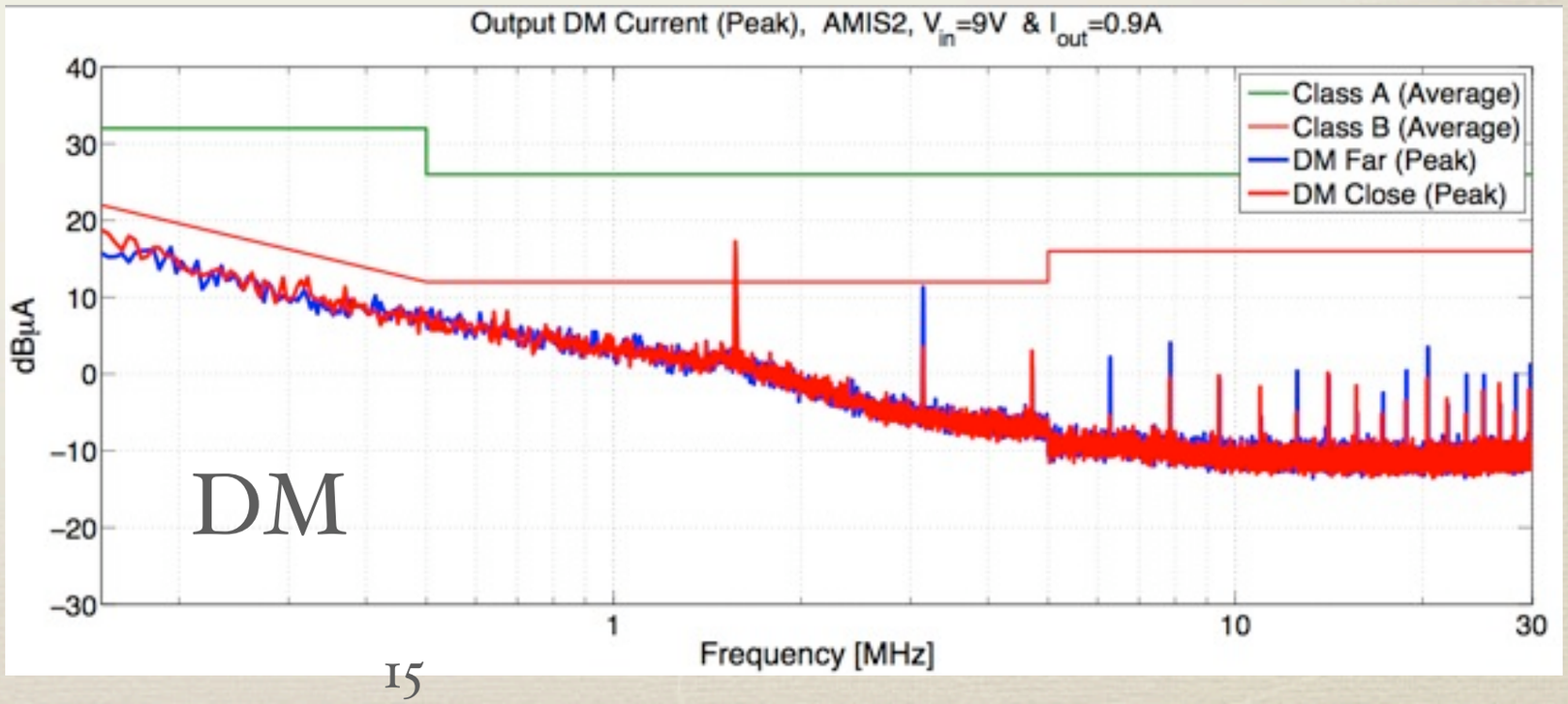
Very low impact



Lr22NET & Lr34NET big impact on CM noise

Ground bouncing and CM

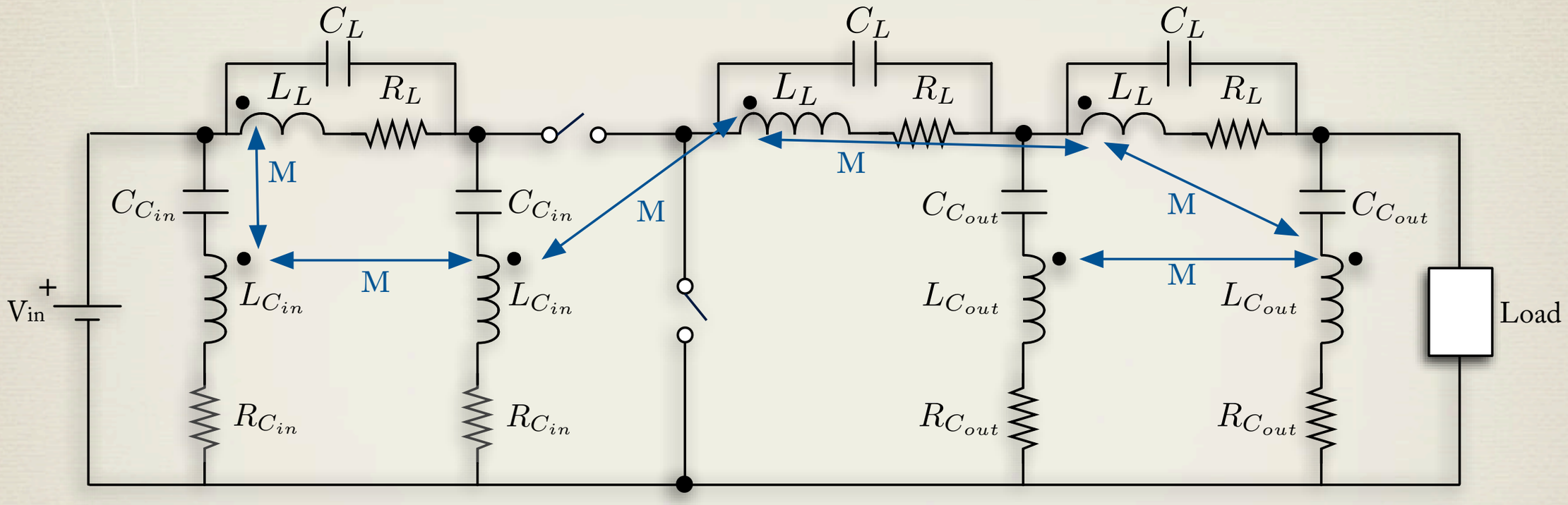




Third Design Considerations

- The return path plane should have the minimum inductance possible. For that, it is fundamental to use a dedicated solid copper layer for return currents. This layer should be as solid as possible.
- Reducing the PCB thickness has a good impact on reducing the Net partial inductance and loop inductance, as it augments the mutual inductance.
- The decoupling capacitor must be as close as possible from switches or ASIC.
- Try to place vias for the control signal out of the path of the power current.

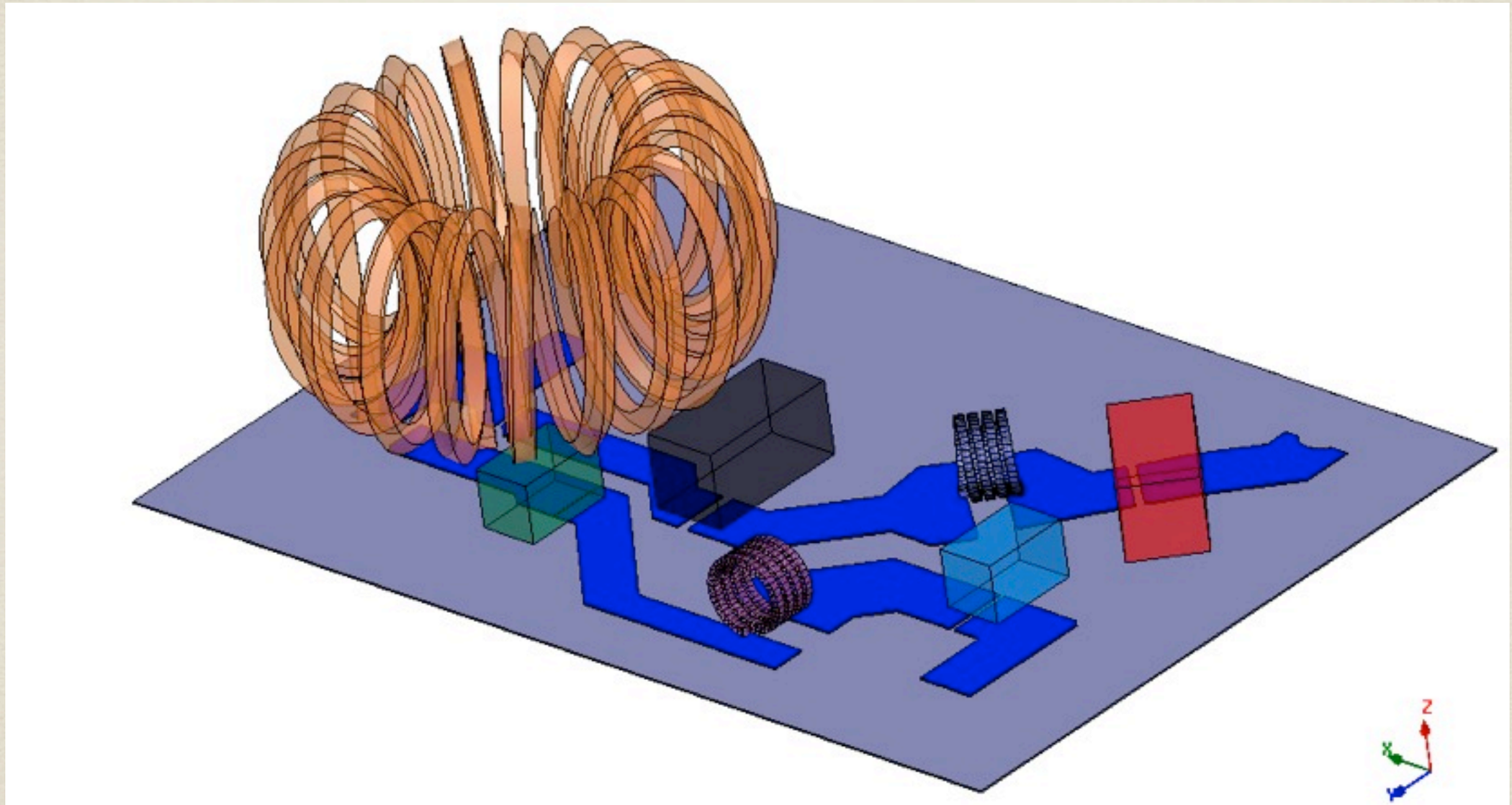
4º Component's couplings



Passive components are magnetically coupled between each other

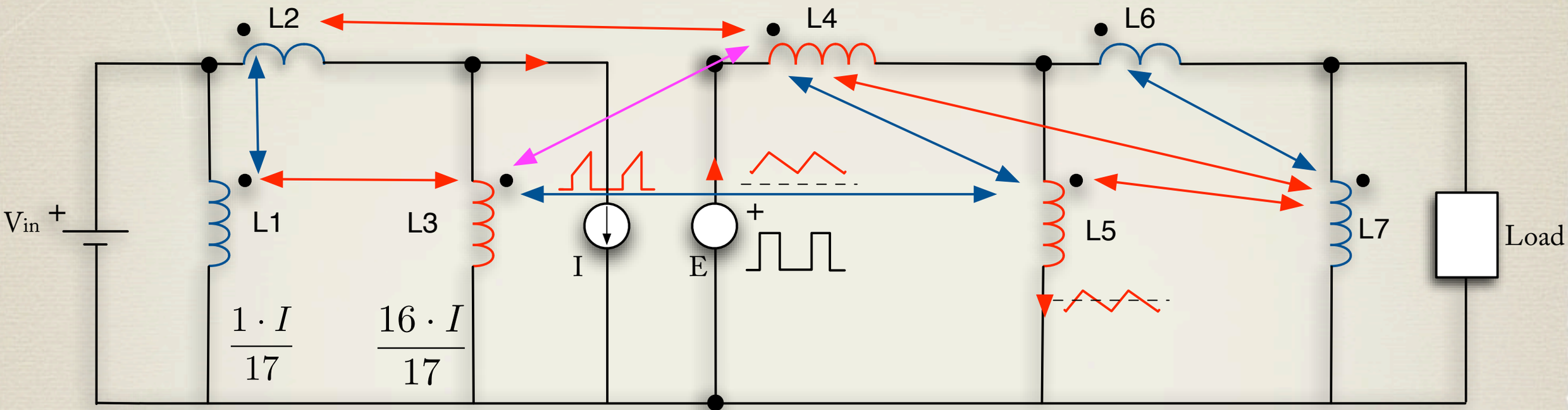
Not all the couplings included in the drawing for simplicity

Obtaining coupling values



Nº of couplings: $\binom{7}{2} = 21$ for 7 different components

Important parameters



Noisy components L3 L4 L5

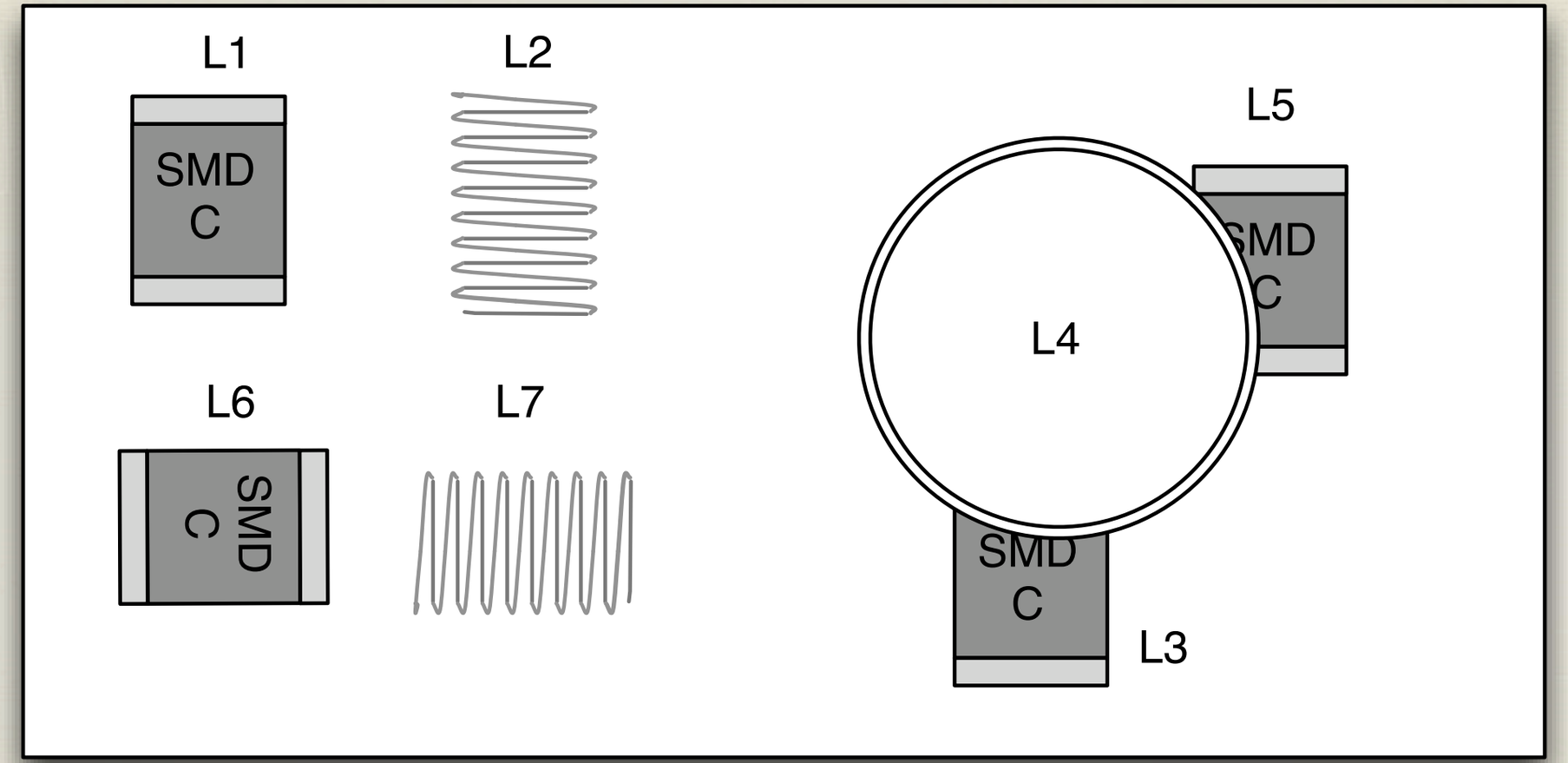
Susceptible components L1 L2 L6 L7

- Couplings between susceptible components are not an issue.
- Couplings between noisy components could have impact
- Couplings between noisy and susceptible components must be avoided. (principally with L4)

Fourth Design Considerations

- Minimize coupling with main inductor L4. (Topology and shield)
- Minimize coupling between noisy and susceptible components. (segregation helps)
- Just like the main inductor, the loop between the MOSFET and decoupling capacitors will emit magnetic field due to the large di/dt input current. Reduce the size of this loop.
- Avoid couplings between susceptible components of different filters (input/output).

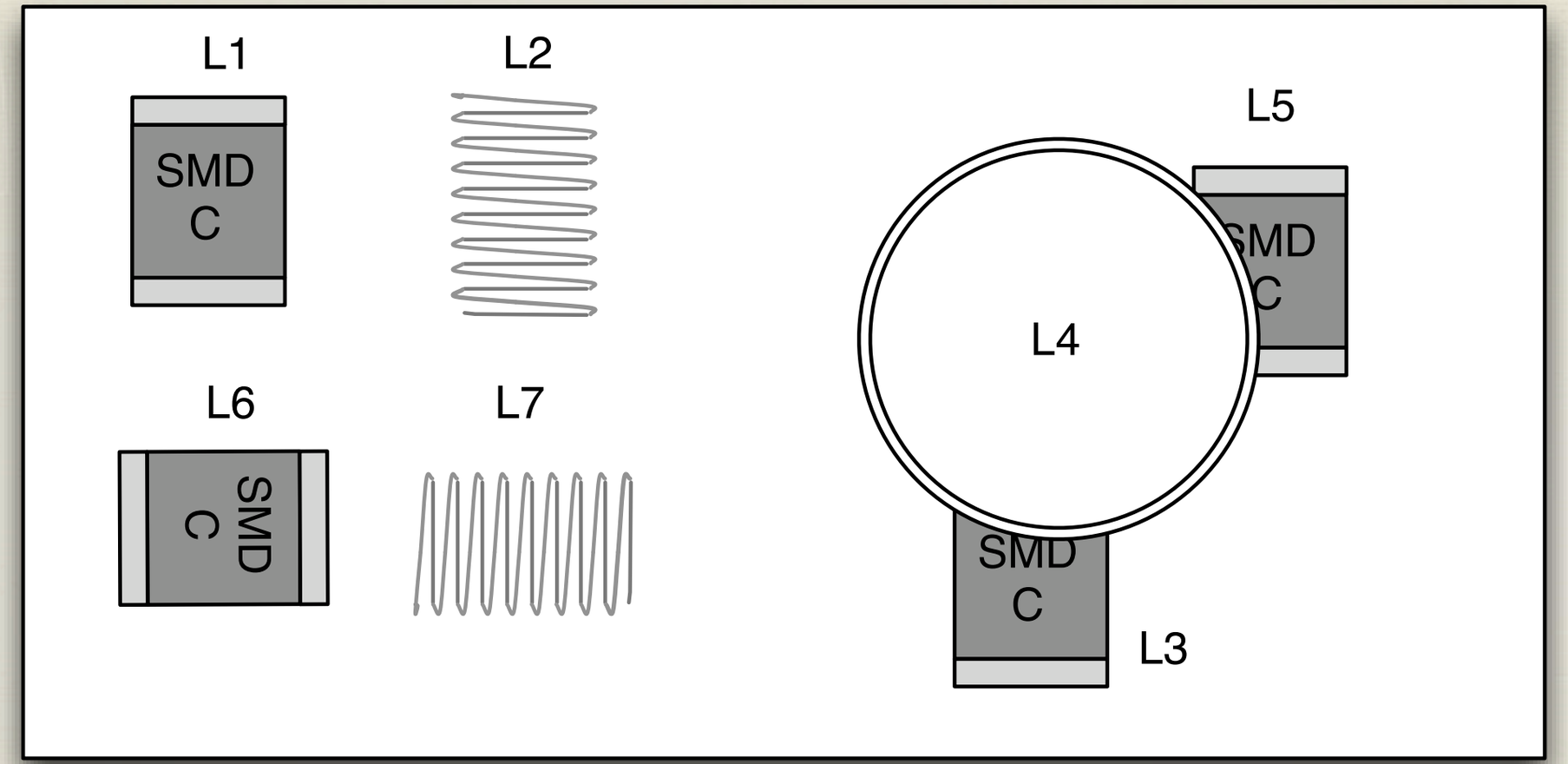
Segregation & Shielding



Quiet components

Noisy components

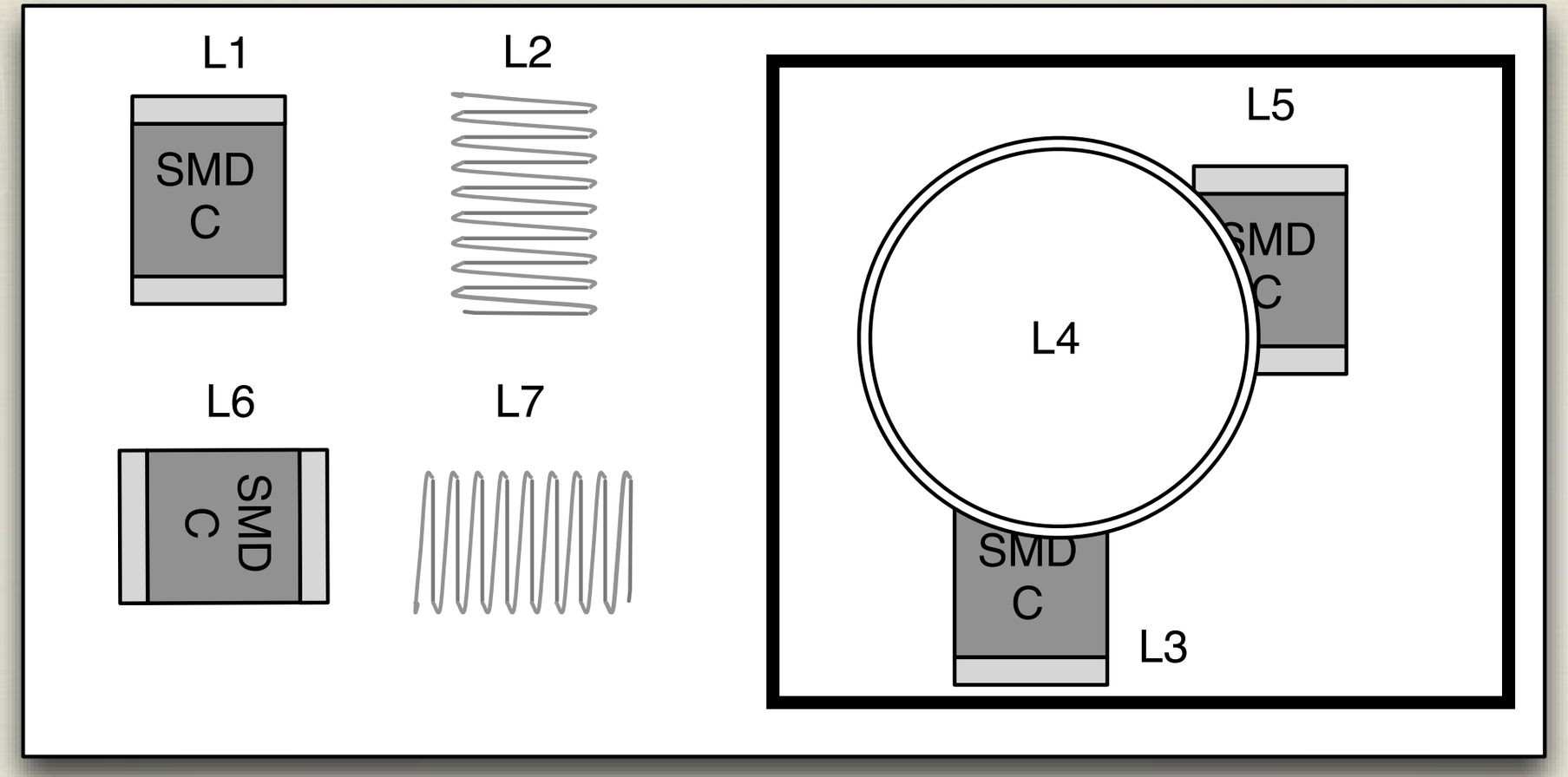
Segregation & Shielding



Quiet components Noisy components

Physical segregation and correct orientation of components have a good impact, and can be improved by shielding the noisy part

Segregation & Shielding



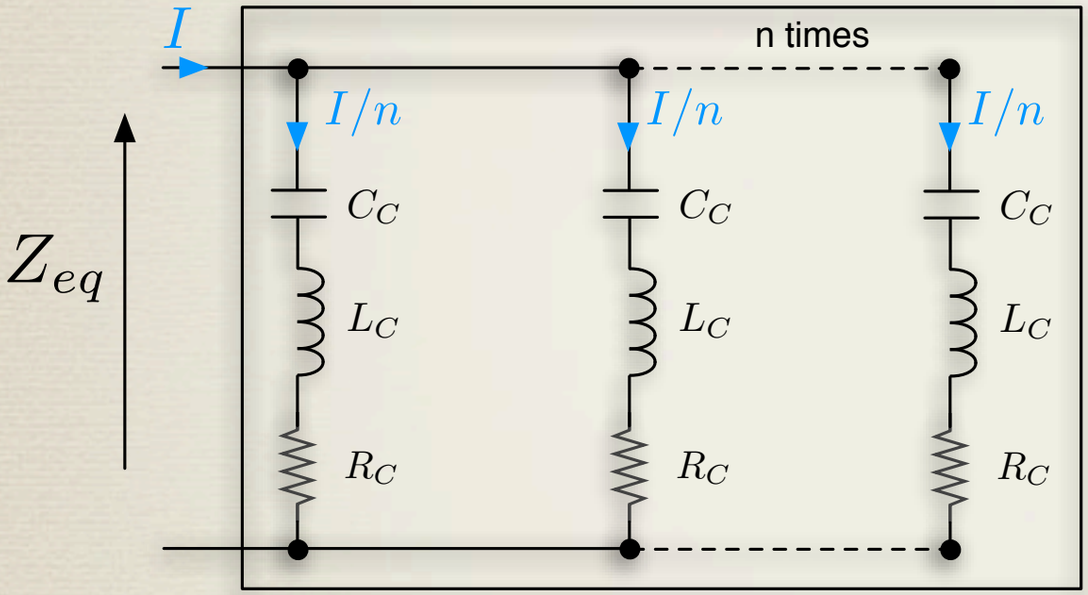
Quiet components

Noisy components

Physical segregation and correct orientation of components have a good impact, and can be improved by shielding the noisy part

Multiple decap of same value in parallel

If same value, they share the same current

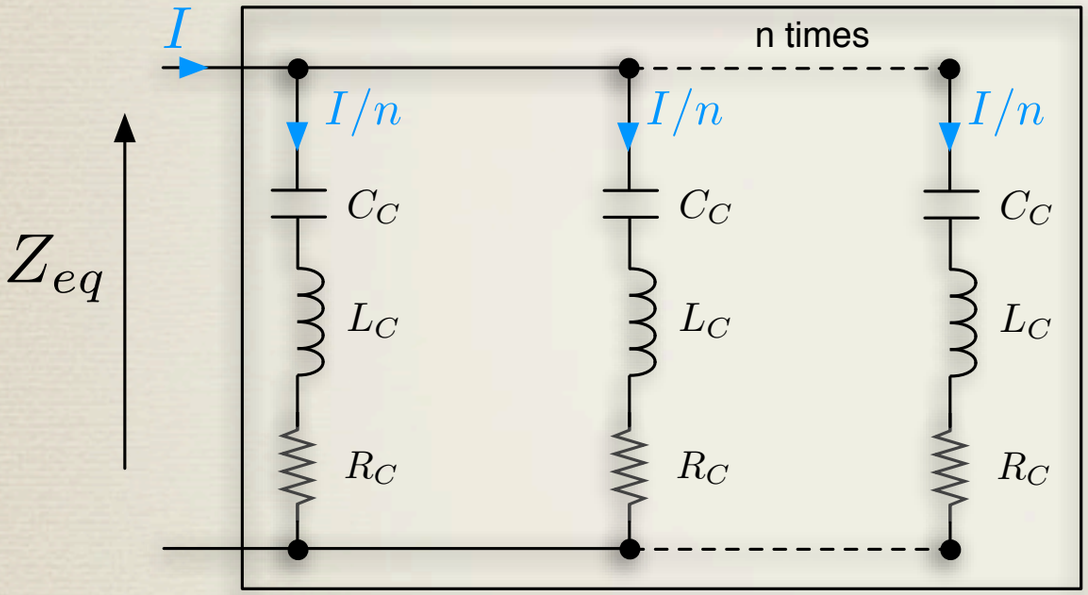


$$Z_{eq} = \frac{1}{jw(nC)} + jw\frac{L}{n} + \frac{R}{n}$$

C augments n times, while L & R decrease n times.

Multiple decap of same value in parallel

If same value, they share the same current

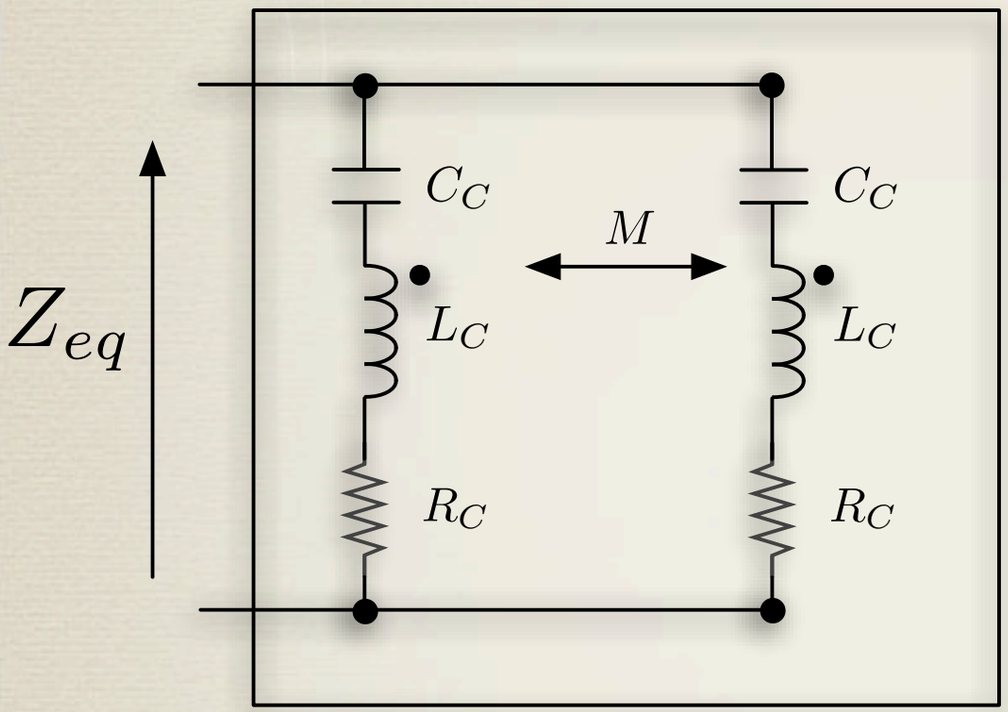


$$Z_{eq} = \frac{1}{jw(nC)} + jw\frac{L}{n} + \frac{R}{n}$$

C augments n times, while L & R decrease n times.

This is partially true!! It is just applicable if there is no magnetic coupling between capacitors.

Two decap of same value in parallel



$$Z_{eq} = \frac{1}{jw(2C)} + jw\frac{(L+M)}{2} + \frac{R}{2}$$

The equivalent inductance depends of the coupling, as was stated before.

$$L_{eq} = \frac{(L+M)}{2}$$

Where $M = k\sqrt{L_c \cdot L_c} = k \cdot L_c$ & $-1 \leq k \leq 1$

If k=0

$$L_{eq} = \frac{L}{2}$$

If k=1

$$L_{eq} = L$$

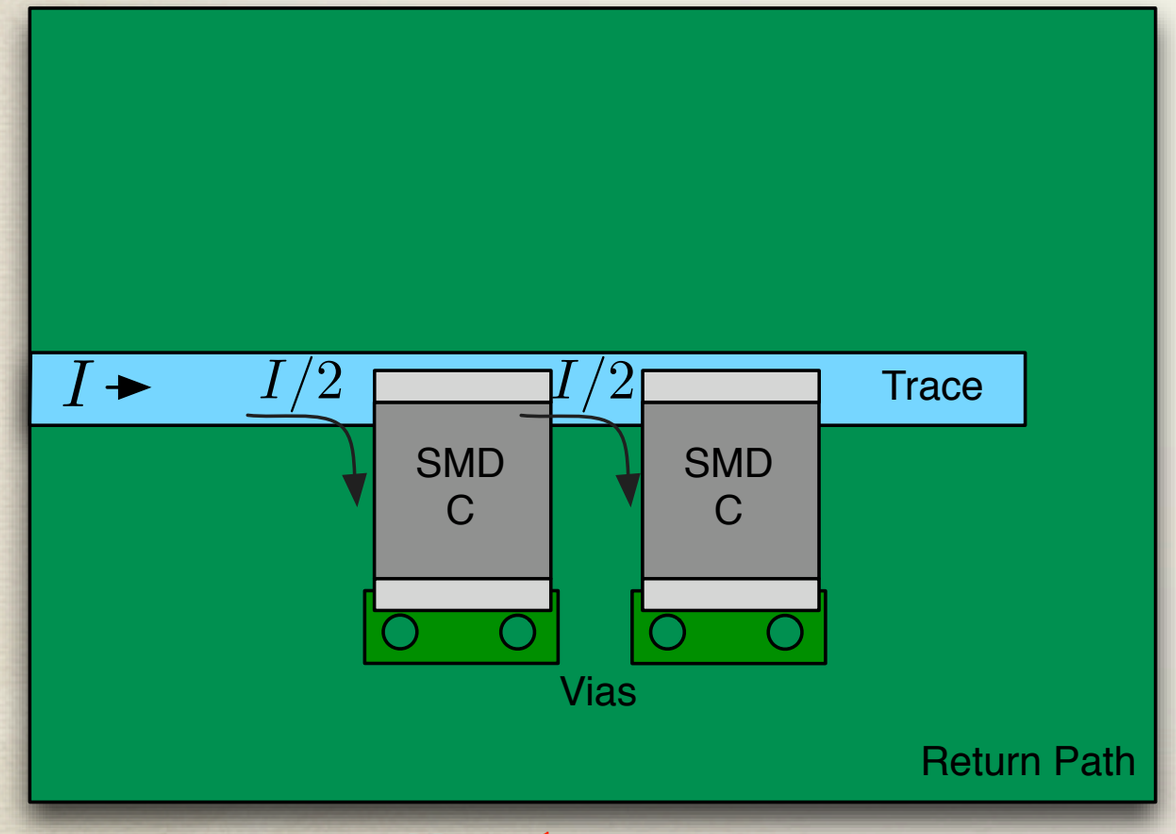
If k=-1

$$L_{eq} = 0$$

Two decap of same value in parallel

Case a) k is close to 1

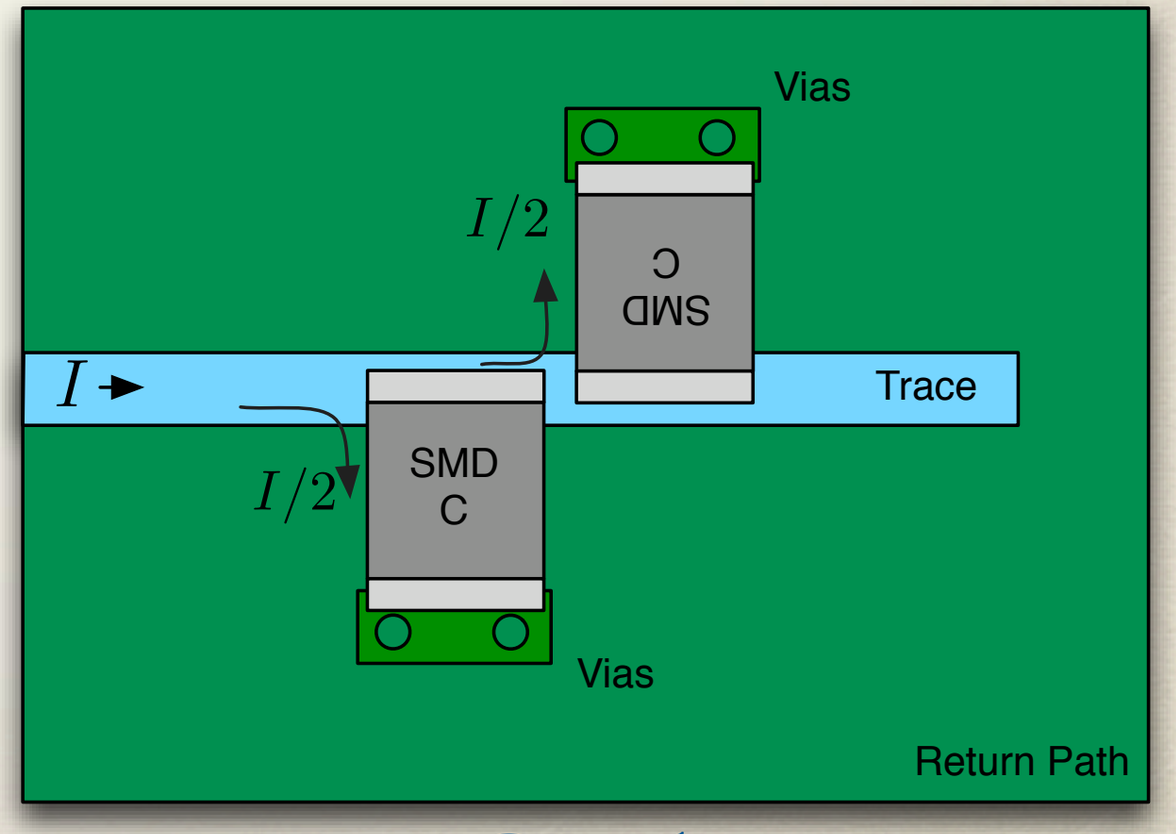
$$L_{eq} = L$$



Bad

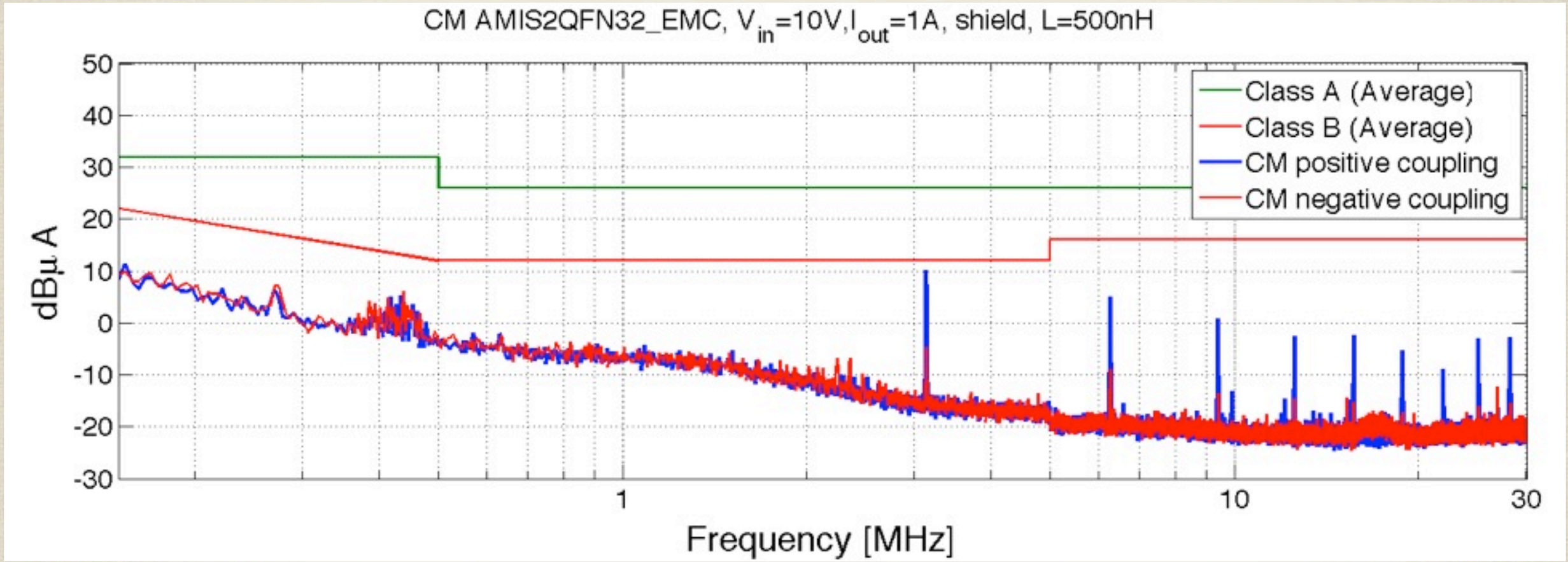
Case b) k is close to -1

$$L_{eq} = 0$$



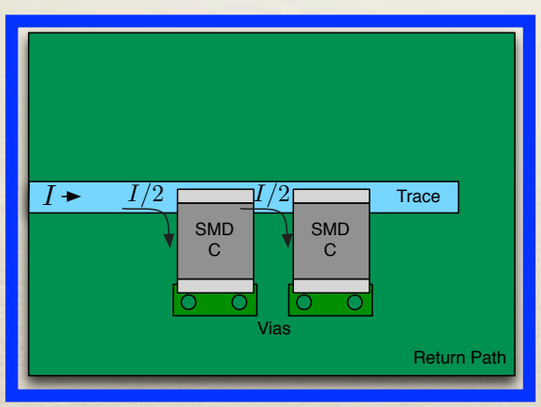
Good

Impact of decap orientations on CM



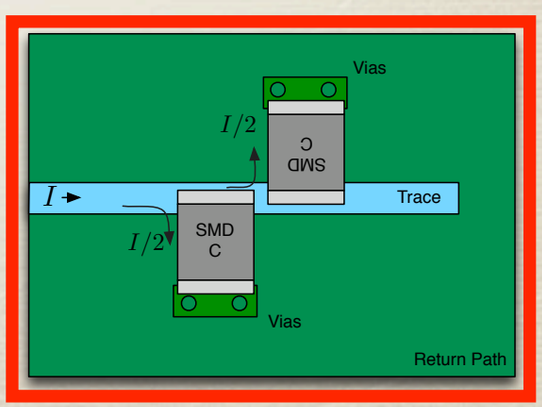
Case a) k is close to 1

$$L_{eq} = L$$



Case b) k is close to -1

$$L_{eq} = 0$$



Thanks for your attention

Acknowledgment

C. Fuentes is supported by MECESUP-Chile under grant FSM0601

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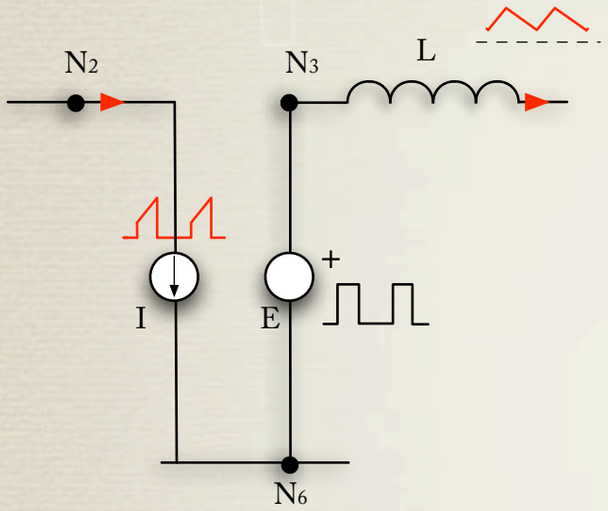
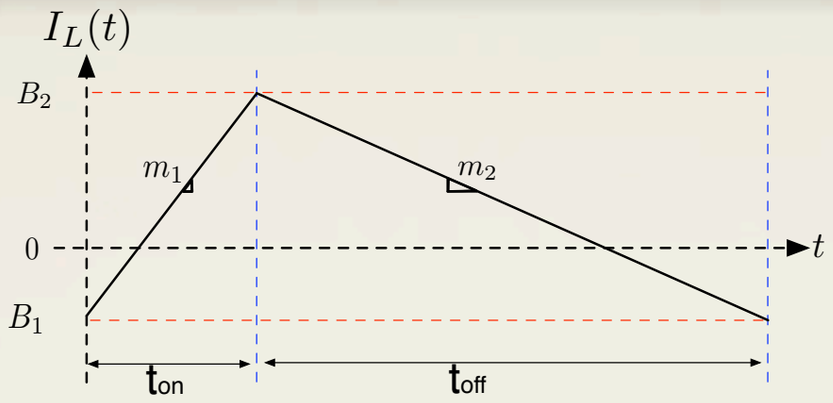
"VALPARAISO CENTER FOR SCIENCE AND TECHNOLOGY"

BACKUP SLIDES

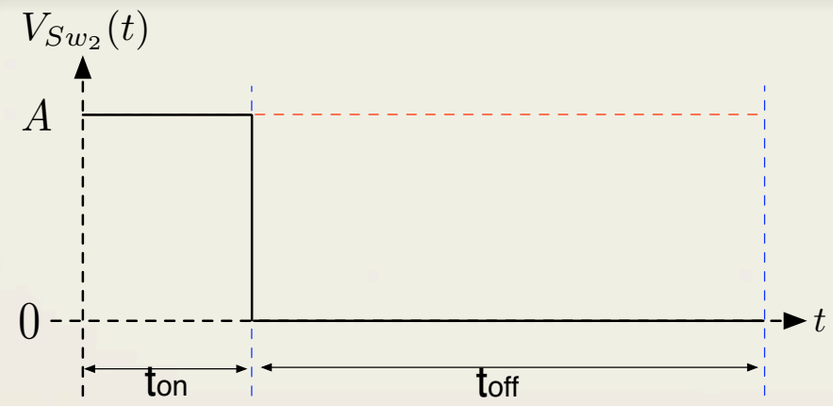
Sources of noise



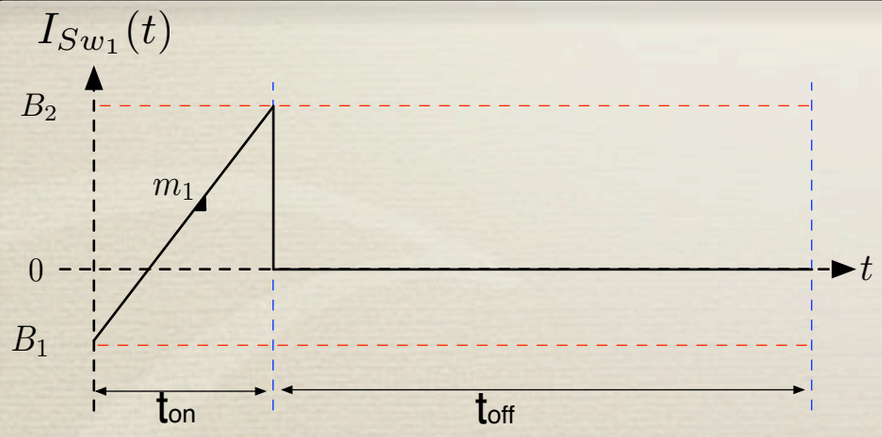


$$c_n = \frac{1}{jn\omega_s}\left[\frac{m_1 - m_2}{jn\omega_s T}(1 - e^{-jn\omega_s t_{on}})\right]$$

$$m_1 > 0 \qquad m_2 < 0$$

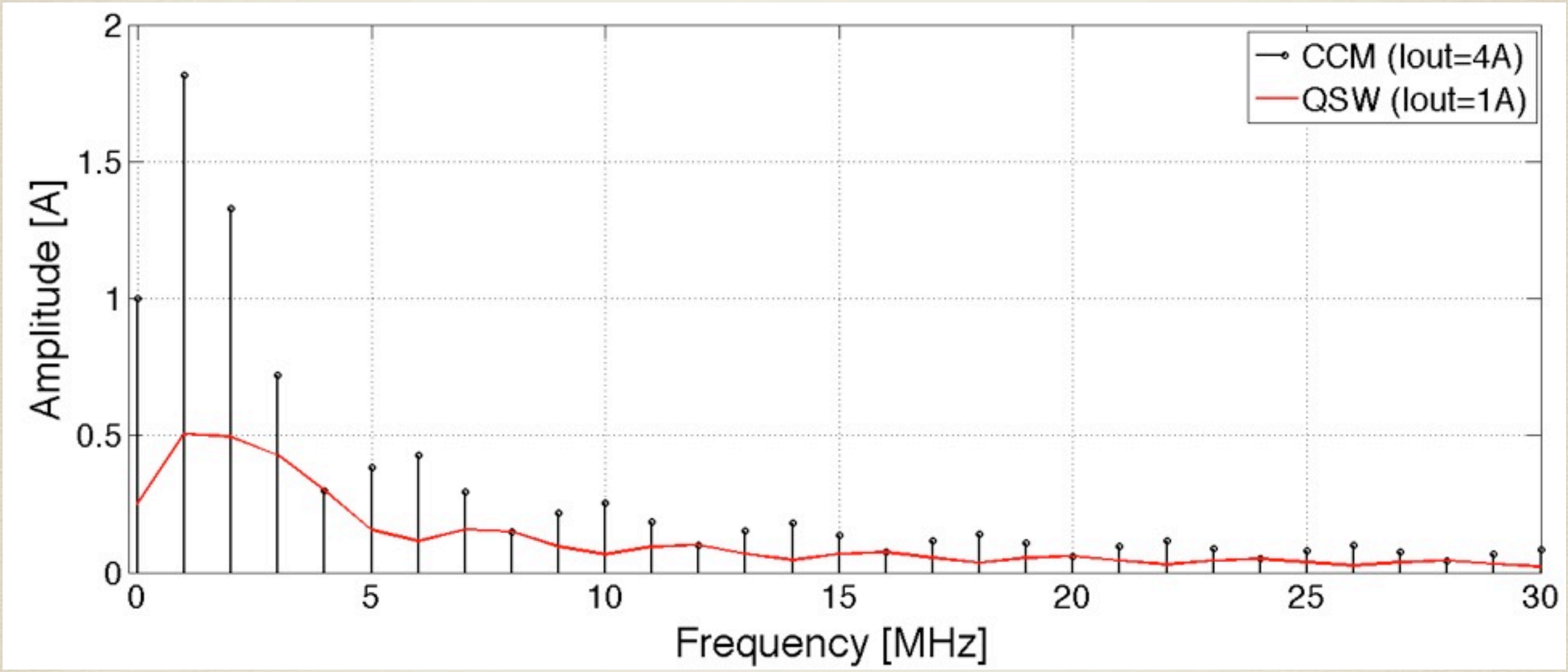


$$c_n = \frac{A}{jn\omega_s T}(1 - e^{-jn\omega_s t_{on}})$$



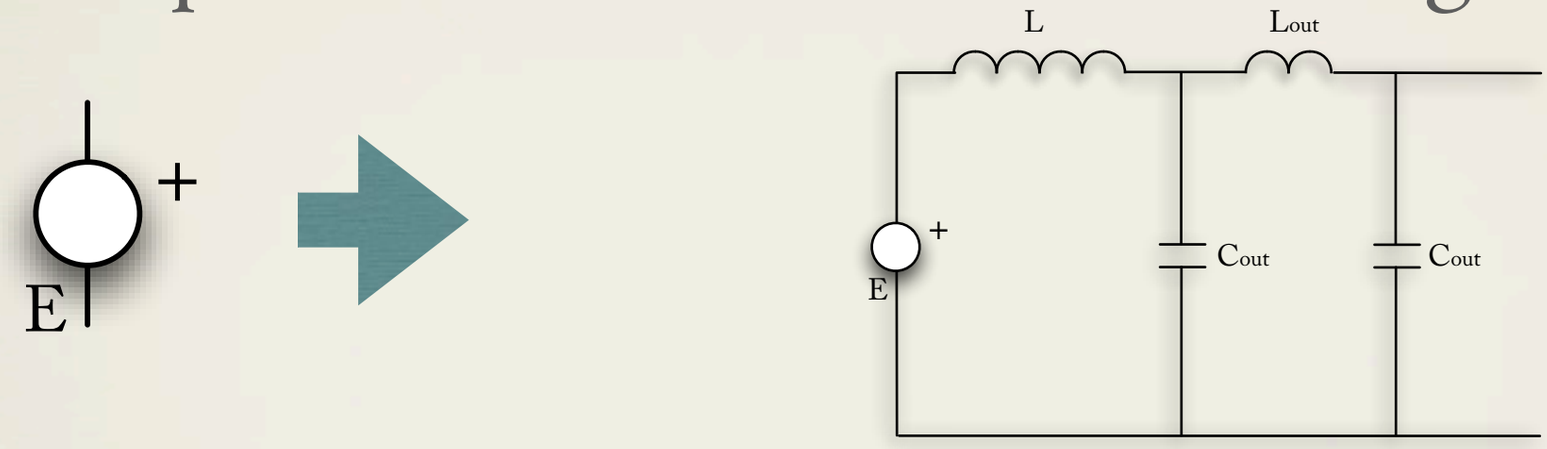
$$c_n = \frac{1}{jn\omega_s}\left[\frac{m_1}{jn\omega_s T}(1 - e^{-jn\omega_s t_{on}}) + \frac{B_1}{T} - \frac{B_2}{T}e^{-jn\omega_s t_{on}}\right]$$

CCM vs QSW

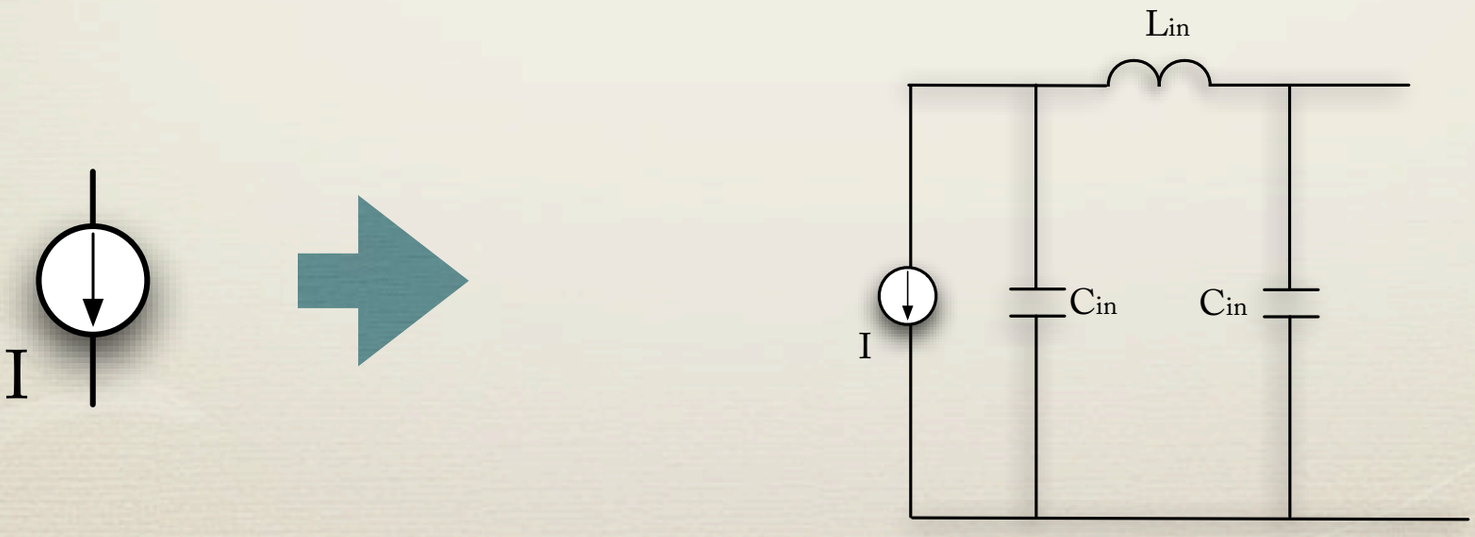

CCM (Iout=4A)
QSW (Iout=1A)
Amplitude [A]
Frequency [MHz]
0
0.5
1
1.5
2
0
5
10
15
20
25
30

Filtering strategies

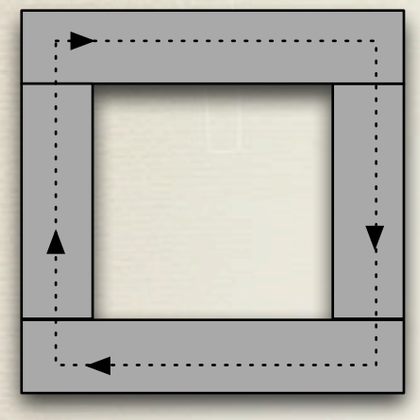
* Low Impedance source of noise (as Voltage sources)

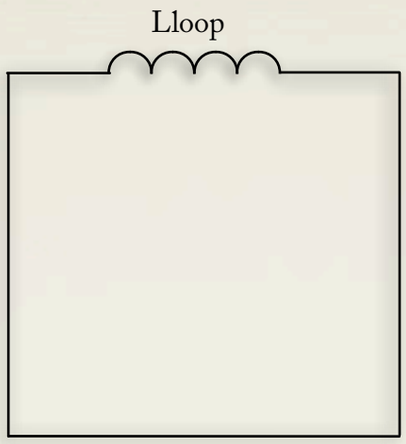


* High Impedance source of noise (as current sources)

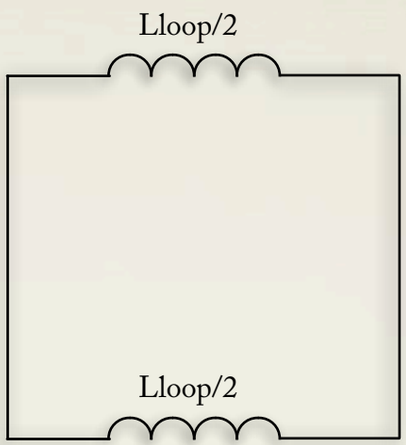


Loop and partial inductance

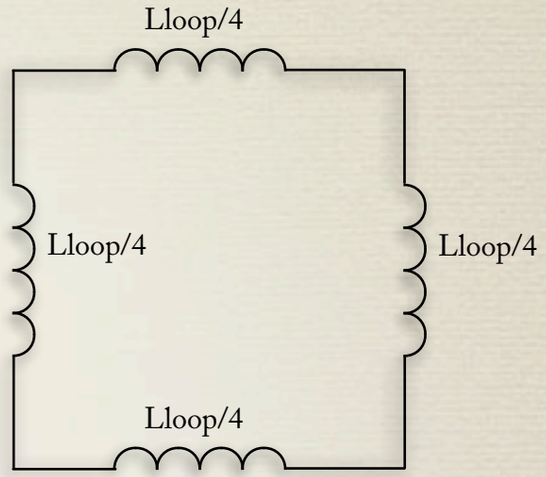




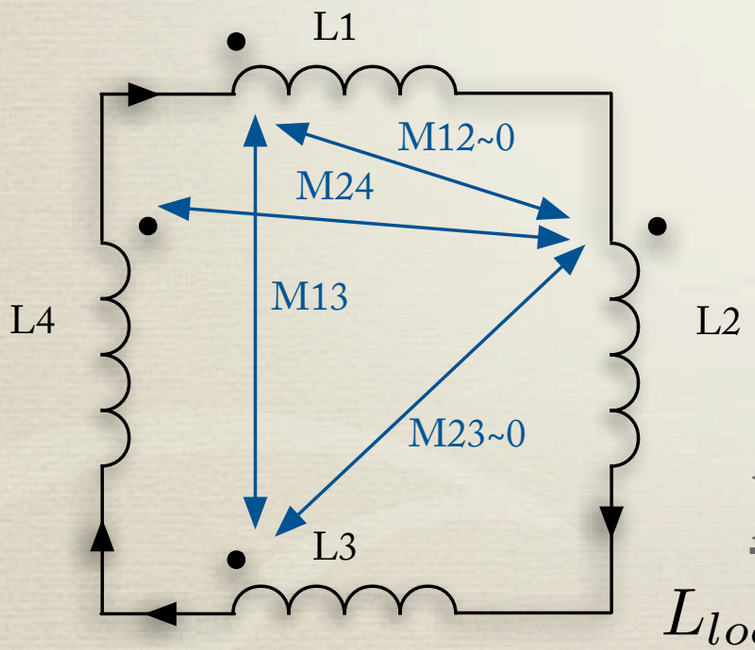
or



or



Partial inductance concept is needed, allowing us to define a unique inductance associated with only part of the loop.



Self Partial Inductance

$$L_1, L_3, L_2, L_4$$

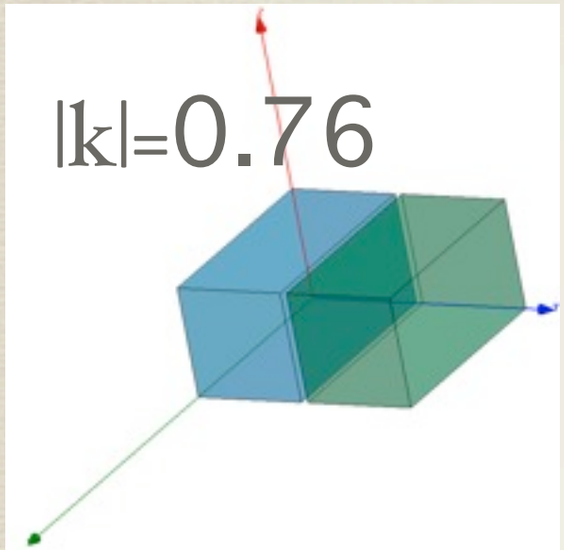
Net Partial Inductance

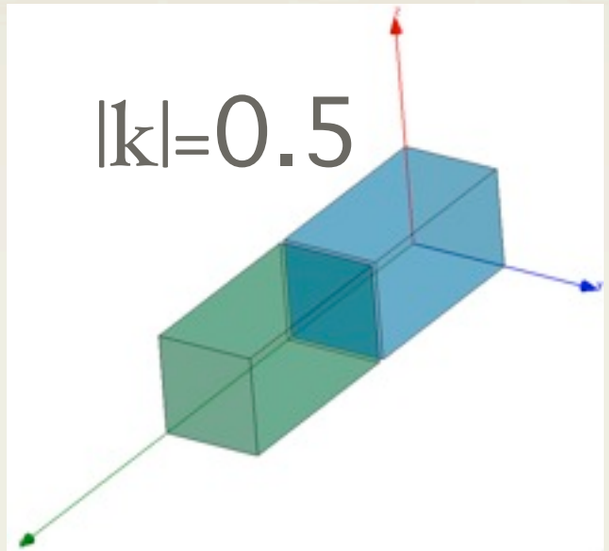
$$(L_1 - M_{13}), (L_3 - M_{13}), (L_2 - M_{24}), (L_4 - M_{24})$$

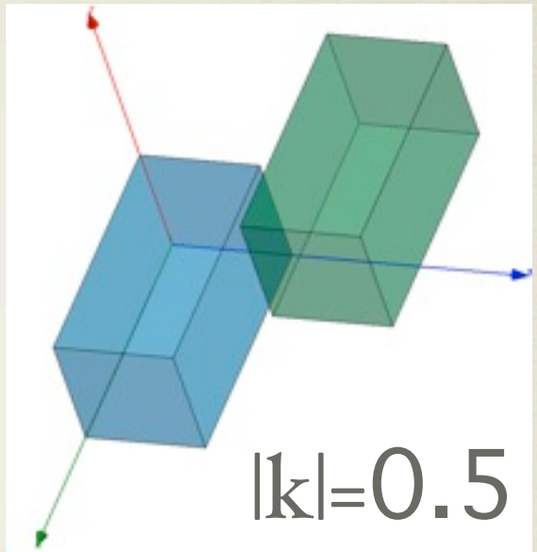
Loop is the sum of Net Partial Inductances

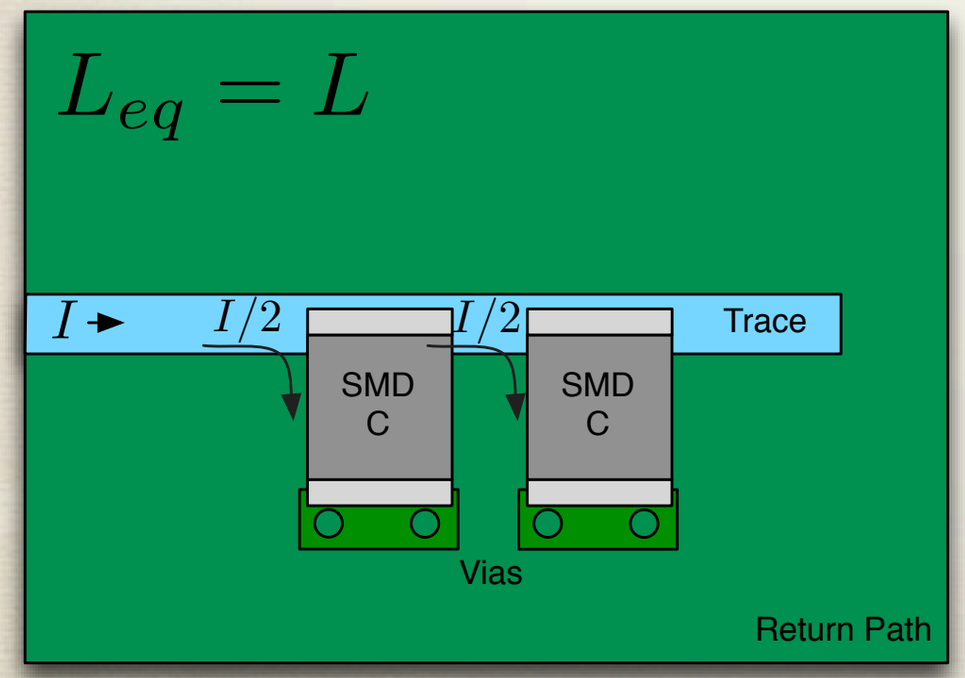
$$L_{loop} = (L_1 - M_{13}) + (L_3 - M_{13}) + (L_2 - M_{24}) + (L_4 - M_{24})$$

k factor for some cases

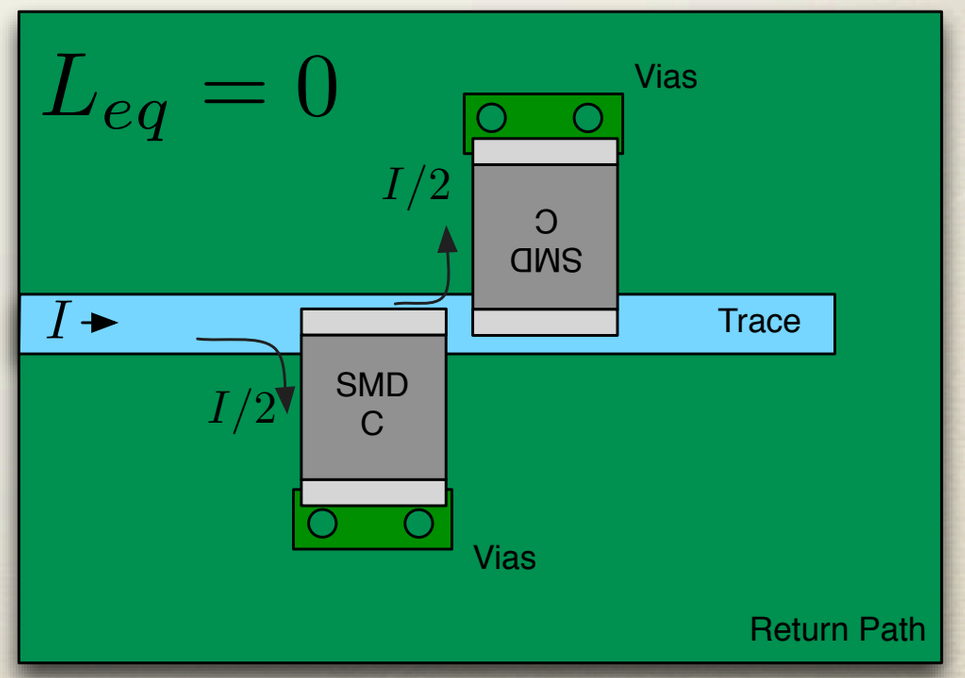






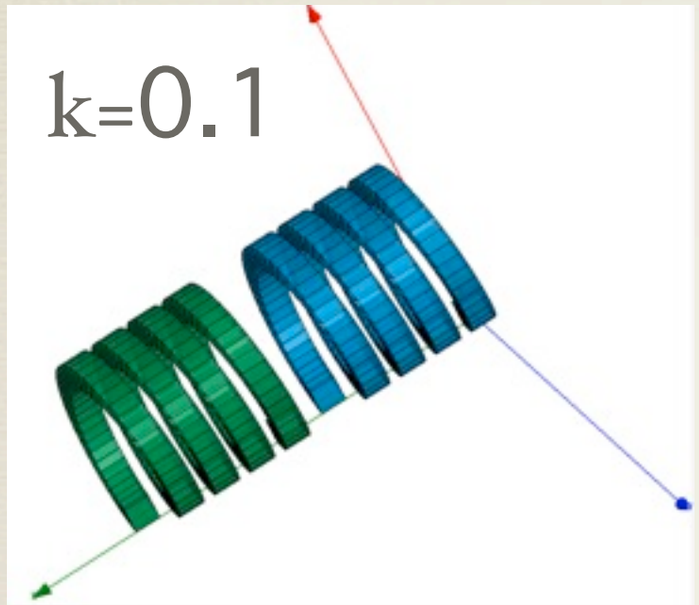


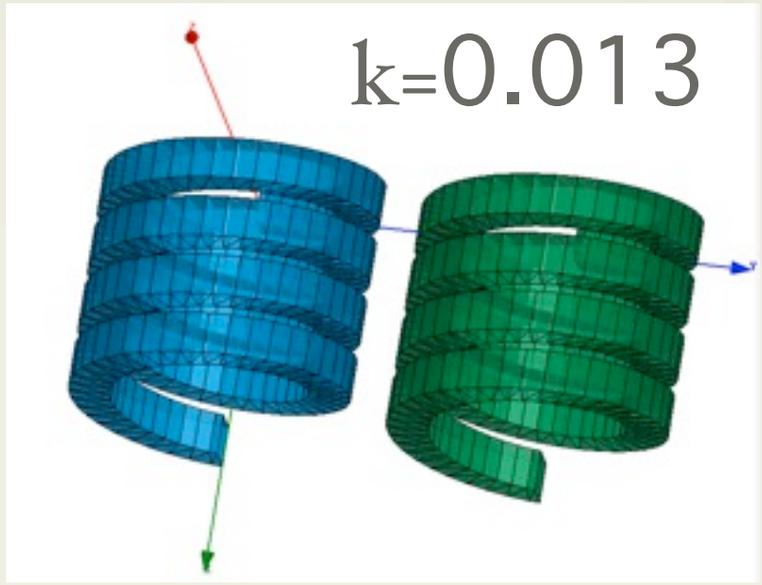
No worth it

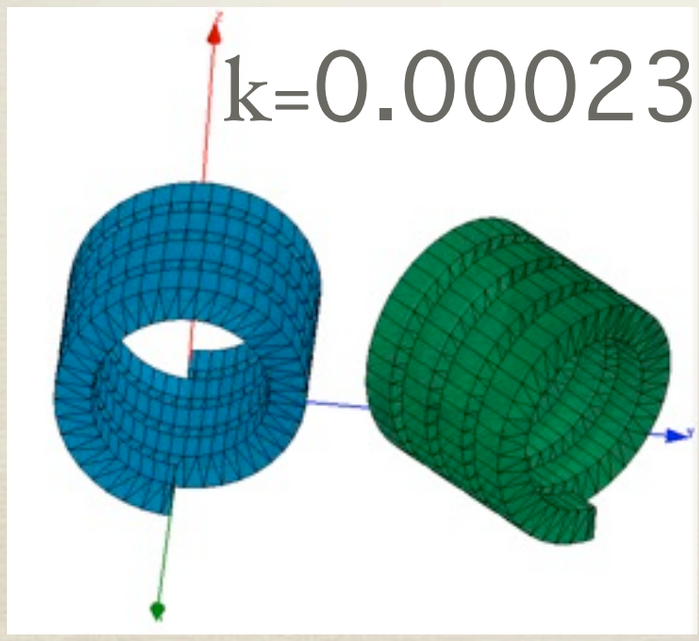


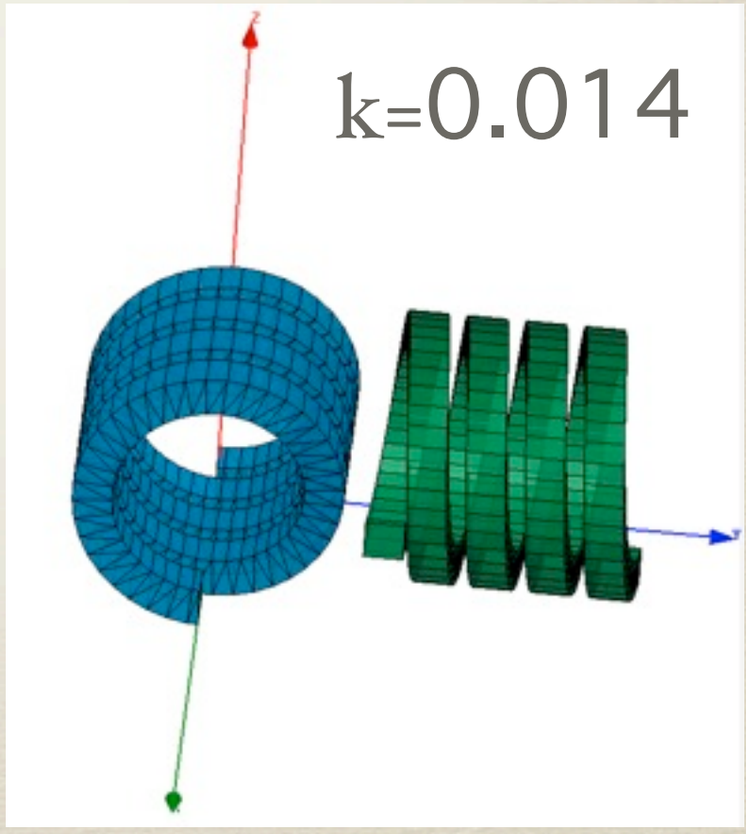
Worth it

Inductor Couplings

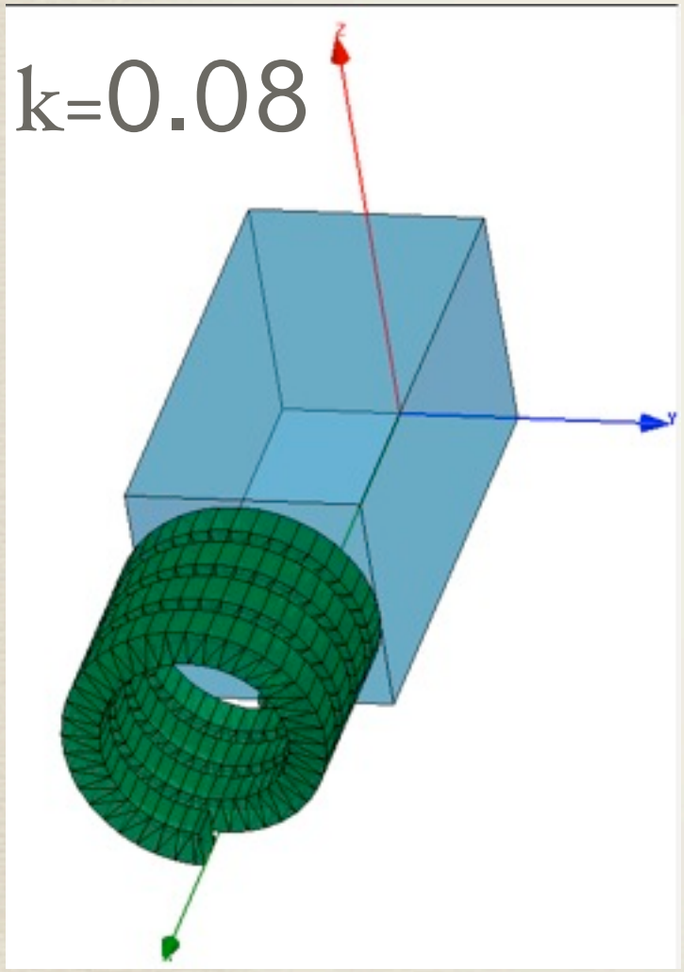


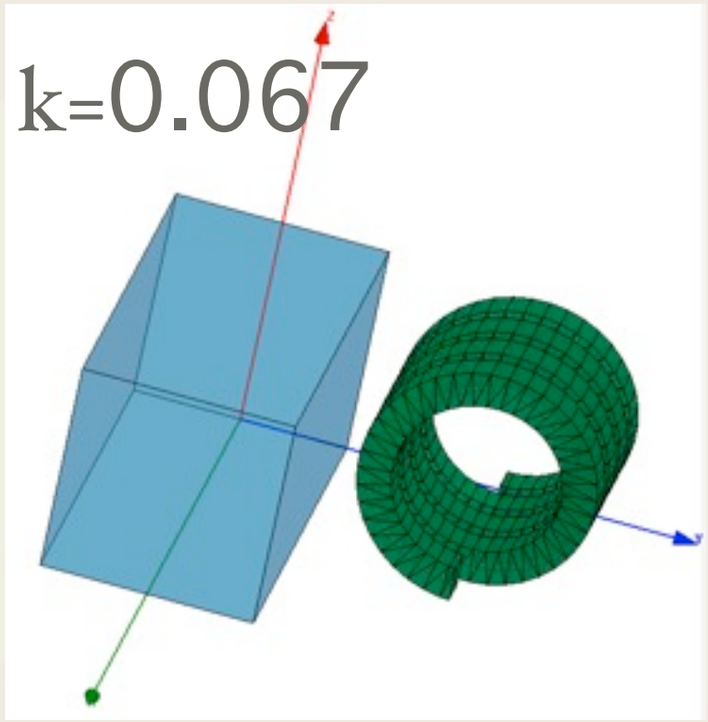


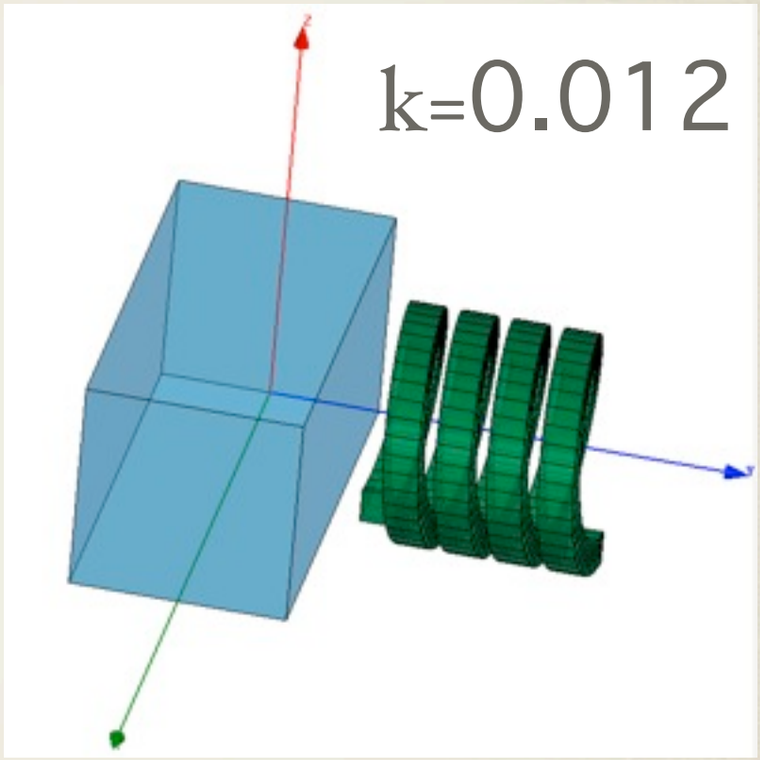




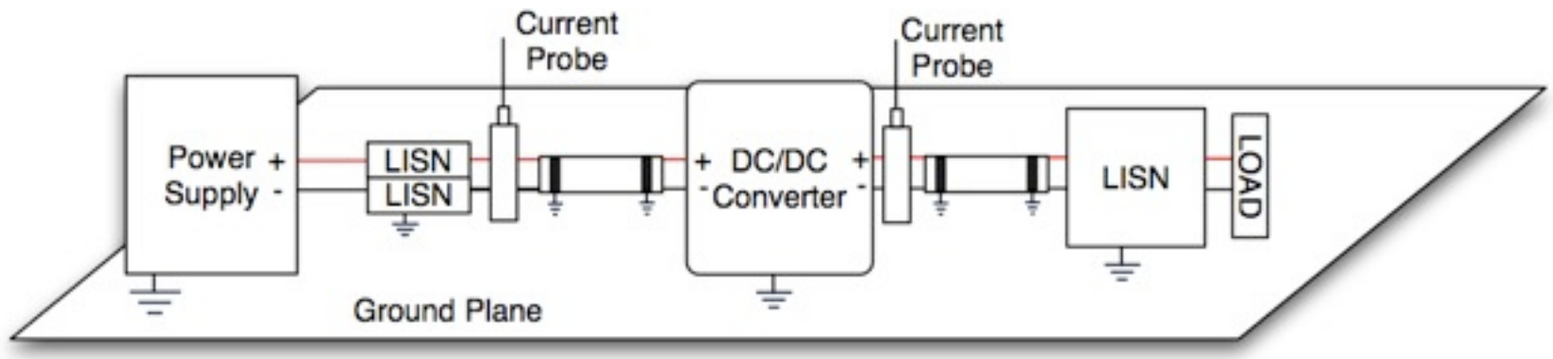
Inductor/Cap coupling

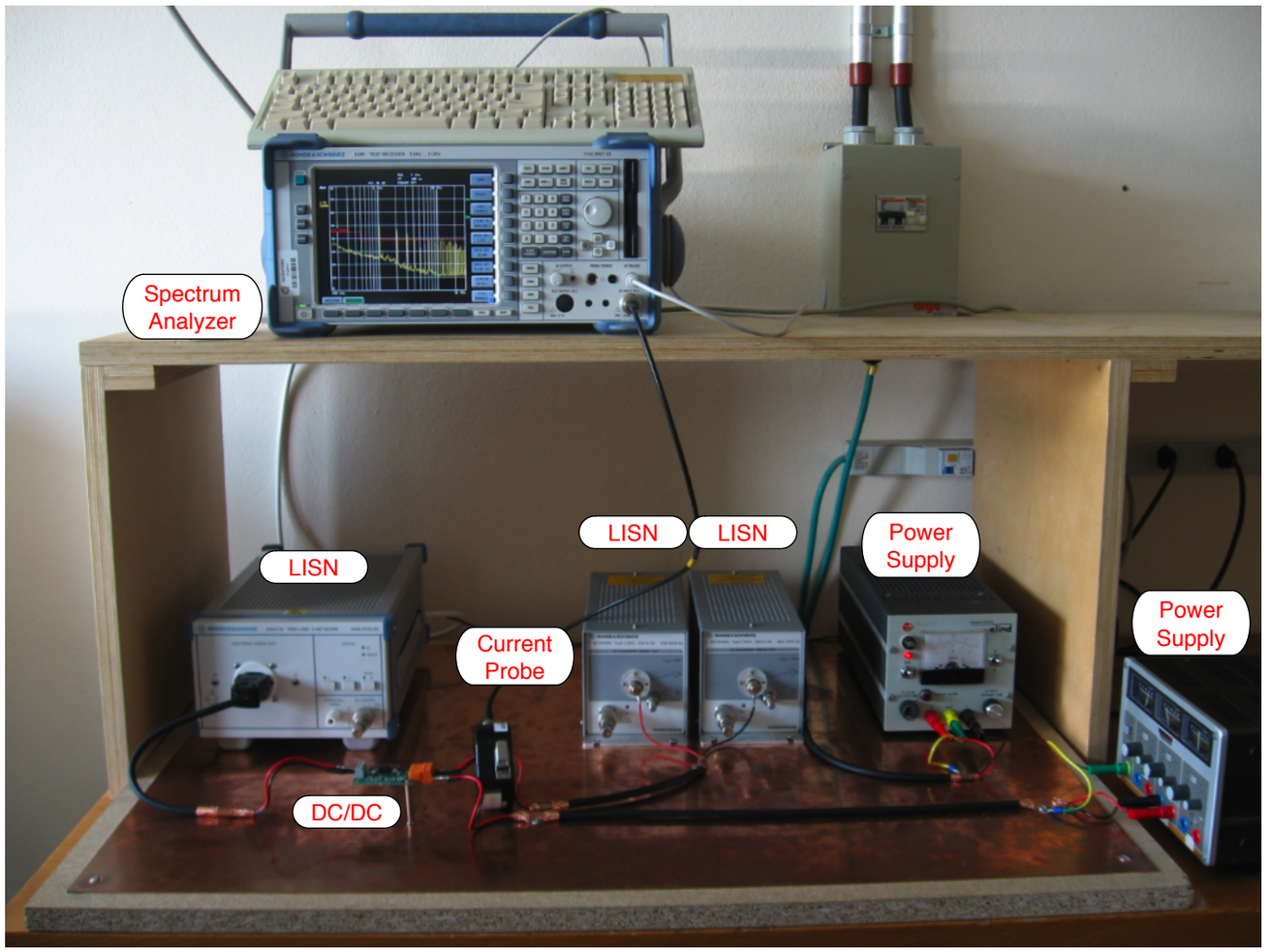






Measurement conducted EMI





Measurement conducted EMI