ATLAS IBL: Integration of new HW/SW readout features for the additional layer of Pixel Detector

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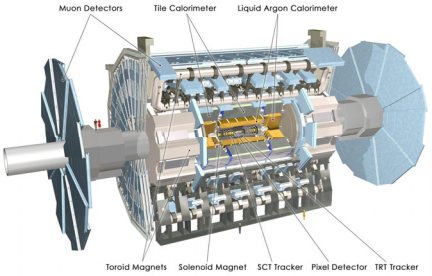
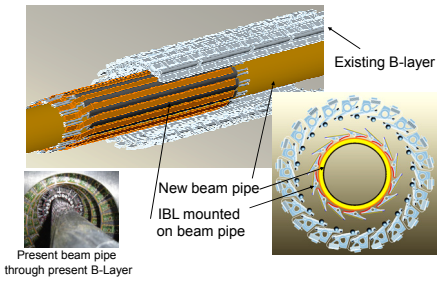
Introduction

An additional inner layer for the existing ATLAS Pixel Detector, called Insertable B-Layer (IBL), is under design and it will be installed by LHC-PHASE1. New front-end readout ASICs fabrication is ongoing and will replace the previous chips in this layer. The new system features higher readout speed - 160Mbit/s per ASIC - and simplified control. The current data acquisition chains are composed of front-end detectors, readout chips, Back-Of-Crate (BOCs) cards and ReadOut Driver cards (RODs). The paper presents a proposal for the new ROD board, which implements modern FPGAs and high-speed links with the detector and with the ATLAS DAQ system.



ATLAS Inner Detector:
- 3 sub-systems: TRT, SCT and Pixel Detector
- $87*10^6$ readout channels
- high precision measurements for large track density near the collision point

ATLAS Pixel Detector:
- 3 barrel + 3 forward/backward disks
- 1744 modules with 16 FE-I3 chips each
- ~$80*10^6$ readout channels



ATLAS IBL (Insertable B-Layer):
- 224 modules with 2 FE-I4 chips each
- ~$12*10^6$ readout channels

Current off-detector readout

The ATLAS Insertable B-Layer (IBL) readout system will carry out the same functions implemented in the current Back-Of-Crate (BOC) and ReadOut Driver (ROD) cards. The IBL B-layer features electronics DAQ boards with modern and powerful programmable devices and high-speed links. Except the IBL system, the current readout architecture that is implemented in all pixels and SCT layers will be maintained unchanged. Particularly, **the current system** interfaces with the front end at a rate that ranges from 40 to 160Mbit/s, depending on the layer and on the type of detector. At maximum a B-Layer ROD-BOC pair interfaces with 7 modules, and each module contains 16 FE-I3s (making it a total 112 Frontends being read by the ROD BOC pair).

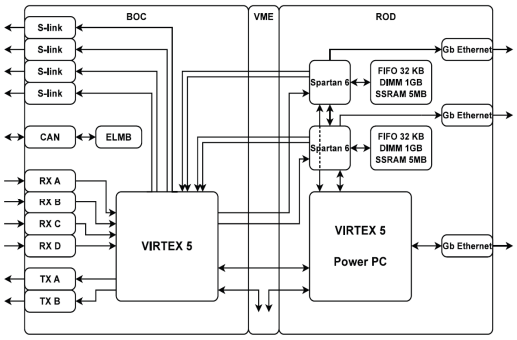
current ROD-BOC pair

- readout of 8 modules @ 160 Mb/s – 1 S-Link
- 11 Spartan2 FPGAs
- 5 TI DSPs:
  - 1 of them for ROD control
  - 4 of them for histogramming and fitting

New off-detector readout

The aim of the new ROD card under design and development for IBL is to interface with **32 FE-I4 ASICs at a rate of 160 Mbit/s** and with the ATLAS DAQ system using **4 S-Links**, supporting the dual output required for the proposed FTK subsystem (dual-HOLA S-Link). The new ROD card proposes two XILINX Spartan6 programmable devices and one Virtex5 with Power PC capabilities. These commercial devices permit also to reuse most of the VHDL code that was designed to implement the firmware on the current ROD card for the ATLAS pixel and SCT experiments. The new BOC-ROD system prototype is foreseen by early 2011 and is going to be tested on the same 64x VME-based crates that are now implemented for the ATLAS pixel and SCT DAQ detector. The new IBL system is scheduled to be mounted in the LHC-PHASE1.

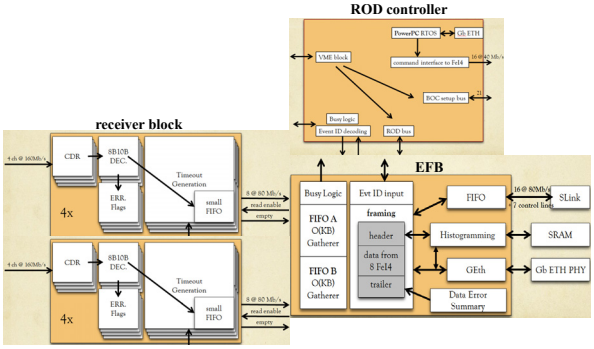
Proposed off-detector readout features:
- readout of 32 FE-I4 @ 160 Mb/s – 4 S-Links
- up-to-date FPGAs with internal memory: Virtex5, Spartan6
- no DSPs
- use of a PowerPC core inside a Virtex5 FPGA
- fast interface (Gb Ethernet) to a PC farm
- faster control and data transmission to/from FE-I4
- collect partial histograms on FPGA/SSRAMs (for selected scans)
- accumulate OCC, optional ToT and ToT² data per Vcal step
- transfer partial histogram to the PC farm (after trigger loop)
- execute fit on remote processing unit, PC and/or GPU
- improved flexibility for fit code development, more convenient tools compared to DSP environment



BOC-ROD main firmware blocks for 8 Fe-I4 chips / 1 S-Link

A **receiver block** per incoming stream has to receive and sample data after being converted into electrical signals by the optical receiver. After 8B/10B decoding data will be gathered in (8+1 bit) words. Frame detects will dump IDLE words and push data into a FIFO, adding header information. The block should also be able to insert Timeout events into the FIFO and do bookkeeping.
4 Receiver blocks will act together transmitting data to a single gatherer, called the Event Fragment Builder (EFB), within the ROD one at a time.
The **EFB** block produces a data frame in which each event contains a header (with L1ID + BCID information inside), data from the 8 FE-I4 in an ordered way, plus a trailer containing a data error summary. Frames produced are then sent towards 3 different paths:
- to the S-Link,
- to the Histogramming block;
- towards the GBit Ethernet block.

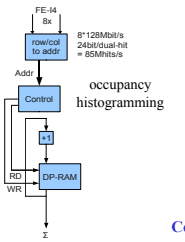
The **ROD controller** is a programmable device with a PowerPC inside performing all the basic control ROD operations. The PowerPC runs an RTOS (Real Time Operating System) with software to perform system control and non real-time functions, while the FPGA logic performs all the real-time functions.

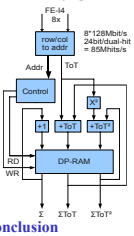


The main functions of the ROD controller are:
- providing the BOC and ROD setup buses used to access the configuration registers on the ROD and BOC boards,
- receiving configuration data from the VME host or through a GBit Ethernet connection to an external control PC,
- managing and distributing triggers: triggers can be generated either by the TIM board (physics triggers) or by the PowerPC serial port (calibration triggers),
- routing the busy signal from the EFB block to the TIM,
- controlling calibration runs via the PowerPC, which provides calibration triggers and checks if the data taking is working properly.

Histogramming block

A novel approach to carry out histograms and analysis is proposed by transferring data to a PC-farm via fast Gbit/s Ethernet links. These features allow for executing calibration and fits off-line instead of using DSP components on the ROD card as it is done now. Also the total calibration processing time will be reduced. In more detail, the new ROD will execute only the calibration loops to accumulate the per pixel occupancies, sums of time-over-threshold and sums of time-over-threshold-squared parameters. Then histograms are created and saved on-the-fly on RAMs and eventually transferred via Gbit/s Ethernet to an off-line high-performance computer.





Conclusion

The architecture of the new BOC-ROD boards for the readout of IBL pixels is presented. The boards are currently under design and a firmware test based on Avnet evaluation boards is planned.