Detailed Performance Study of ATLAS Endcap Muon Trigger with Beam Collision Data

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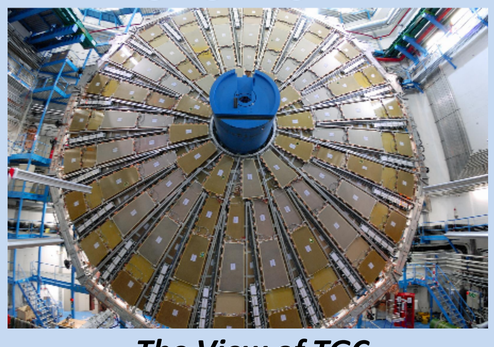
1. ATLAS Level-1 Endcap Muon Trigger : TGC (Thin Gap Chamber)

TGC : Multiple Wire Proportional Chamber, with high-gain gas and thin (1.4mm) gap for fast response.

- 7 gas gaps grouped in 3 stations
- Gas : CO_2/n-Pentane (55:45)
- Number of chambers : ~3700
- Readout channels : 320k
- Anode : wire (measures η^* direction)
- Cathode : strip (measures ϕ direction)
- Coverage in η : $1.05<|\eta|<2.40$
  Endcap ($1.05<|\eta|<1.95$) , Forward ($1.95<|\eta|<2.40$) * $\eta = -\ln(\tan\theta/2)$
- Trigger sector : Endcap (divided by 48 in ϕ) , Forward (24 in ϕ)



The View of TGC

Trigger Information

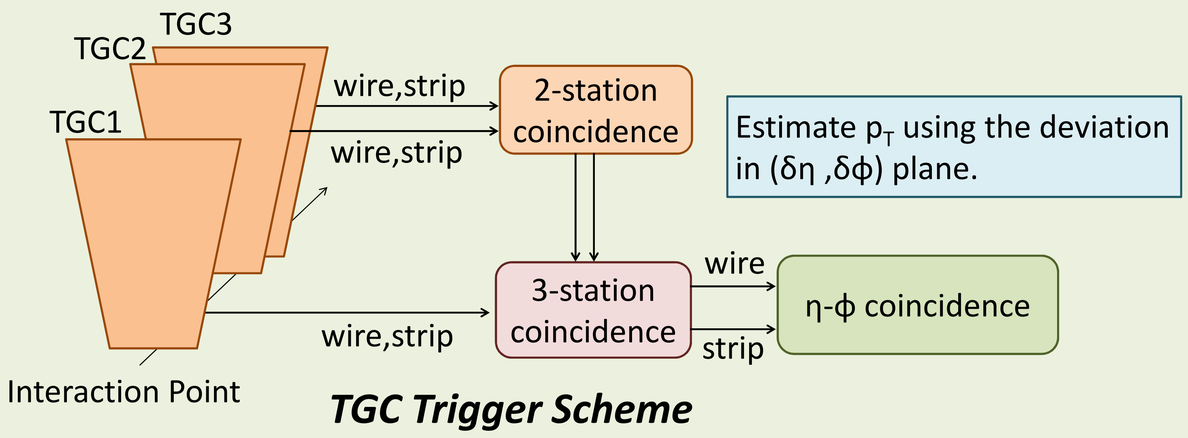
1. Position (Region of Interest, RoI) : provided as a seed of Level-2
   the total number of RoI is 8640 per side
   $\eta \times \phi$ = 0.026 x 0.033 (Endcap),
   0.034 x 0.066 (Forward)
2. Transverse momentum p_T :
   classified into 6-levels
3. Timing : Give a triggered bunch ID.

p_T1	L1_MU0	Wire-strip coincidence
p_T2	L1_MU6	Track p_T > 6GeV/c
p_T3	L1_MU10	Track p_T > 10GeV/c
p_T4	Not Used	
p_T5	L1_MU15	Track p_T > 15GeV/c
p_T6	L1_MU20	Track p_T > 20GeV/c

p_T threshold for TGC

2. Trigger Scheme

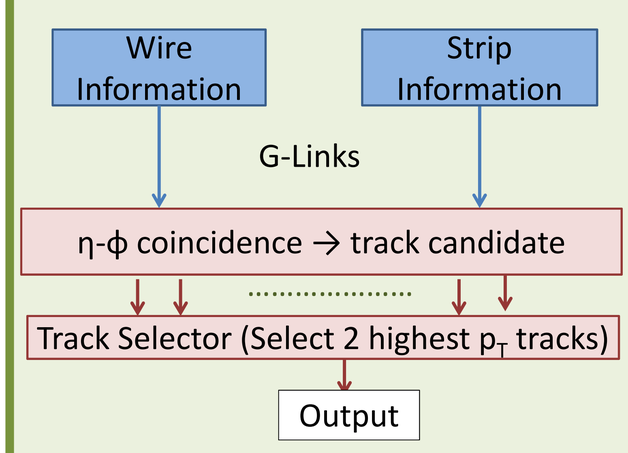
- p_T is determined by the measurement of deviation from infinite moemtum track in $\delta\eta$ and $\delta\phi$.
- Fully hardware-based (FPGAs , ASICs)



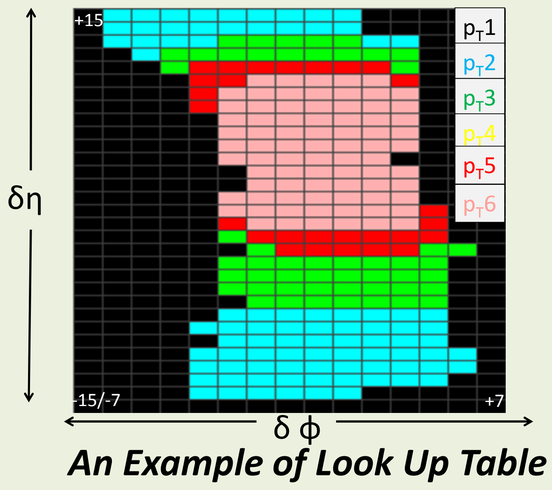
TGC Trigger Scheme

3. Sector Logic (SL)

- Electronics for η-ϕ coincidence.
- p_T is determined by using Look Up Tables (LUTs) in $\delta\eta$-$\delta\phi$ plane.
- Because of variety of magnetic field and amount of material in front, different LUTs are prepared for each RoI (1080 per octant).



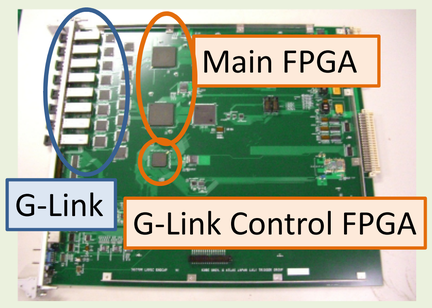
SL Trigger Diagram



An Example of Look Up Table

- Trigger rate and the status of G-Links are monitored in real time and recorded.

- SL Board
  - ◆ LUTs are stored in the main FPGAs (Xilinx Virtex-II XC2V3000-BG728)
  - ◆ G-Link controller (Xilinx Spartan-2E XC2S150E-FG456)
  - ◆ G-Link receivers (Agilent HDMP-1034A) 900 G-Link chip set are used in total.

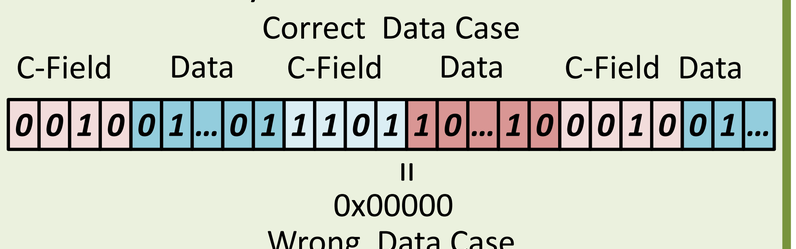


Sector Logic Board

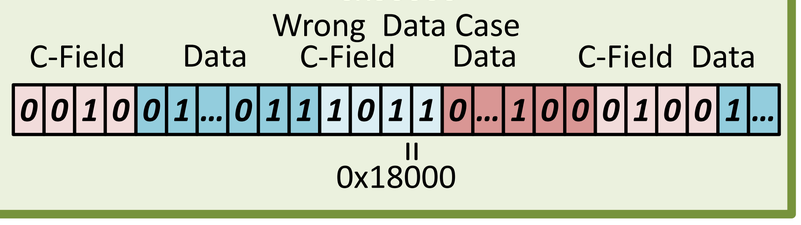
4. Sector Logic G-Link

- If serializer (G-Link Tx) continuously sends data of "all zero" without idle words, then deserializer (G-Link Rx) can make an wrong interpretation in the serial bit trains. To avoid this problem, Tx is set to idle mode before going to the run state.
- The status of G-Link synchronization is monitored and if the problem is found, reset command is sent automatically.

Correct word synchronization; all 0 data sent from TX is interpreted as 0x00000 by RX.



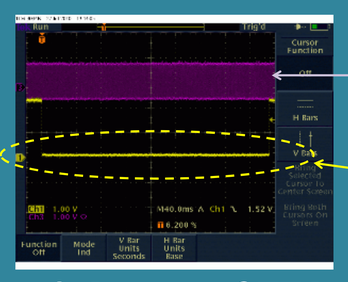
Wrong word synchronization; all 0 data sent from TX is interpreted as 0x18000 by RX.



5. Timing, Trigger and Cotrol (TTC) Configuration

- The TTCrq (LHC clock receiver) may loose synchronization when clock phase is drastically changed. (clock source changing, beam ramping up, beam squeezing)
- The configuration procedure to make the clock more robust.
  1. TTCrx reset
  2. QPLL reset (resynchronization) , which is initiated by the phase shift (180˚) of the clock from TTCrx.
  3. Set TTC signal delays of TTCrx.

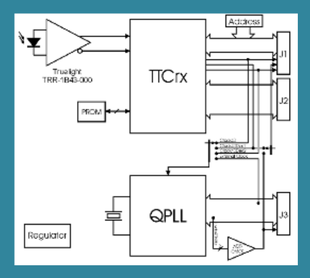
Synchronization procedure of the QPLL to be installed



Output clock from TTCrq

QPLL is processing the resynchronization

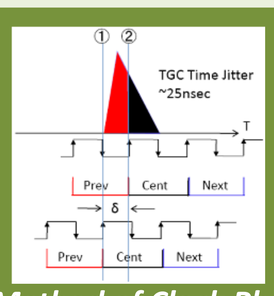
Lock Status of TTCrq



TTCrq Diagram

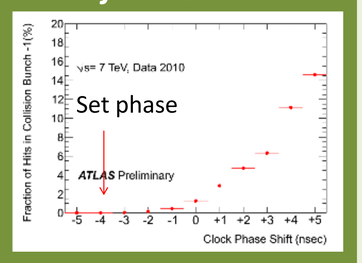
6. TGC Clock Phase Scan

- BCID timing of hit signals from chambers should be adjusted with LHC beam collision.
- The best of the clock phase is the timing when the fraction of Hits in previous bunch is turned on.



The Method of Clock Phase Adjustment

- The figure shows the result of phase scan($30nb^{-1}$). The fraction of the TGC hits in the bunch crossing before the colliding bunch as a function of the clock phase shift of the TGC, from which the optimal delay time for the opening gate can be determined.



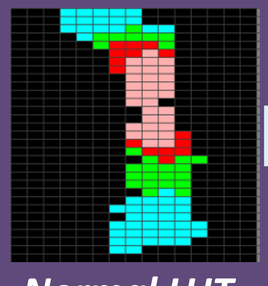
Clock Phase Shift vs Hit Fraction

The BCID timing of hit signals was adjusted

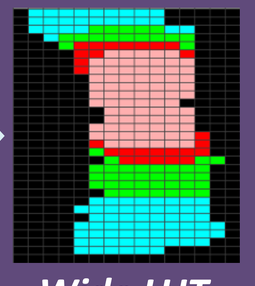
7. Level-1 Endcap Muon Trigger Efficiency

- The efficiency of L1_MU6 was lower by ~10% compared to the simulation in early days.
- It was identified as the problem of chamber crosstalk in strip which makes ϕ position resolution worse .
  ← Wider LUTs in ϕ improve the efficiency of L1_MU6.

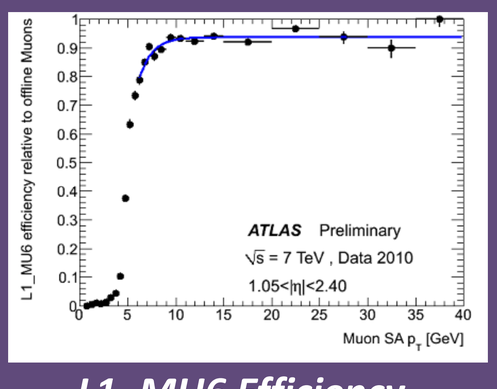
L1_MU6 Efficiency was improved by 6−8%



Normal LUT



Wide LUT



L1_MU6 Efficiency

	Data	***Simulation***
L1_MU6 Efficiency at Plateau	***93.6 $^{+0.6}_{-0.6}$ %***	***95.0 $^{+0.2}_{-0.2}$ %***