Upgrade of the PreProcessor System for the ATLAS LVL1 Calorimeter Trigger: from ASICs to FPGA

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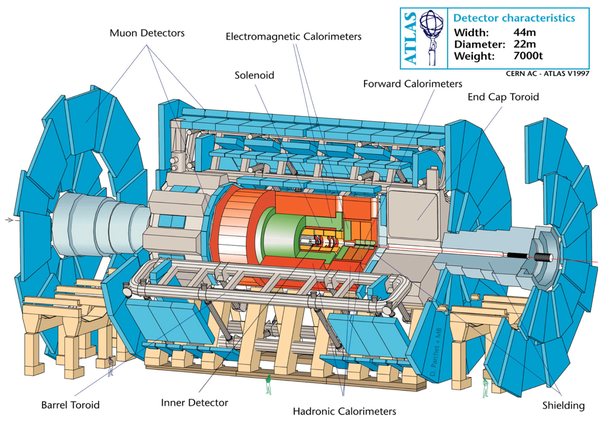
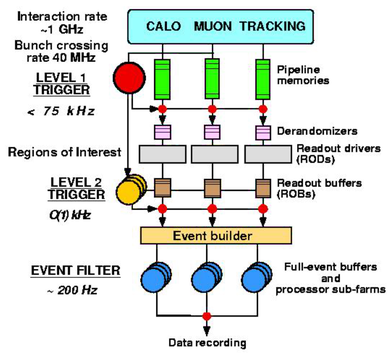
on behalf of the ATLAS TDAQ collaboration

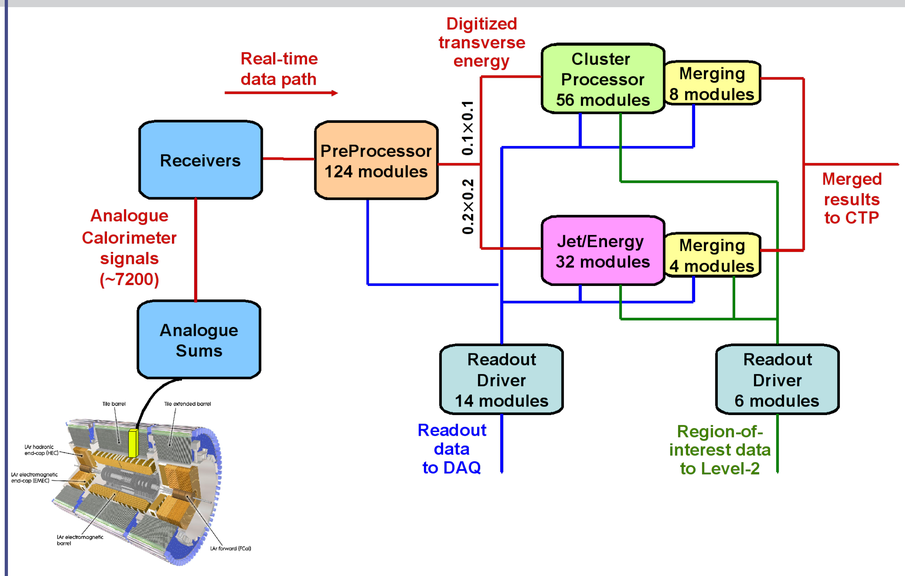
The ATLAS Experiment





ATLAS is a multipurpose experiment designed for the LHC.
3-Level trigger system is used to reduce data rates from 40 MHz to ∼200 Hz.
Custom designed processors (ASIC and FPGA based) used at LVL1 to make a fast (<2 μs) decision using reduced granularity data.

ATLAS Level-1 Calorimeter Trigger

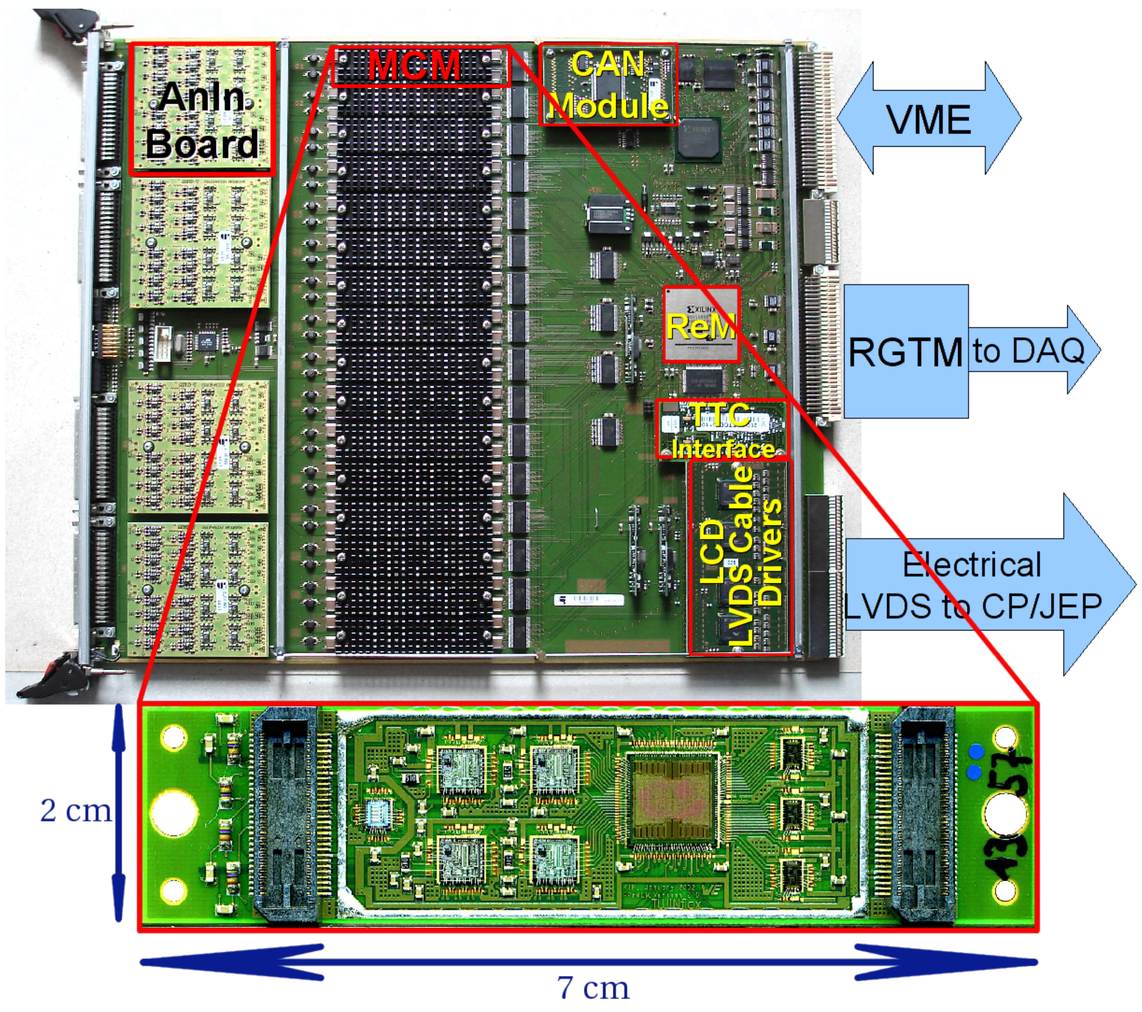


Based on Trigger Towers i.e. pre-summed Calorimeter signals
Two step system:

- **Preprocessing**: Digitisation and Bunch Crossing Identification (identifying which collision produced the signals)
- **Processing**: Search for electron, jet and tau candidates, determination of *Missing* E_T and *Sum* E_T

Features of the Real-time Data Path:
Fixed Latency (∼1 μs); Pipeline processing; Massive parallelism;

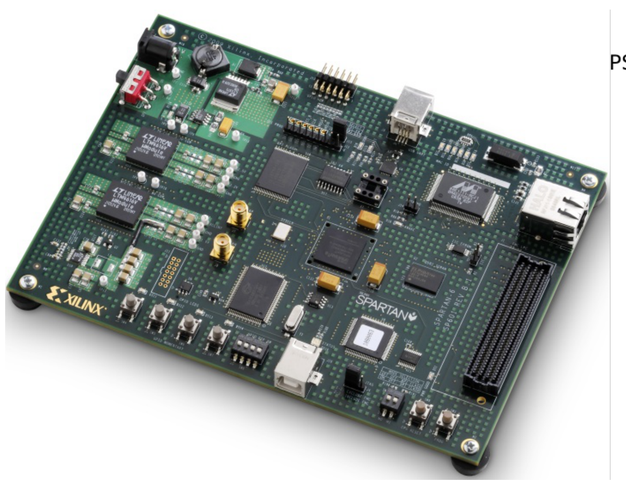
The PreProcessor System: 124 PreProcessor Modules

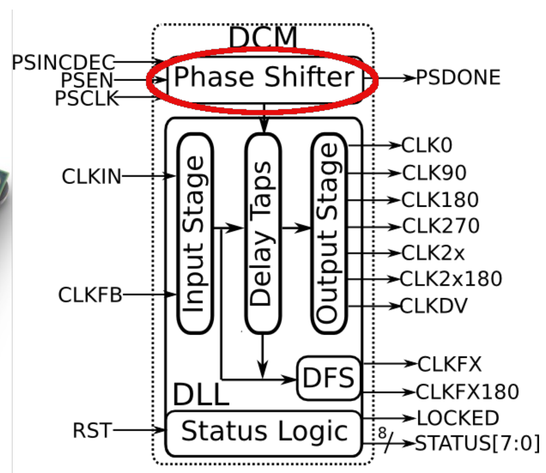


Processing is performed on a Multi Chip Module (MCM):

- 10-bit, 40 MHz, 3 BC delay, 595 mW per channel digitisation
- 1 ns sampling time adjustment
- BCID (2 methods)
- Look-up table based calibration
- Histogramming, playback
- Jet pre-summing
- 400 Mbit/s serialisation (480 Mbit/s with overheads)
- 13 BC ticks from analogue input to Jet (pre-summed) serial output

Test 1. PHOS4 replacement: FPGA for time-adjustment



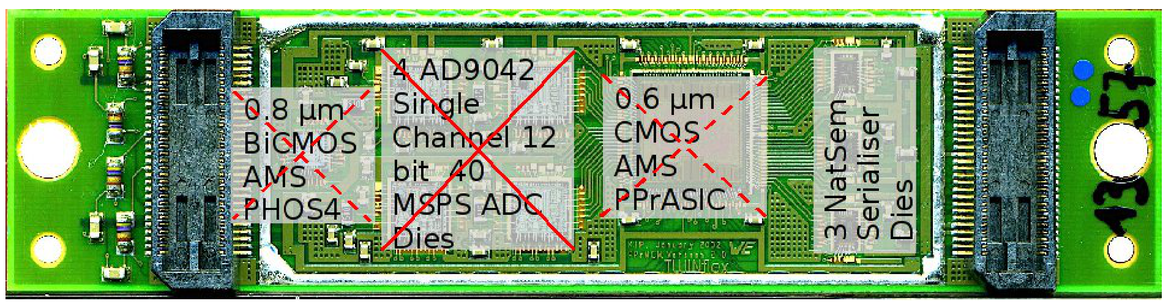


- XILINX development board with XC6SLX16-CSG324 Spartan-6 FPGA is used for testing. The CSG324-package is suitable for MCM mounting.
- PHOS4 chip task is fine time adjustment (resolution: 1 ns). This job can be done by FPGA's Digital Clock Manager (DCM):
  - Phase Shifter step is well below 1 ns
  - There are 8 DCMs in the SC6SLX45 and 4 of them can be used for PHOS4 replacement (4 channels)

Conclusions

- New MCM (nMCM) will be built with the same form-factor and functionality
- Having a reconfigurable component (FPGA) we will gain in flexibility
- PHOS4 functionality and LVDS serialisers can be implemented inside FPGA ⇒ fewer components on the module
- ASIC code is ported to XC6SLX16-CSG324 Spartan-6 FPGA for testing (78% of the chip is utilised by the ASIC and serialisers implementation)
- Standard components allow us to use commercially available evaluation boards, together with the existing equipment for the current MCM testing, for the FPGA configuration bitstream development and for tests in parallel with the design of the PCB layout for the new module

New MCM. Motivation.

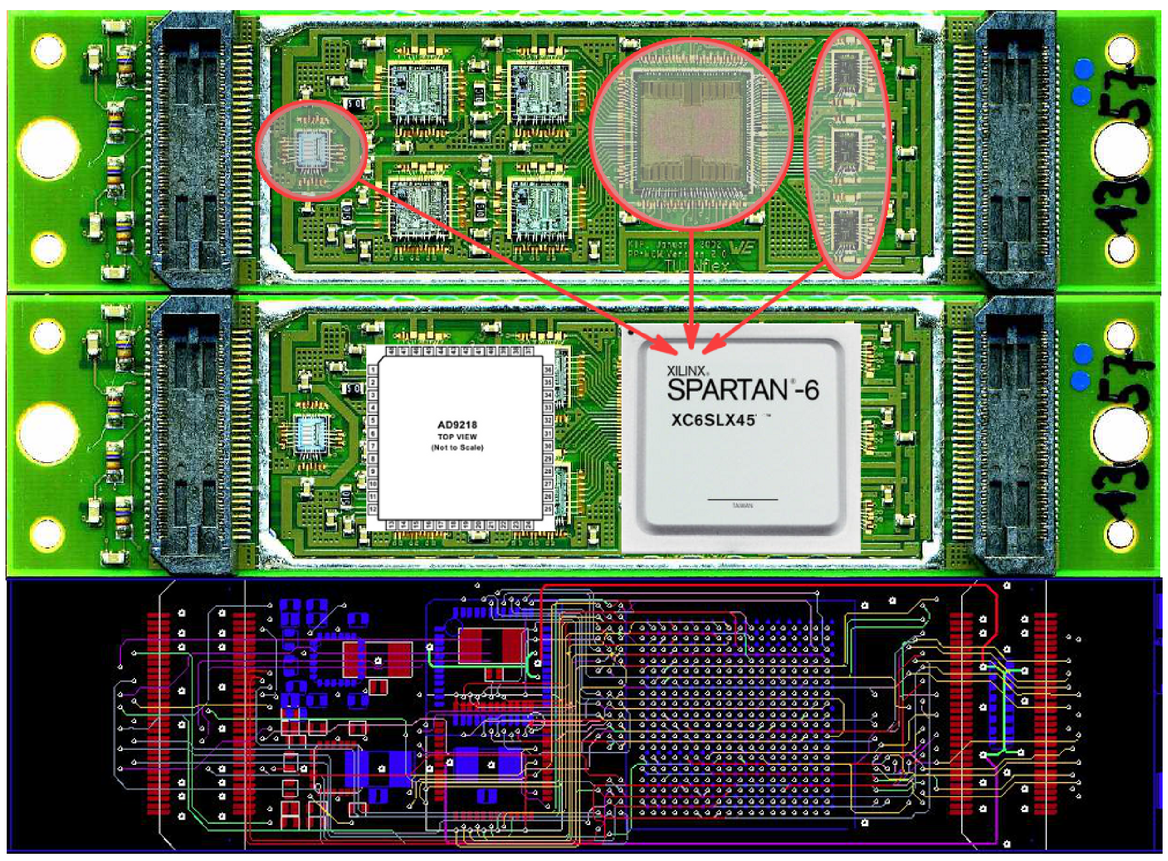


VERY conservative spare policy(50%) has been implemented, but we would not be able to quickly produce more MCMs. We have 9 ASIC dies on each of 2048 MCMs:

- **PHOS4** (time-adjustment chip with 1 ns resolution): GDSII available, process (still) available, success uncertain, no support
- **AD9042**: not available as unpackaged die any more, packaged version has prohibitive size
- **PPrASIC**: Verilog available, process (still) available, GDSII available, outdated technology (0.6 μs)
- **Serialisers**: available, new pin compatible DS92LV1023E is recommended by NatSem

Ten years of technology change since original MCM development. ***Modern reconfigurable devices will allow us to adjust and to add new pre-processing algorithms (event-by-event pedestal subtraction, more sophisticated BCID algorithms, etc.) for higher luminosity expected after the LHC Upgrade***

New MCM

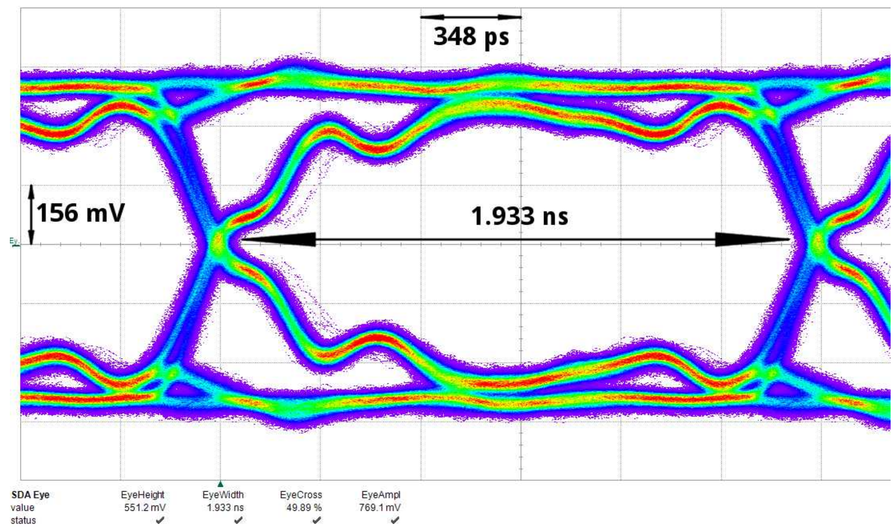


We would like to develop a pin-, size- and latency-compatible substitute for the MCM based on today's components:

- AD9218 – dual 105 MHz 10 bit FADC
- Xilinx Spartan-6 (SC6SLX45) FPGA in the CSG324 (15x15) package
- Functionality of ASIC, PHOS4 and LVDS Serialisers inside FPGA – is it possible?

Test 2. LVDS serialisers in FPGA

480 Mbits/s: (10 data bits + 1 start bit + 1 stop bit) @ 40MHz
Eye-diagram shows a good signal quality confirming that Spartan-6 can be used as a serialiser:



Implemented using Spartan-6 output serialiser blocks (OSERDES2).