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Development of a beam test telescope based on the Alibava readout system

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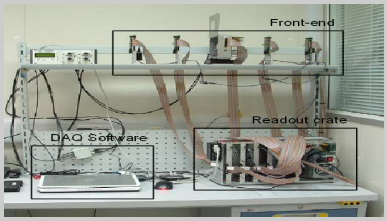
Introduction

- A telescope is a tracking system used to measure the spatial resolution performance when developing new detectors.
- The system is intended for working in a beam test environment.
- The system will be used to carry out both analogue charge collection and spatial resolution measurements.
- The system is designed to be with different types of microstrip or pixel silicon detectors.

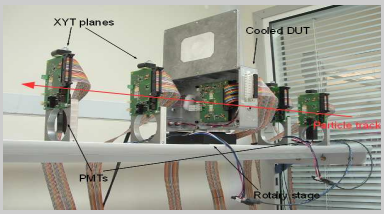


The main parts of the telescope

- The telescope has a front-end part, a readout part and a DAQ software.

System architecture

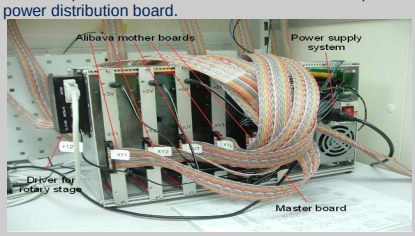
- The front-end includes the following parts.
  - Four XY measurement and trigger planes, perpendicular to the particle track, where XYT boards are located.
  - Detector under test (DUT) attached to a chilled DUT board, mounted on a rotary stage.
  - Two scintillators and PMTs placed in the outermost XYT planes for triggering purposes.



Front end of the telescope

- Although in the base unit designed there is a provision for just one plane, up to twelve DUT boards can be read out by the telescope.

- The readout part of the system is composed of the following items.
  - An Alibava mother board connected to each XYT or DUT board.
  - A master board which collects the data and distributes the control signals (trigger, clock and reset) to the Alibava mother boards
  - The master board is connected to the DAQ software via Ethernet.
  - The boards are placed in a crate with a standard PC-like power supply and a power distribution board.

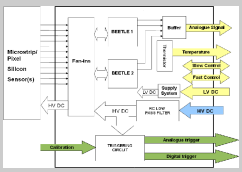


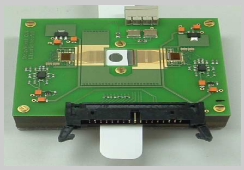
Readout part of the telescope

- The boards are placed in a crate with a standard PC-like power supply and a power distribution board.
- There is also a driver for the rotary stage attached to the crate.

DUT Board

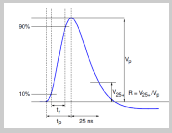
- Two Beetle ASICs (256 channels) for the readout of either strip or fanout pixel silicon detectors of different types.
- Buffer stage for the Beetle chips analogue outputs. Optional equalization if long cables are required.
- Fast control (LVDS) and Slow control (I2C) shared by the Beetle chips.
- There is a temperature sensor attached to the backplane via the copper chuck.
- Independent HV DC level for biasing the sensors.
- Trigger circuit from the detector backplane signal if a self-triggering mode is required.
  - Charge amplifier stage: analogue trigger pulse.
  - Constant fraction discriminator: digital trigger pulse.
  - Time jitter of 60 ns.
- The DUT can be mounted on a rotary stage controlled manually or by software: possibility of varying the angle between the DUT and the particle track.
- The DUT is chilled with a Peltier element.
  - USB temperature controller.
  - Air fans for the heat sink of the Peltier element.


Block diagram of the DUT board

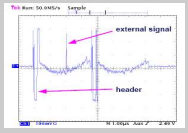

DUT board picture

Beetle ASIC

- ASIC Beetle: readout chip developed at ***ASIC laboratory of the University of Heidelberg.***
- 128 input channels with charge amplifiers and shapers.
- Front-end output signal: V_p = kQ. T_p – 25 ns.
- This output is sampled into the analogue pipeline (128x187 cells) with the frequency of the Beetle chip clock (40 MHz).
- Analogue pipeline latency fixed of 128 CLK cycles (3.2 µs).
- Analogue multiplexed readout: 16 bits header + 128 analogue channels 25 ns wide.
- Charge injector on each channel for calibration purposes.
- Fast control (LVDS) signals for clock, trigger, reset and readout detection.
- Slow control (I2C) for chip configuration.



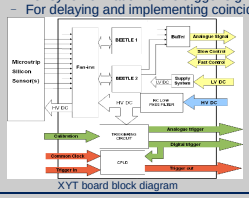
Beetle front-end output signal

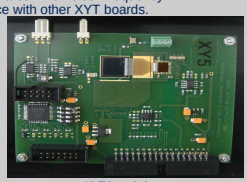


Beelte analogue multiplexed readout

XYT Board

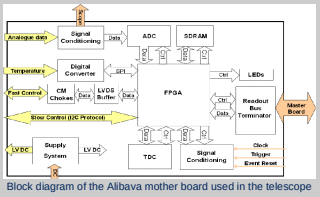
- The XYT board measures the track space points using two silicon strip detectors mounted back-to-back at 90 degrees.
- Different strip detectors (p-in-n and n-in-p) with a thickness of 300 µm are used for robust amplitudes and charge sharing.
- Either 80 µm pitch detectors or 40 µm pitch detectors with intermediate strips (for more spatial resolution) can be used.
- The coordinate measurements are carried out with two Beetle ASICs (256 channels).
- Buffer stage for the Beetle chips analogue outputs. Optional equalization if long cables are required.
- Fast control (LVDS) and Slow control (I2C) shared by the Beetle chips.
- The XYT board can also trigger on the particle tracks in the beam test using a trigger circuit from the detector backplane signal.
- The trigger circuit produces analogue and digital trigger pulses with a time jitter of 60 ns.
- There is a CPLD connected to the trigger circuit. It is also connected to other XYT boards and to the Master board.
  - For synchronization of the trigger signal to a common clock frequency.
  - For delaying and implementing coincidence with other XYT boards.


XYT board block diagram

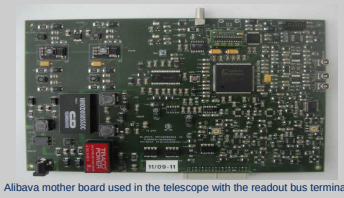

XYT board picture

Alibava Mother Board

- A modified Alibava mother board is used to readout and to control each XYT/DUT board.
- The board works using a common trigger and clock signals as well as an common event reset signal as inputs.
- The board has a Xilinx Spartan 3 FPGA clocked at 40 MHz with an on-board oscillator.
- There is also a SDRAM (256 Mb) for temporary acquisition data storage.
- Beetle ASICs analogue data are processed and digitized by a signal conditioning block and two ADCs.
- Fast control and Slow control signals for the Beetle ASICs are generated directly by the FPGA.
- The former board trigger inputs are used for the common input signals (clock, trigger and event reset).
- The TDC on board (600 ps resolution) is used to have a time stamp of each input trigger: no synchronization required between common clock and trigger.
- The data collected by each Alibava board are sent to the a Master board: local data/address bus with a custom digital protocol.
  - The former USB controller replaced by a digital connector and a readout bus terminator for the communication with the Master board.
- The board has its own supply system (DC-DC converters and LDO regulators) from a 5V DC input: required Alibava board supply levels and XYT/DUT board supply levels generated from this level.

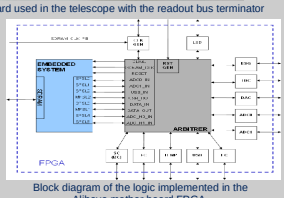


Block diagram of the Alibava mother board used in the telescope

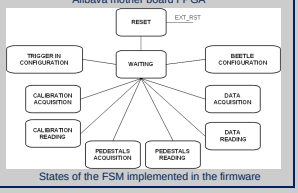

Alibava mother board used in the telescope with the readout bus terminator

- The logic implemented in the FPGA is a combination of custom digital blocks and an embedded system.
- A CFSM controls the different blocks depending on the current state of the system.
- The CFSM and SDRAM CONTROL have been implemented with a Microblaze embedded processor (32 bits RISC).
- The custom digital blocks have been described in VHDL. They perform the hardware low level control (ADCs, TDC, Master board communication, Beetle control, etc.).
- The required internal clock (40 MHz and 200 MHz) and reset signals are generated by the CLK GEN (on-board clk/rst) and ESG (external clk).
- An ARBITRER has been implemented for the communication between the embedded processor and the rest of the blocks.
- The Microblaze processor firmware has been designed as a Finite State Machine (FSM).

FPGA xc3s400-5pq208 device utilization			
Logic	Used	Available	% Utilization
Slices	3365	3584	93 %
Slice FF	1797	7168	25 %
LUTs	3851	7168	53 %
DCMs	2	4	50 %
BRAMs	16	16	100 %
Mult 18x18	3	16	18 %



Block diagram of the logic implemented in the Alibava mother board FPGA



States of the FSM implemented in the firmware

Master Board

- The Master board is implemented with a Spartan 3E Xilinx development board and a custom patch board.
- The board distributes the common clock, trigger and event reset signals to the Alibava boards through the patch board.
- The trigger signal generated by the telescope can come from the XYT boards or from two PMTs: the patch board provides the connections and circuitry required to process these signals.
- The Master board merges the data streams coming up to sixteen Alibava boards: the patch board is used for connecting the data/address bus cable to the Master board using a decoder for addressing each Alibava board.
- A test channel has been implemented for testing in a standalone mode a XYT or DUT board.
- The board also performs the communication with the DAQ software via 100M Ethernet: an Ethernet controller implemented in the FPGA.
- The board is a communication bridge. It addresses and collects data from the corresponding Alibava board. It sends these data in the corresponding Ethernet frames.
- New functions can be added to the Master board by implementing new digital logic in the FPGA.


Master board: Xilinx development board connected to the patch board

Power supply

- The power distribution for the system is carried out by means of a standard PC power supply which supplies +5V and +12V.
- There is a power distribution board connected to the power supply to fan-out these levels to:
  - Alibava boards.
  - Master board.
  - PMTs.
  - DUT rotation stage.
  - Air coolers for the Peltier element of the DUT.
- The XYT boards and the DUT board are powered from the Alibava boards.
- The detectors of the XYT boards and the DUT board are powered with dedicated power supplies since they require HV and current sensing.

Software

- Main characteristics.
  - Control the telescope hardware by raw Ethernet communication for configuration, calibration and data acquisition.
  - User interface with the system (GUI).
  - Generation of information (output file).
  - The software also processes the raw data acquired by the Alibava boards to obtain data with physical meaning.
- The DAQ software has been designed using two levels.
  - Low level implements the communication between the software and the Master board by raw Ethernet and the low level data processing.
  - High level includes the GUI and the output file generation.
- The software has been designed using C++ language.
- Operating system compatibility: Linux.
- Track based alignment software has also been developed for the data obtained with the DAQ software.

System status

- The hardware part of the system is produced and tested separately.
  - 5 XYT boards.
  - 2 DUT boards.
  - 10 Alibava boards.
  - 2 Master boards.
  - 10 Readout bus terminators.
  - 2 power distribution boards .
  - Cabling.
- The Alibava FPGA logic and firmware has been redesigned and tested.
- The Master board FPGA logic has been designed and tested.
- The DAQ software is being developed based on the Alibava DAQ software.
- The track based alignment software is being developed.
- Next steps:
  - Software tests.
  - System integration and commissioning.