Study for the LHCb readout board

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Outline

- LHCb Upgrade
- Building blocks for high speed read-out
- Performances
- Slow control
- Scalable read-out architectures

LHCb Upgrade

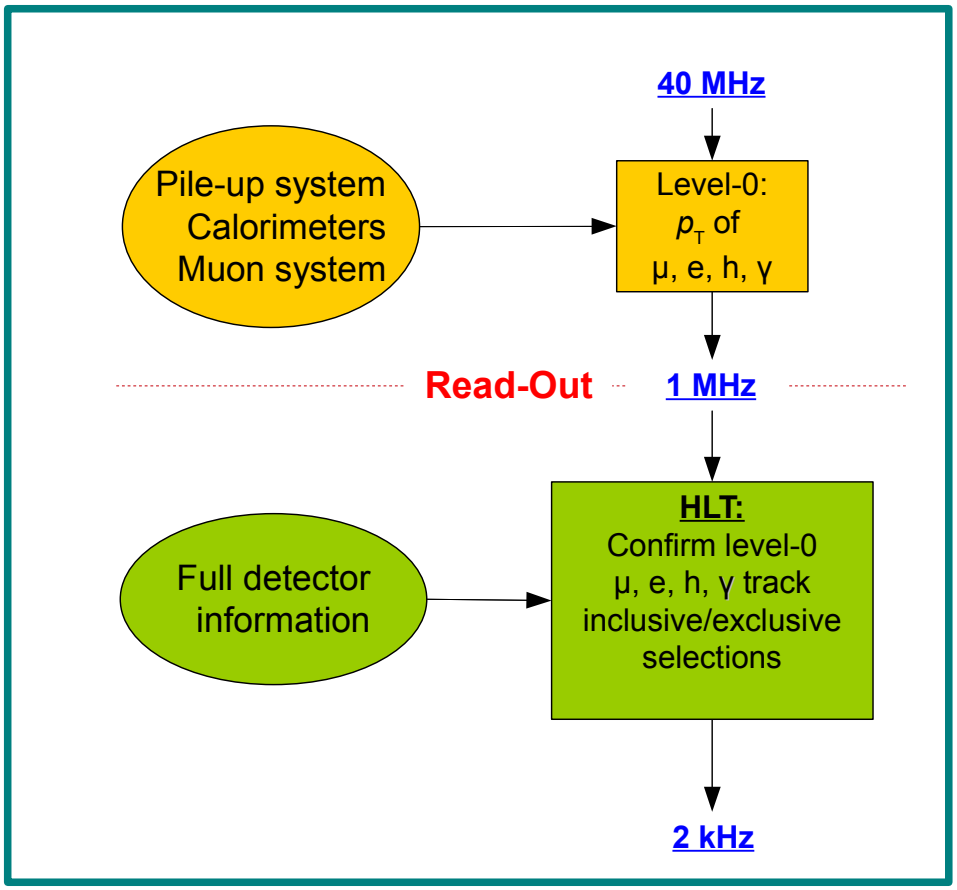
Envisaged LHCb Upgrade in 2016

Motivation

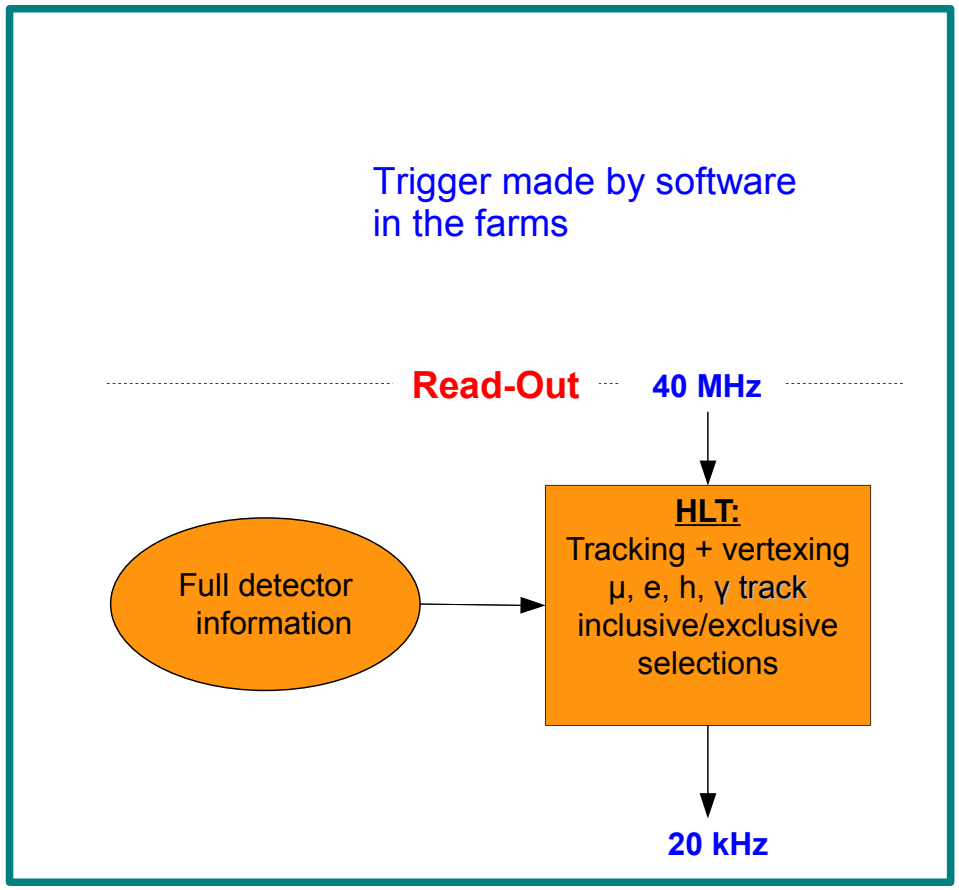
Goal is to increase the statistical power to study new physics by:

- Increasing the instantaneous luminosity from 2×10^{32} to 2×10^{33} $cm^{-2}s^{-1}$
- Improving the trigger efficiency for hadronic channels
- Collect $\int \mathscr{L} \geq 50$ fb^{-1}

Trigger upgrade



Current trigger scheme

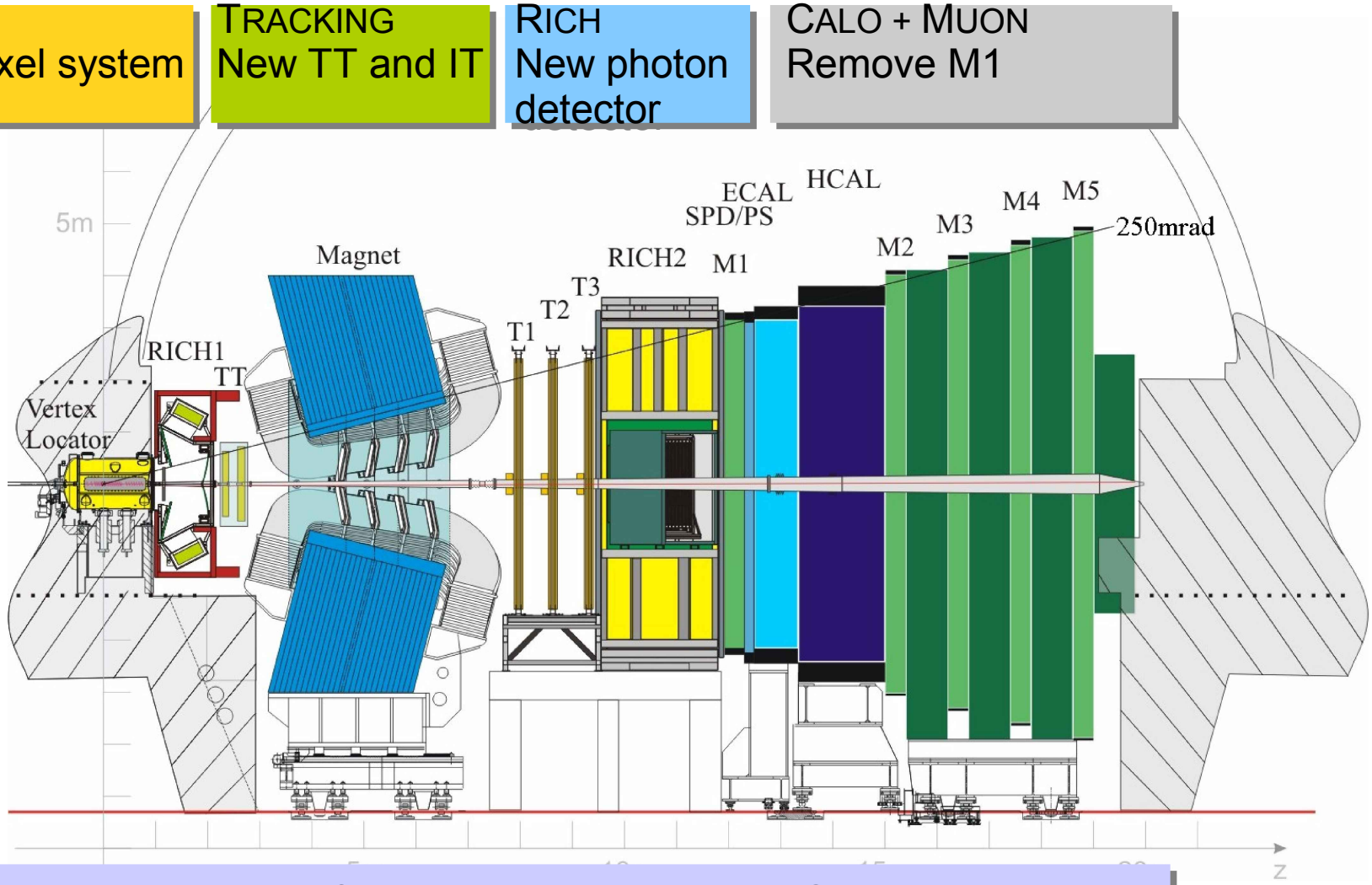


Future trigger scheme

All detectors read at 40 MHz

Detector Upgrade

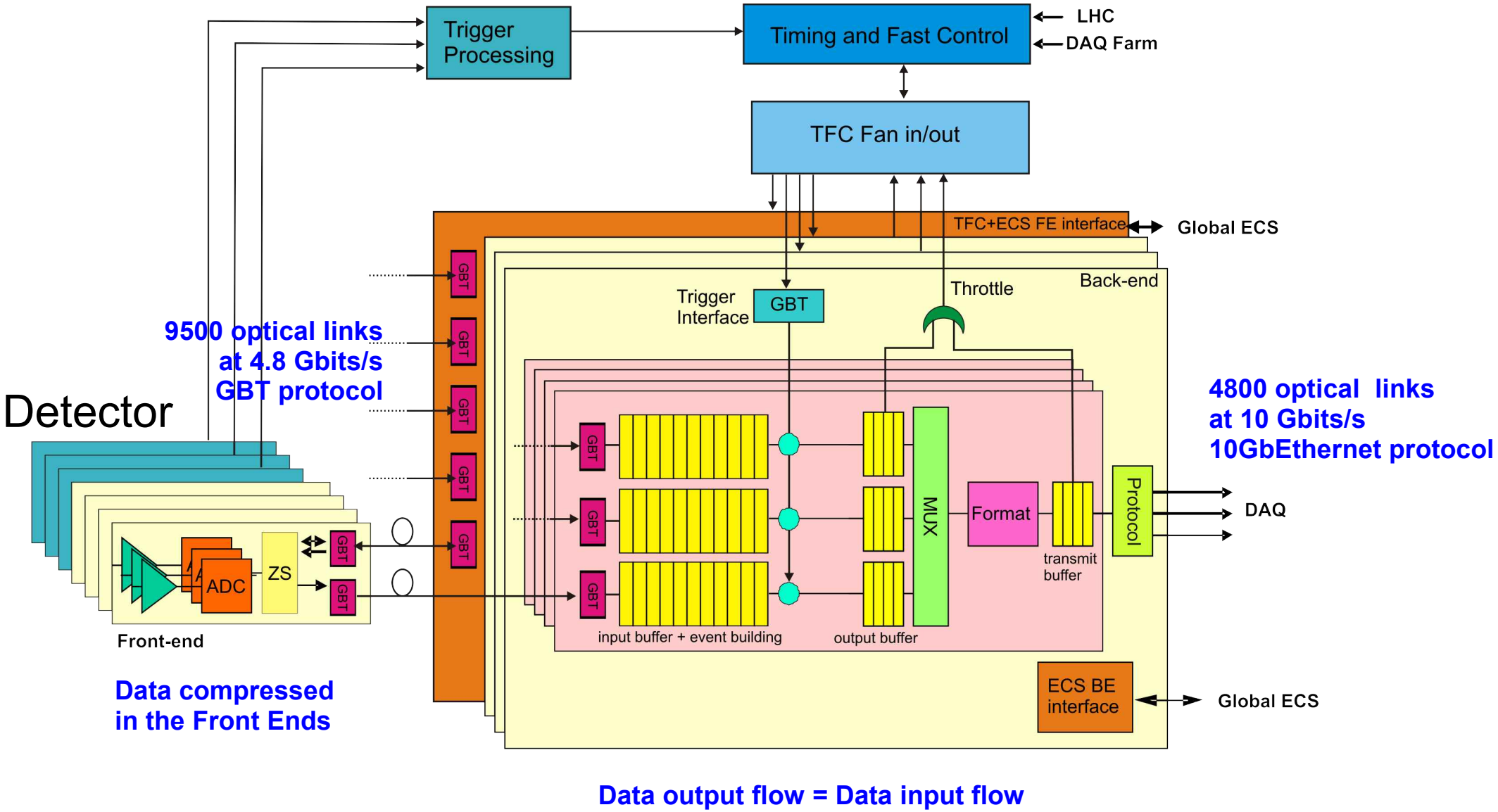
VELO	TRACKING	RICH	CALO + MUON
New pixel system	New TT and IT	New photon detector	Remove M1



Replace all the front-end electronics + DAQ network

See "The Front-end Electronics of the LHCb Upgrade" presentation by Jan Buytaert in this workshop: 21-Sep-2010 12:15

LHCb read-out requirements

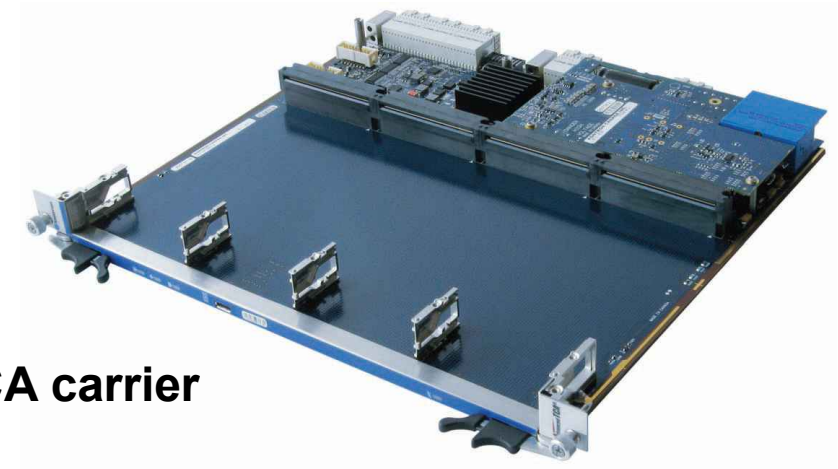


Building blocks for high speed read-out

Guidelines for the study

Requirements	Prototype implementation
Interface with Front Ends: GBT protocol Interface with the farms: 10 GbE	**Emulation of GBT protocol** in FPGAs. Handling of **high speed serial links (10 Gbits/s).** *Understand the limits (signal integrity, connectivity).*
Find an architecture flexible enough to face demand changes, reuse of common building blocks ...	Test modular standard communication architecture (**xTCA**). *See eventual limitations.* **Use of mezzanines for I/Os**.
GBT centered architecture mixing data, slow control and time distribution	Test **new supervision scheme** embedded within FPGAs. *Measure performance.*

Development based on xTCA



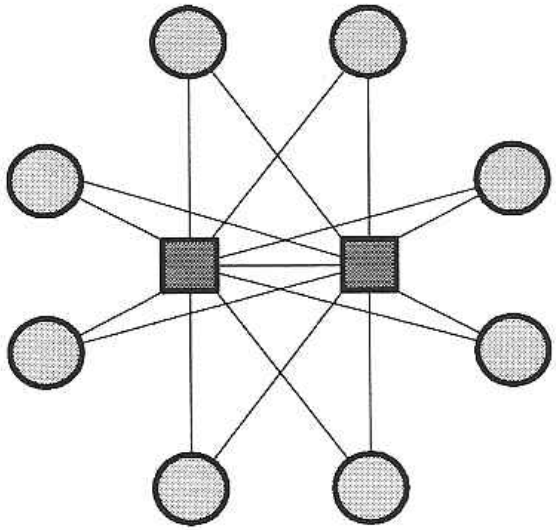
ATCA carrier

ATCA

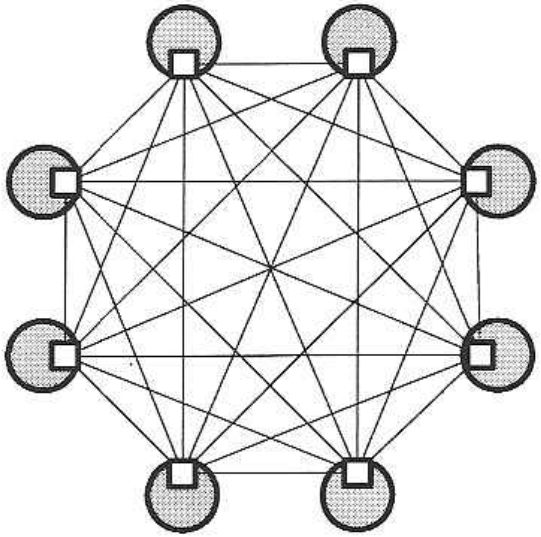
AMC card

µTCA

Powerful connectivity in xTCA standards

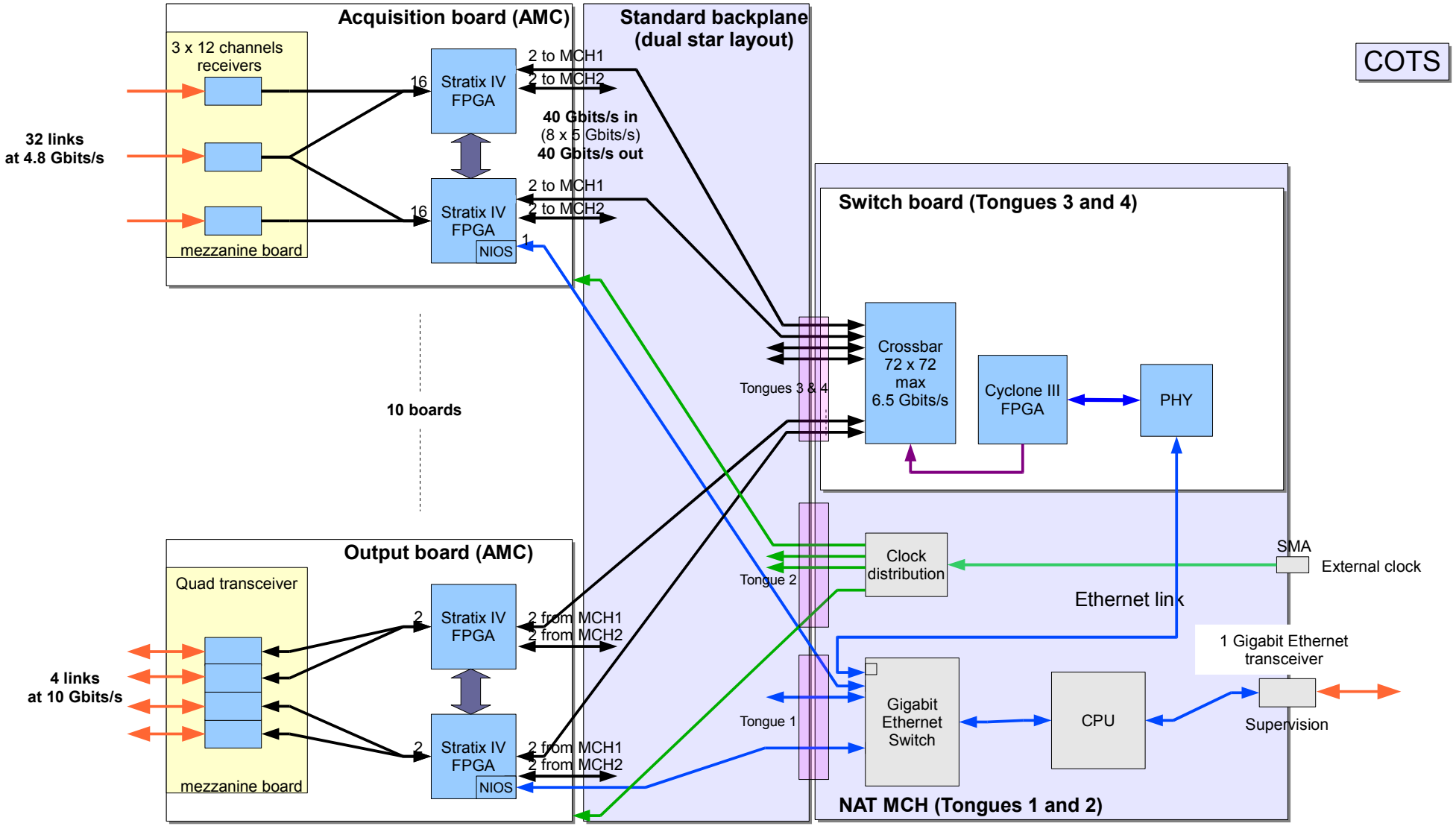


Dual star topology

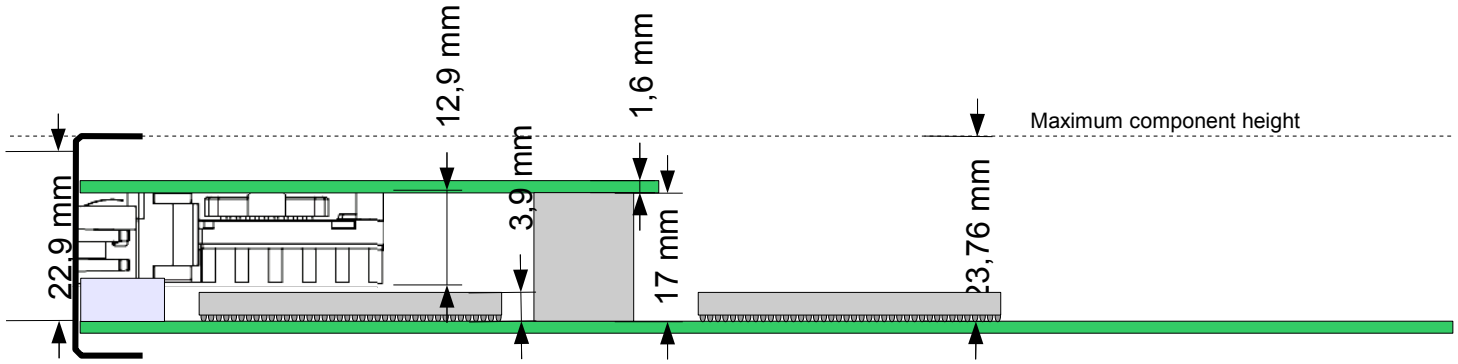


Full mesh topology

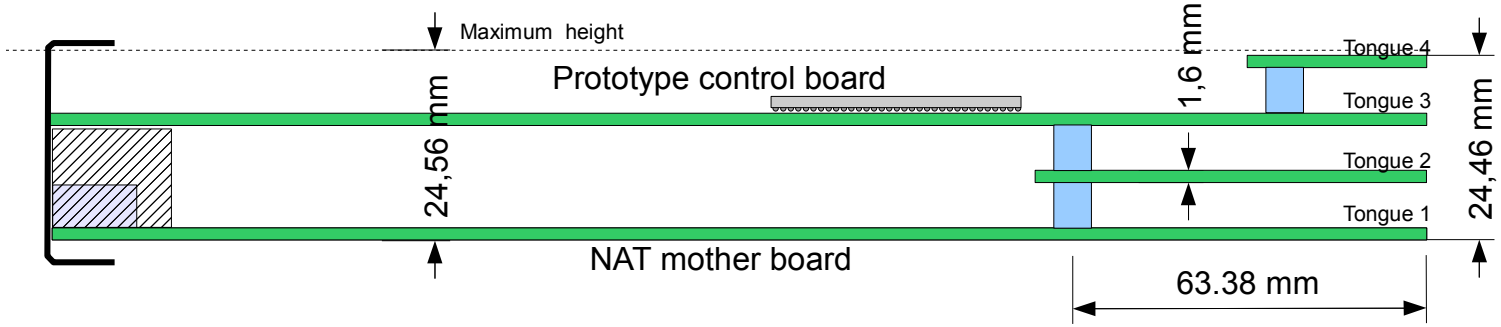
µTCA Prototype



Mechanics



AMC board

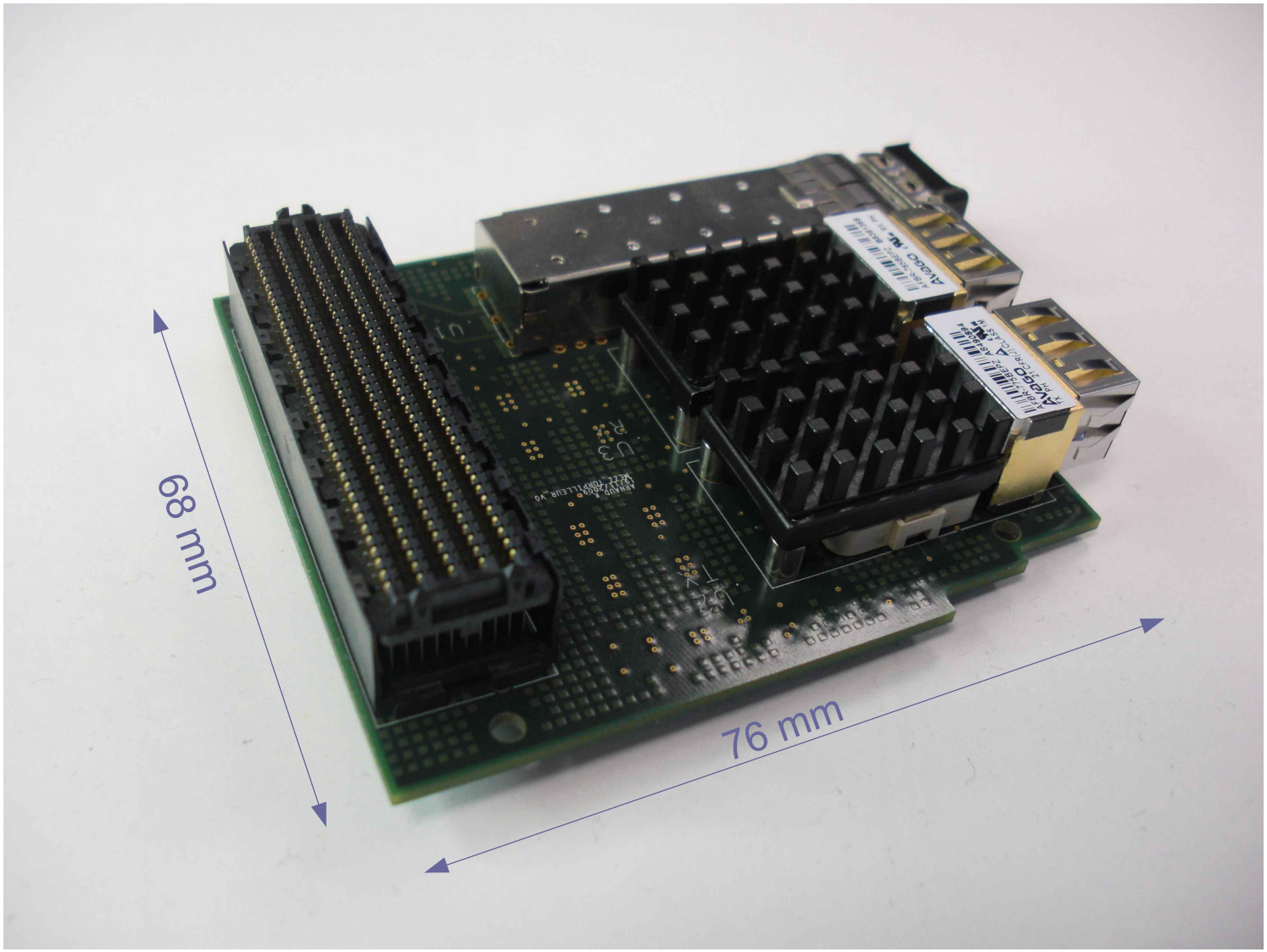


MCH board

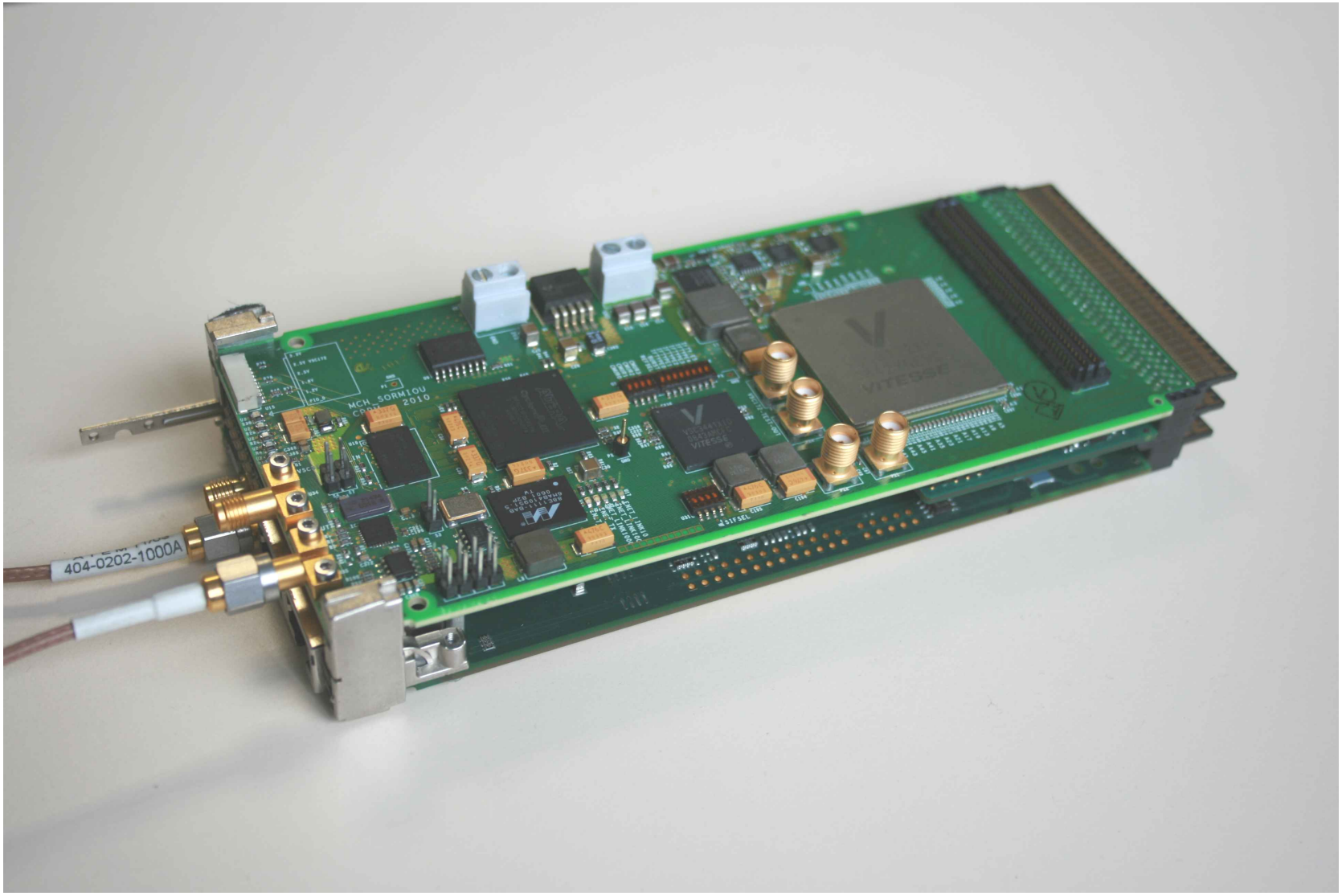
AMC board


73 mm
181 mm
ALTERA
Stratix IV
EP4SGX230KF40C2NES
H AAAA80913A
KOREA

Mezzanine board



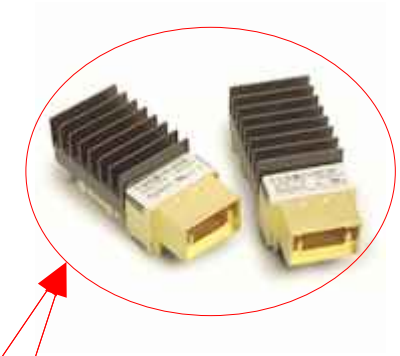
MCH board

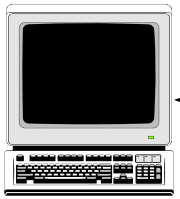


Performance

Serial lines at 4.8 Gbits/s

- **Setup**
  - Implementation of the **GBT protocol**
  - **No preemphasis – No equalization**





JTAG

NIOS core

Data generator

84 bits

GBT protocol encoder

SNAP12 emitter

Optical fiber 10 m

32 bits

Error counter

Check

84 bits

GBT protocol decoder

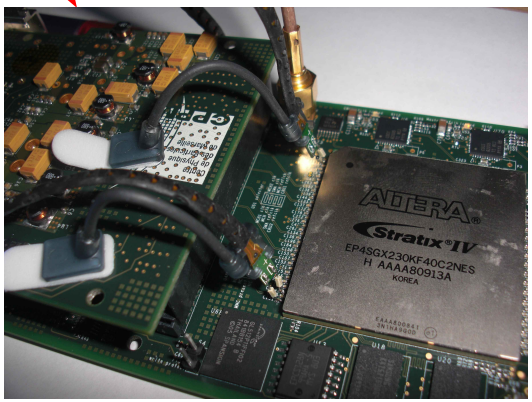
SNAP12 receiver

84 bits

Data generator

Stratix IV GX

Measurement



40 MHz

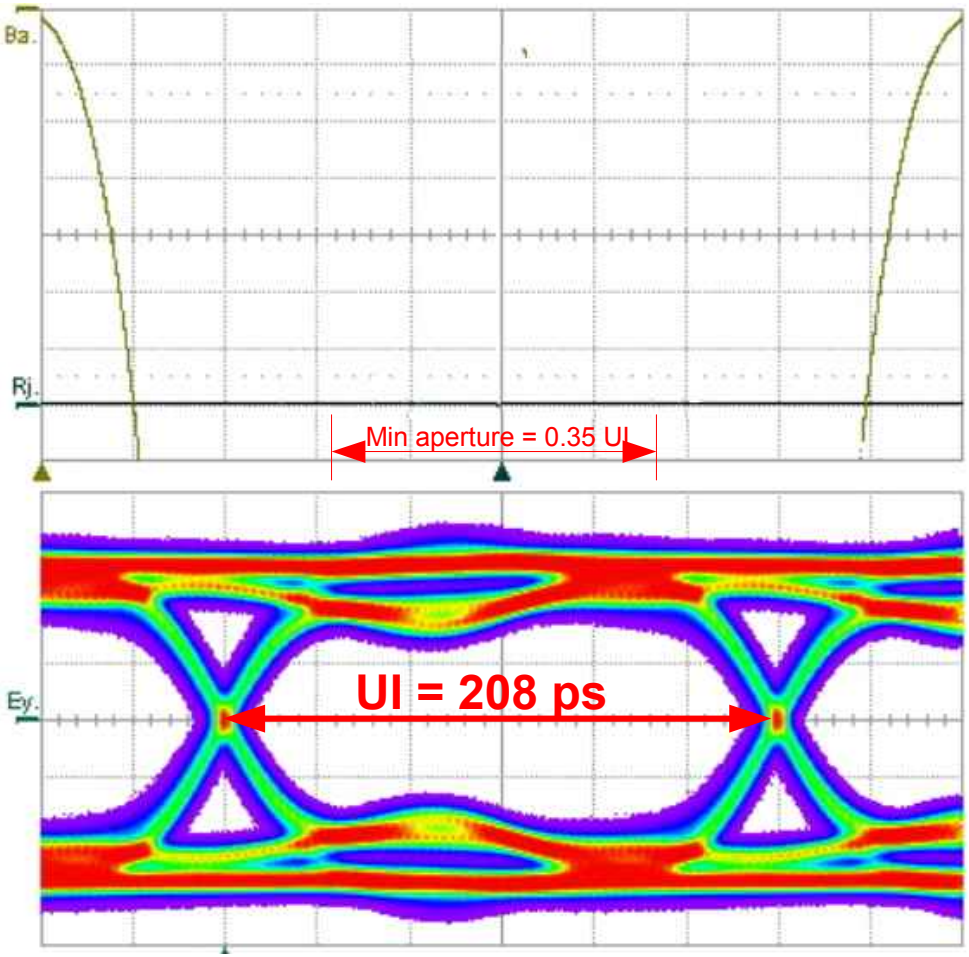
PLL Jitter filter

240 MHz

0.35 ps RMS (10 kHz to 20 MHz)

Measurements at 4.8 Gbits/s

Serial link at 4.8 Gbits/s with GBT protocol

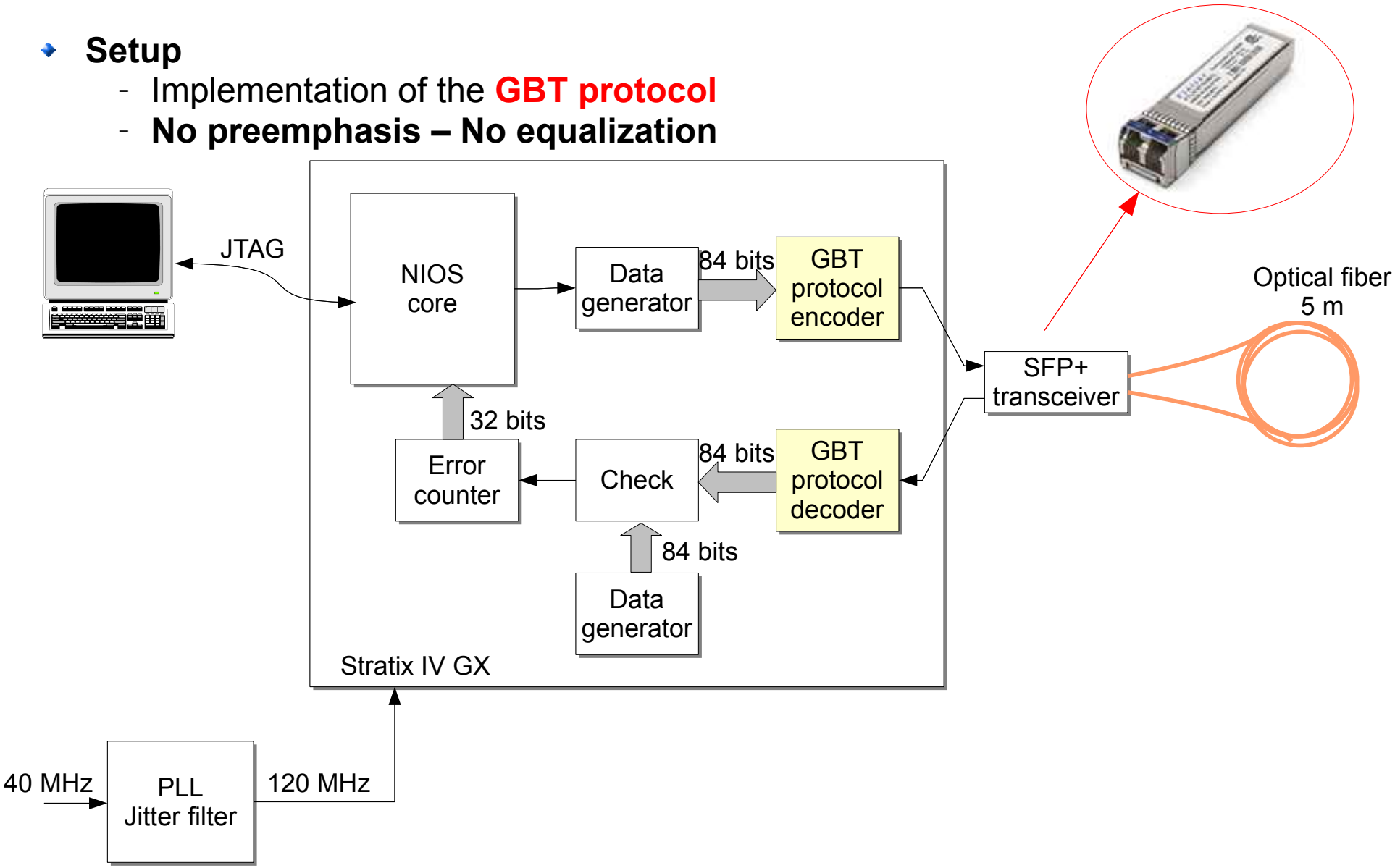


- **Measured jitter at 10^{-12}**
  Total : **40 ps (p to p)**
  Random : **2.4 ps**
  Deterministic : **7.8 ps**

- **Estimated error rate :**
  much less than **10^{-16}**

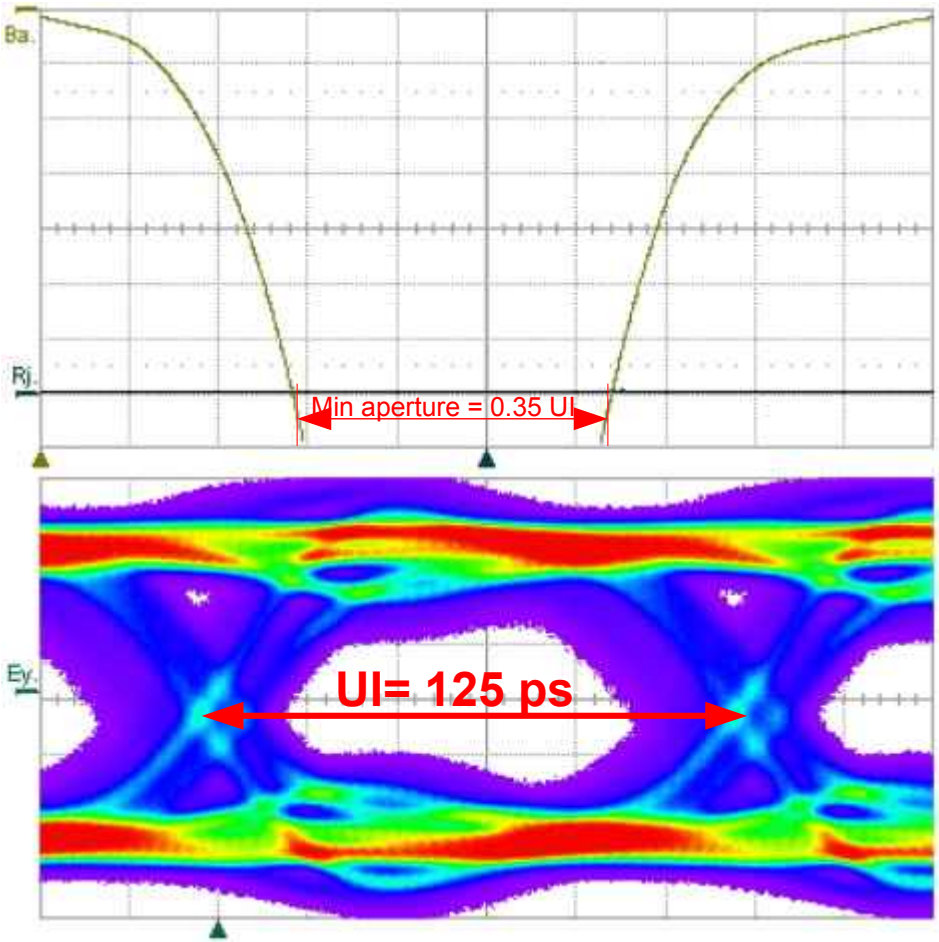
Serial lines at 8 Gbits/s

- **Setup**
  - Implementation of the **GBT protocol**
  - **No preemphasis – No equalization**



Measurements at 8 Gbits/s

Serial link at 8 Gbits/s with GBT protocol



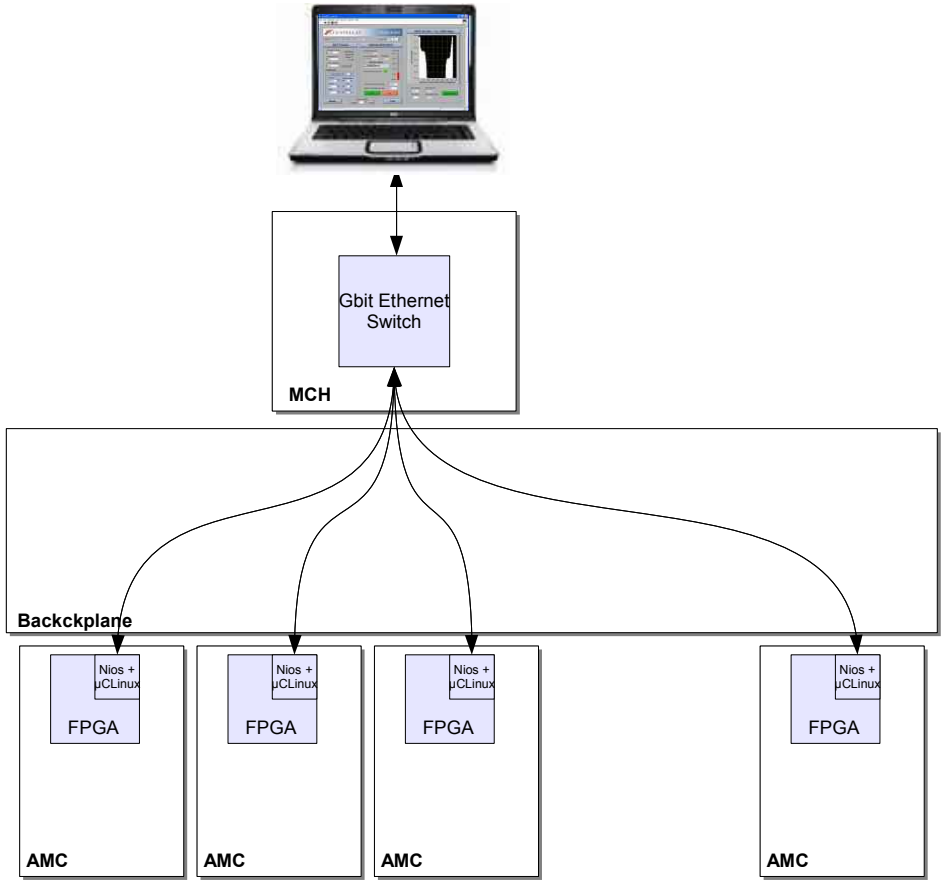
- **Measured jitter at 10^{-12}**
  Total : **77 ps (p to p)**
  Random : **3.0 ps**
  Deterministic : **36 ps**
- **Estimated error rate :**
  10^{-15} without pre-emphasis or equalization
- Closure of eye diagram: inter symbol interference due to attenuation of high frequencies

Slow control

System control

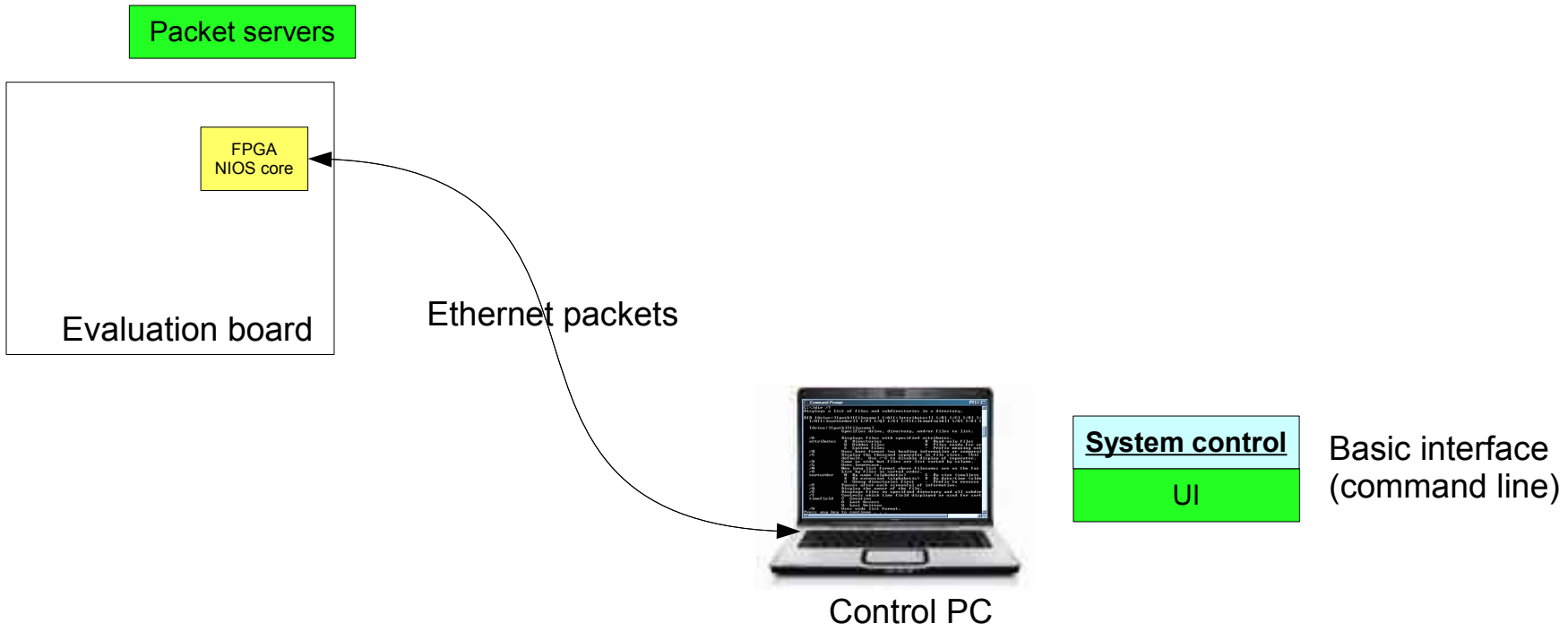
Based on NIOS cores(*) embedded in FPGAs

- Communication through Gigabit Ethernet
- Switch is buried in hardware
- Single control point
- Same Architecture for ATCA or µTCA



(*) NIOS II core = RISC CPU directly embedded in FPGA

TCP/IP packet server running on NIOS II core
Test configuration



Feasibility of a scalable supervision system

- A NIOS core with a triple speed Ethernet interface takes **only 4%** of the logic in a EP4SGX230

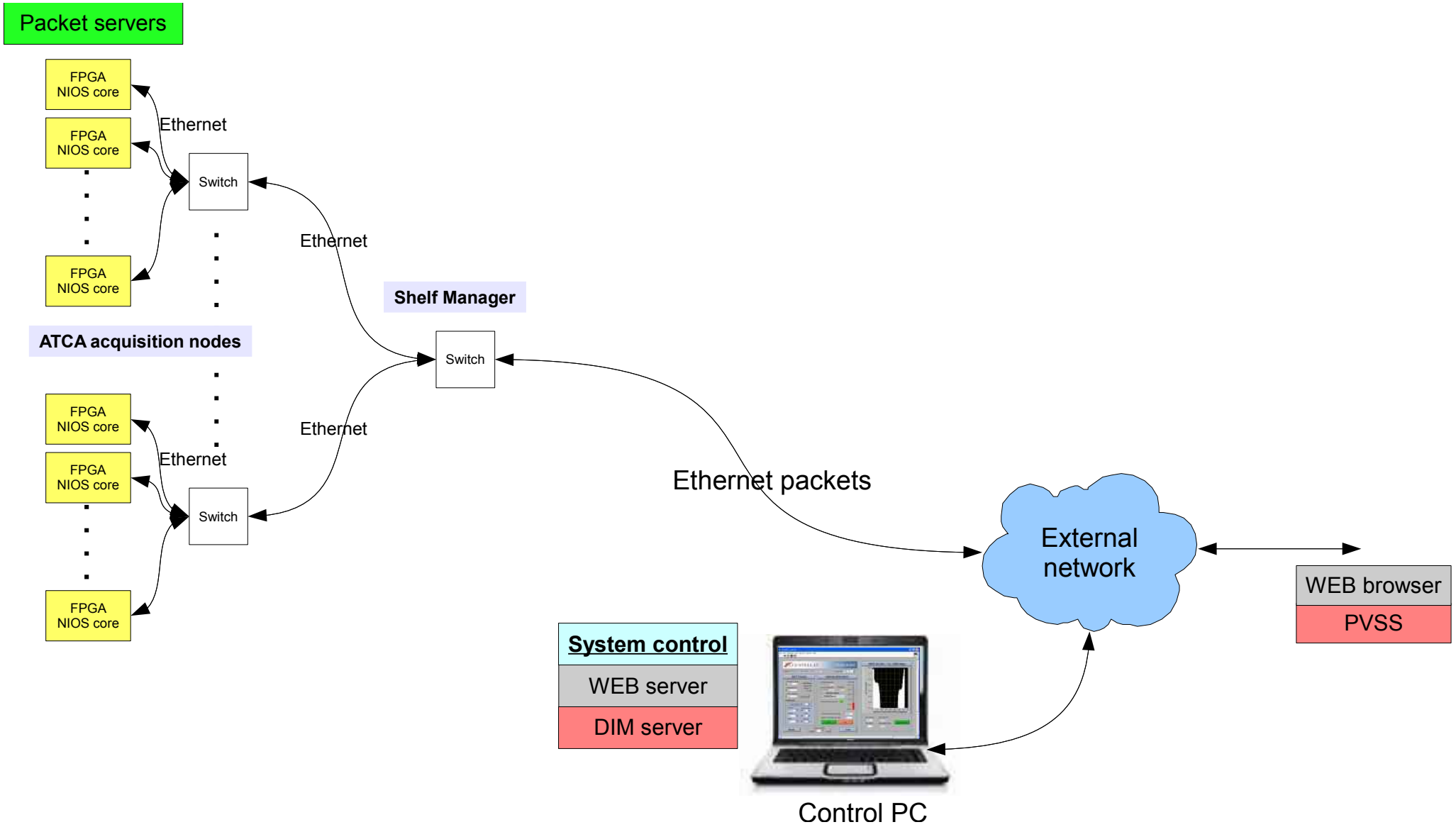
- **Successful implementation of a basic server** running over a microC/OSII realtime kernel.

  Between **1 and 1.8 ms on average per transaction** (several consecutive writes + readbacks) with a simple NIOS core running at 50 MHz.

Packet size	Nb of transactions/s	Nb of tranfered bytes/s
1	943	1886
500	767	767000
1000	647	1294000
1458	568	1656288

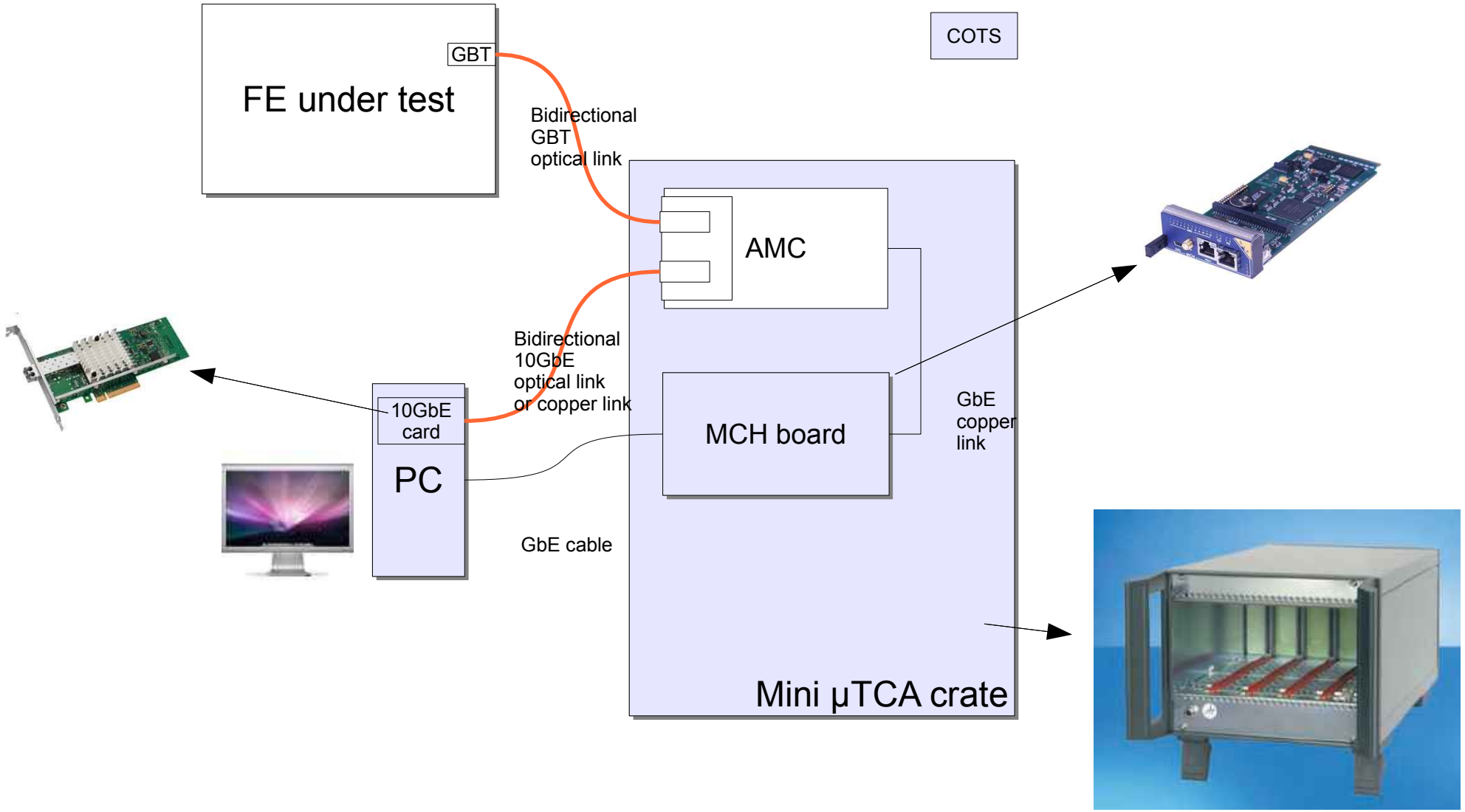
- **Implementation of µCLinux + Dim server**

TCP/IP packet server running on NIOS II core High level interface



Scalable read-out architectures

Mini Read-Out
For FE debug & test



Data acquisition at 40 MHz

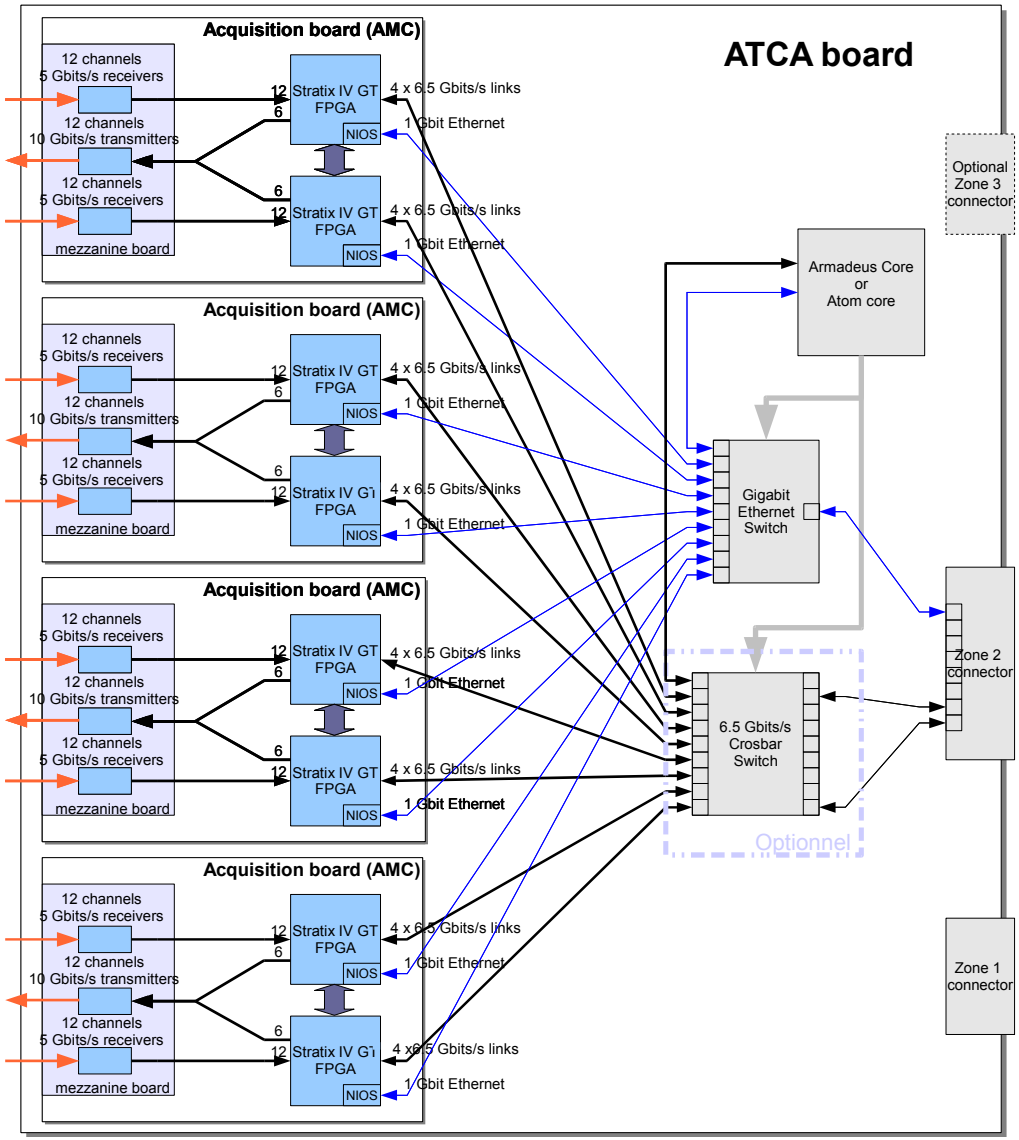
from FE

96 GBT channels IN
4.8 Gbits/s per channel
Effective bandwidth = 307 Gbits/s

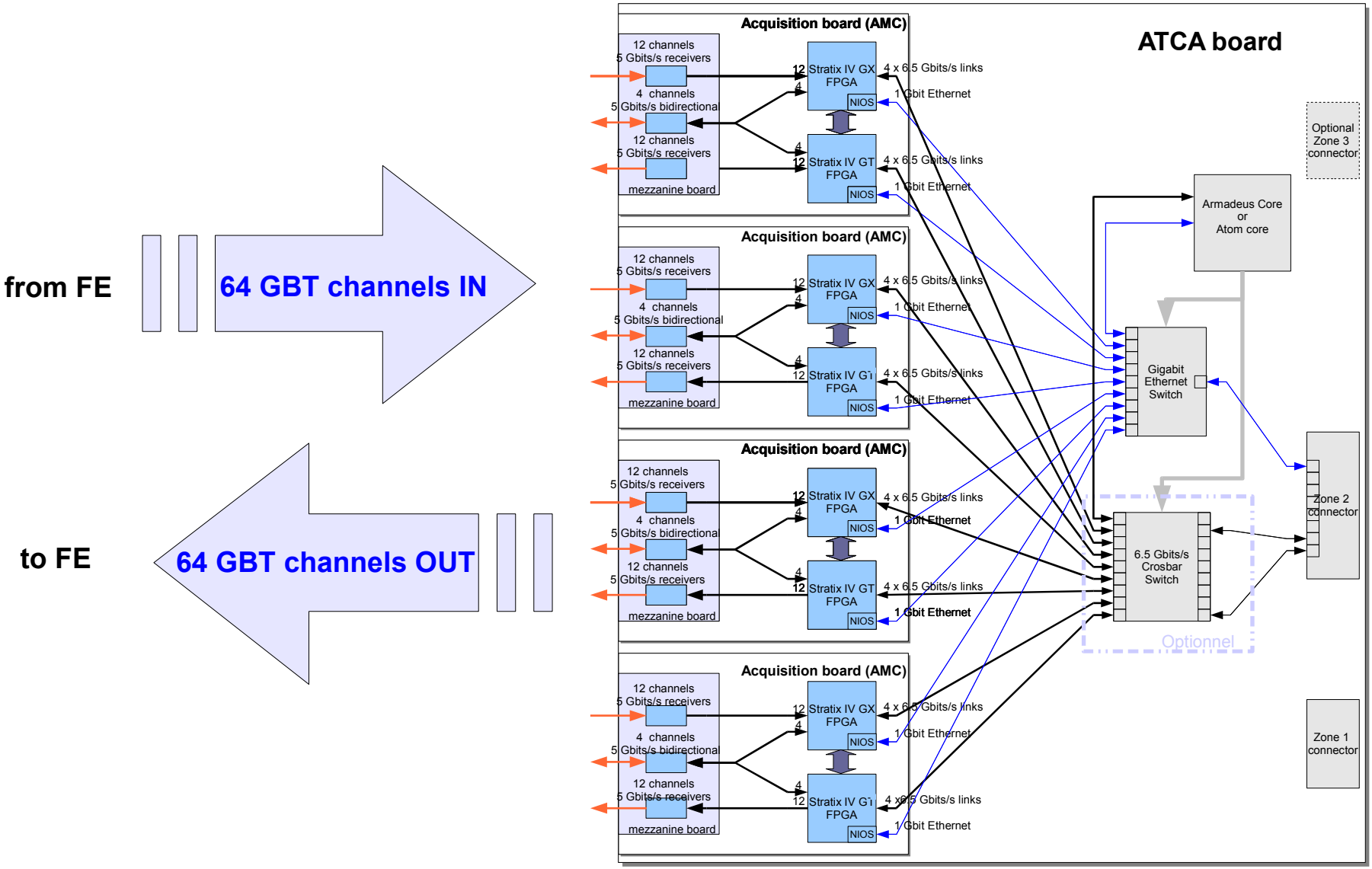
to switches/ farms

48 GbE channels OUT
10 Gbits/s per channel
Effective bandwidth = 441 Gbits/s

9500 links from FE
⇨ **100 boards**



Slow control / Time distribution



Conclusions

- Study on signal integrity is on-going
  - Serial links at 4.8 and 8.5 Gbits/s are OK
  - Pre-emphasis and equalization should allow to increase speed up to 10 Gigabit/s
  - New version of the board with Stratix GT running at 10 Gbits/s soon available.
- xTCA system can be used to build scalable architectures for LHCb upgrade
  - Advantages of a standard: mechanics, COTS systems, interoperability, ...
  - Star topologies present in the standard might help for time distribution, slow control and communications between boards.
- Mezzanine concept allows flexible reconfiguration of boards
  - Quick redesign at low cost
- Supervision system based on NIOS cores embedded in FPGAs is very promizing