Electronics for the European XFEL: AGIPD a high frame rate camera

Peter Göttlicher, DESY, Hamburg, Germany

for

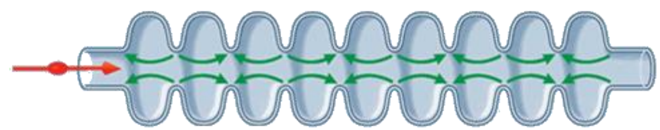
AGIPD collaboration,

Bonn-Univ.,
DESY
Hamburg-Univ,
PSI

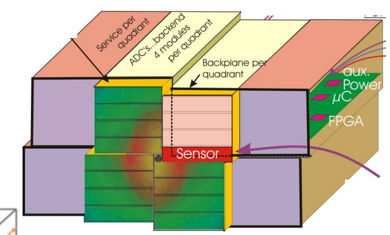
TWEPP 2010, Aachen, Sept. 20th 2010

Outline

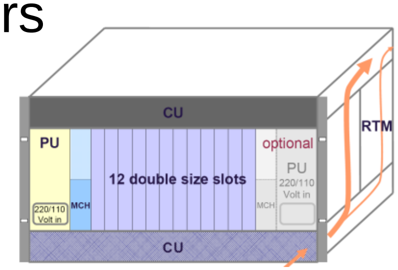
- Motivation for new **X**-ray sources and detectors
- **X**-ray **F**ree **E**lectron **L**aser: Sources of the new 4th generation
  European XFEL



- Detectors
  2 dimensional cameras,
  one is AGIPD: **A**daptive **G**ain **I**ntegrated **P**ixel **D**etector



- Control and data Acquisition for detectors

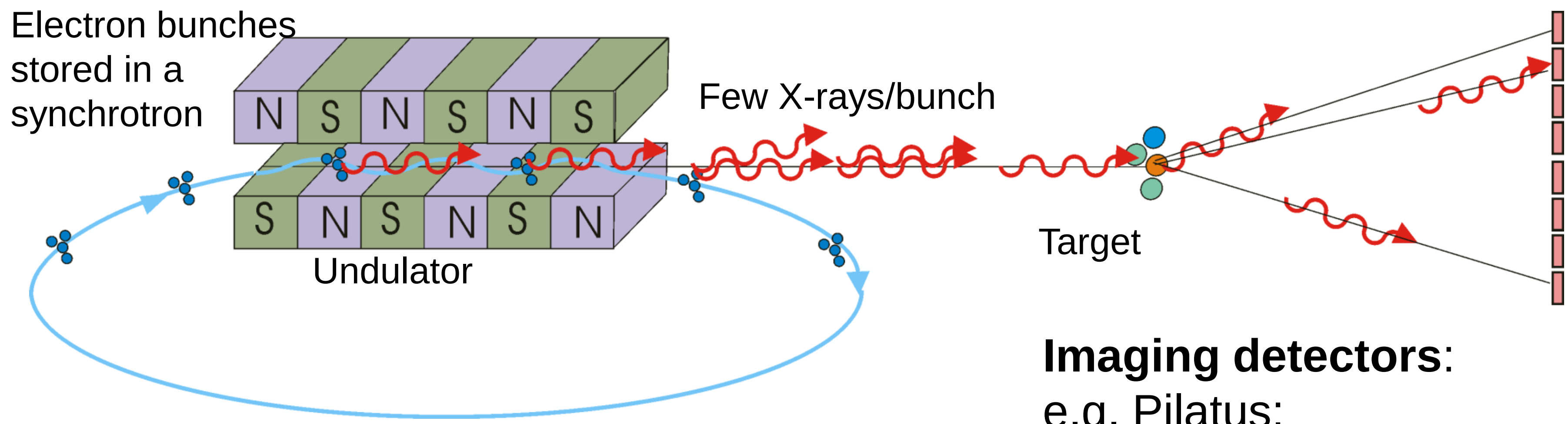


- Status of the project
- Outlook

Outline

- Motivation for new X-ray sources and detectors
- X-ray Free Electron Laser: Sources of the new 4th generation
  European XFEL
- Detectors
  2 dimensional cameras,
  one is AGIPD: Adaptive Gain Integrated Pixel Detector
- Control and Data Acquisition for detectors
- Status of the project
- Outlook

Science with X-ray from nowadays synchrotrons
3rd Generation

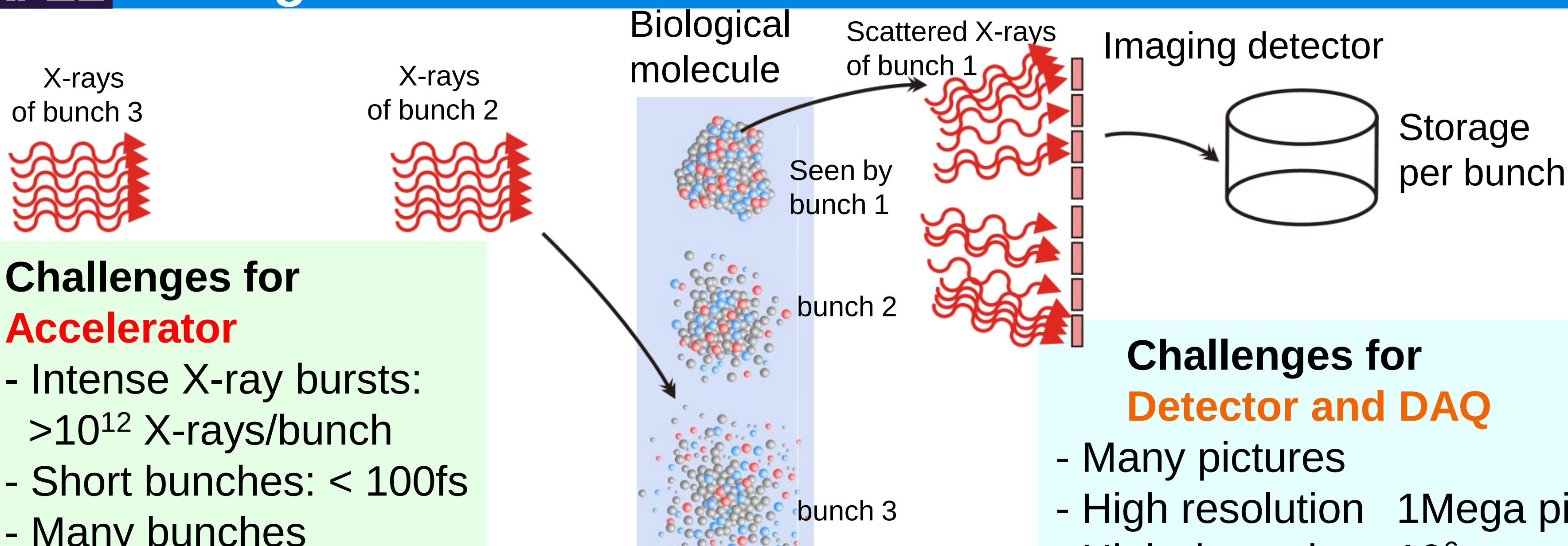


Imaging detectors:
e.g. Pilatus:
2-dimensional pixel
Counting: 1MHz/pixel
Rate: 10-100 pictures/sec

> Nice systems, but more wishes for the future

- Intensity
- Coherence for holography
- Many photons/bunch in <100fs:
  $\Rightarrow$ Get the picture before X-rays destroy the target

Dream of users : Challenges for the designers
4th generation



Challenges for Accelerator
- Intense X-ray bursts: $>10^{12}$ X-rays/bunch
- Short bunches: < 100fs
- Many bunches 27k/s @ XFEL

Challenges for Target
- Fast cleaning
- Fast exchange

Challenges for Detector and DAQ
- Many pictures
- High resolution 1Mega pixel
- High dynamics 10^6
- Fast repetition 220 ns
- High data rates ~80 Gbit/s

> All that effort will open new opportunities for science

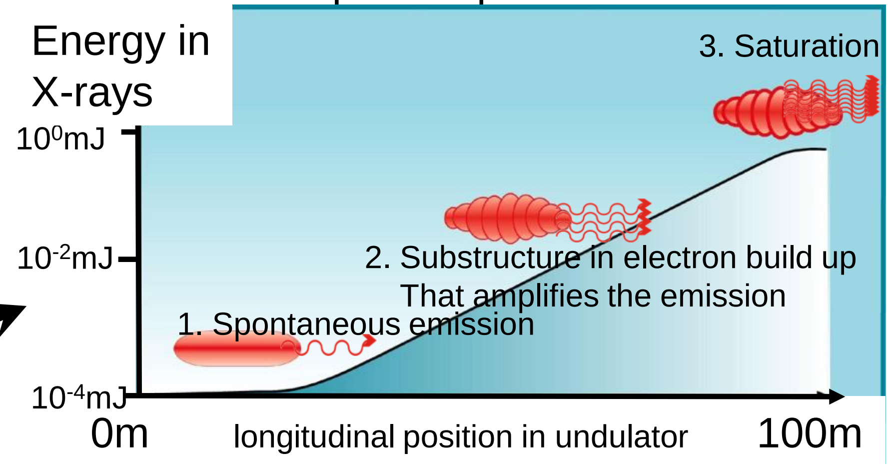
- Structure and dynamics in complex systems: Molecules, clusters, biological objects, plasma
- Physics, chemistry, material science, biology, medicine

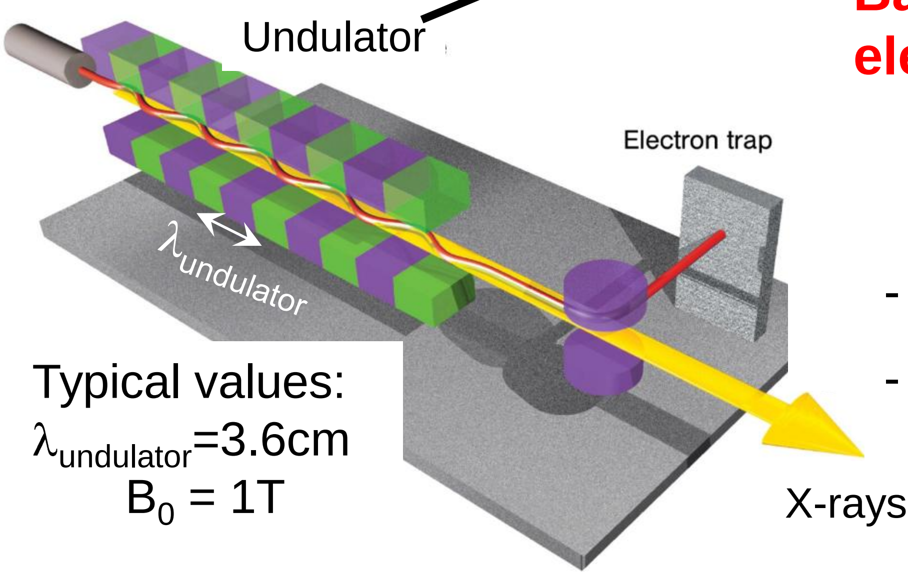
The technique to realize: Free Electron Laser

Lasing for X-ray FEL's needs
very dense electron bunches
at moderate energies

The SASE principle

Self amplified spontaneous emission





Typical values:
$\lambda_{undulator}$=3.6cm
B_0 = 1T

Basic requirements, for electron source and accelerator

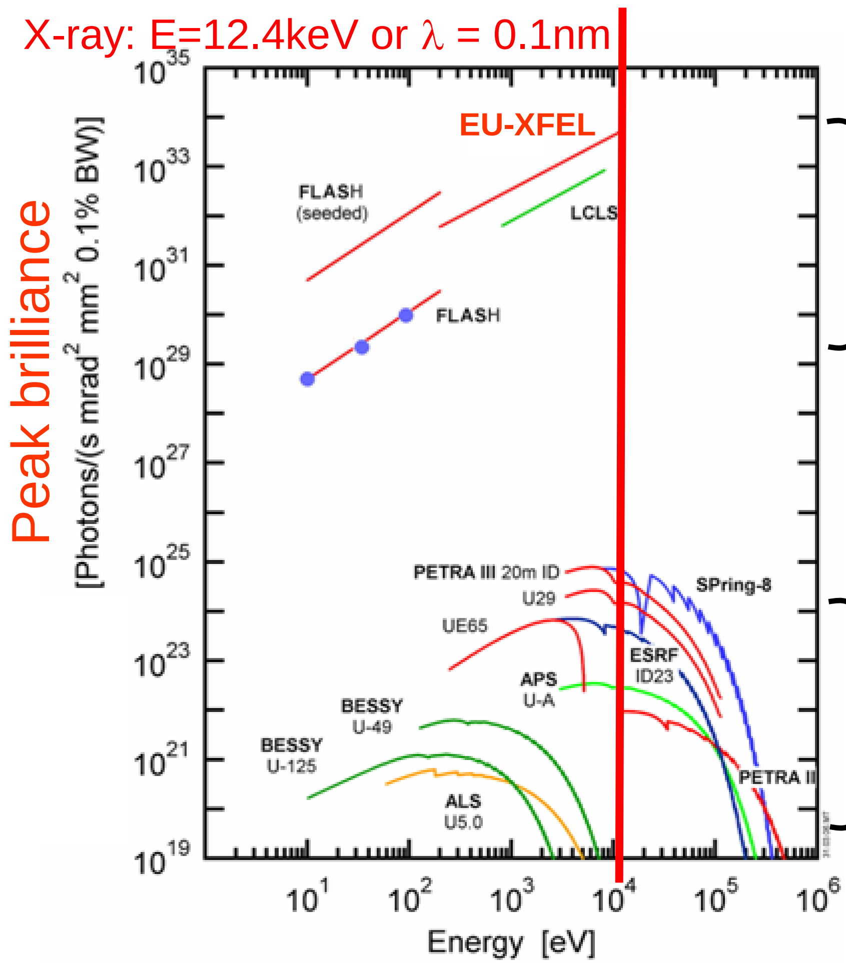
$$\lambda_{X-ray} = \frac{\lambda_{undulator}}{2\left(\frac{E_e}{m_e c^2}\right)^2}\left(1+\frac{K^2}{2}\right) \quad with \quad K = \frac{eB_0\lambda_{undulator}}{2\pi\, m_e c} = 1...10$$

- Wavelength 0.1nm: **17.5GeV** electrons
- Power grows with current density $\propto e^{\sqrt[3]{j}}$ ....
  Short bunches ~20µm with Q=1nC
  20µm converts to 70fsec

Comparison: From synchrotrons to FEL's

Intense light gets delivered by lasers,
now lasing for X-ray

X-ray: E=12.4keV or λ = 0.1nm



FEL based sources

LCLS: Operation since 2009: X-ray
SLAC, USA

SCSS: Planned for 2011, X-ray
Spring-8, Japan

FLASH: Operation since 2005: VUV-light
DESY, Germany
User-operation and
test facility for XFEL

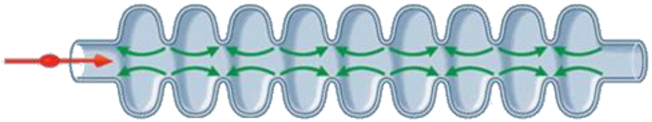
European XFEL: Construction until 2014/15: X-ray
DESY, Germany

Synchrotron based sources

9 orders of magnitudes
Good reason to build new accelerators

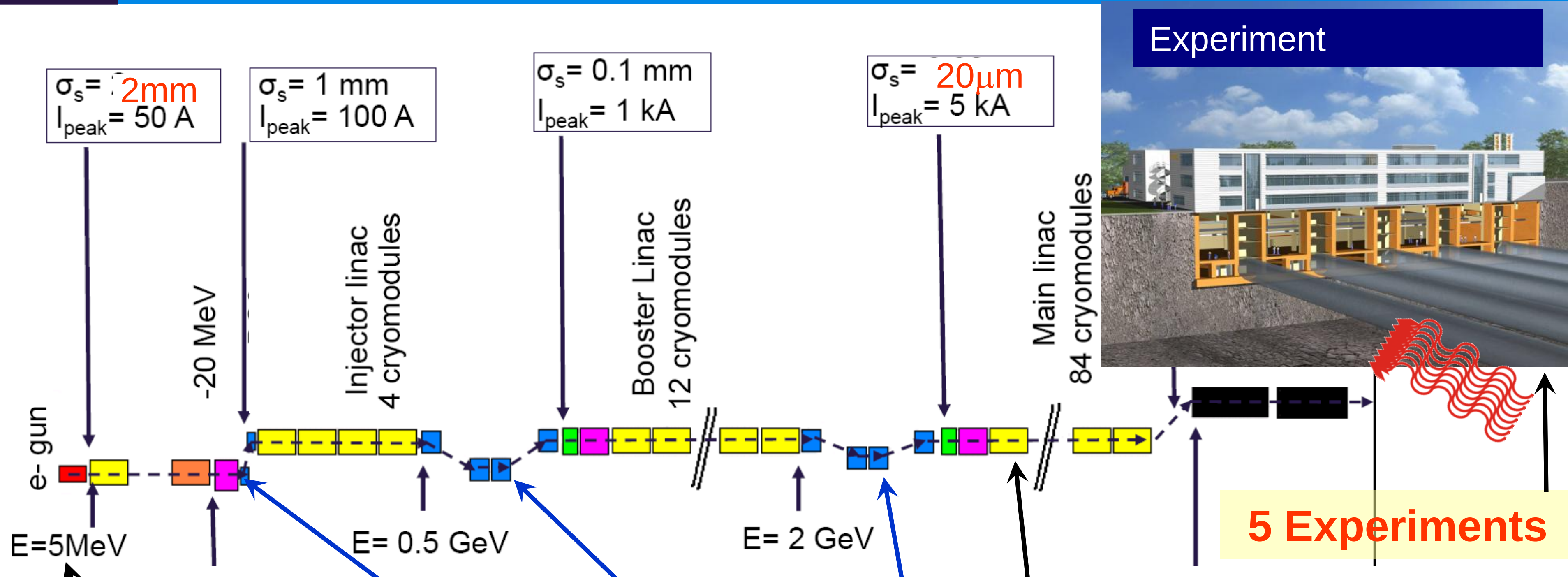
Outline

- Motivation for new X-ray sources and detectors
- X-ray Free Electron Laser: Sources of the new 4th generation
  European XFEL



- Detectors
  2 dimensional cameras,
  one is AGIPD: Adaptive Gain Integrated Pixel Detector
- Control and Data Acquisition for detectors
- Status of the project
- Outlook

XFEL: Functional blocks



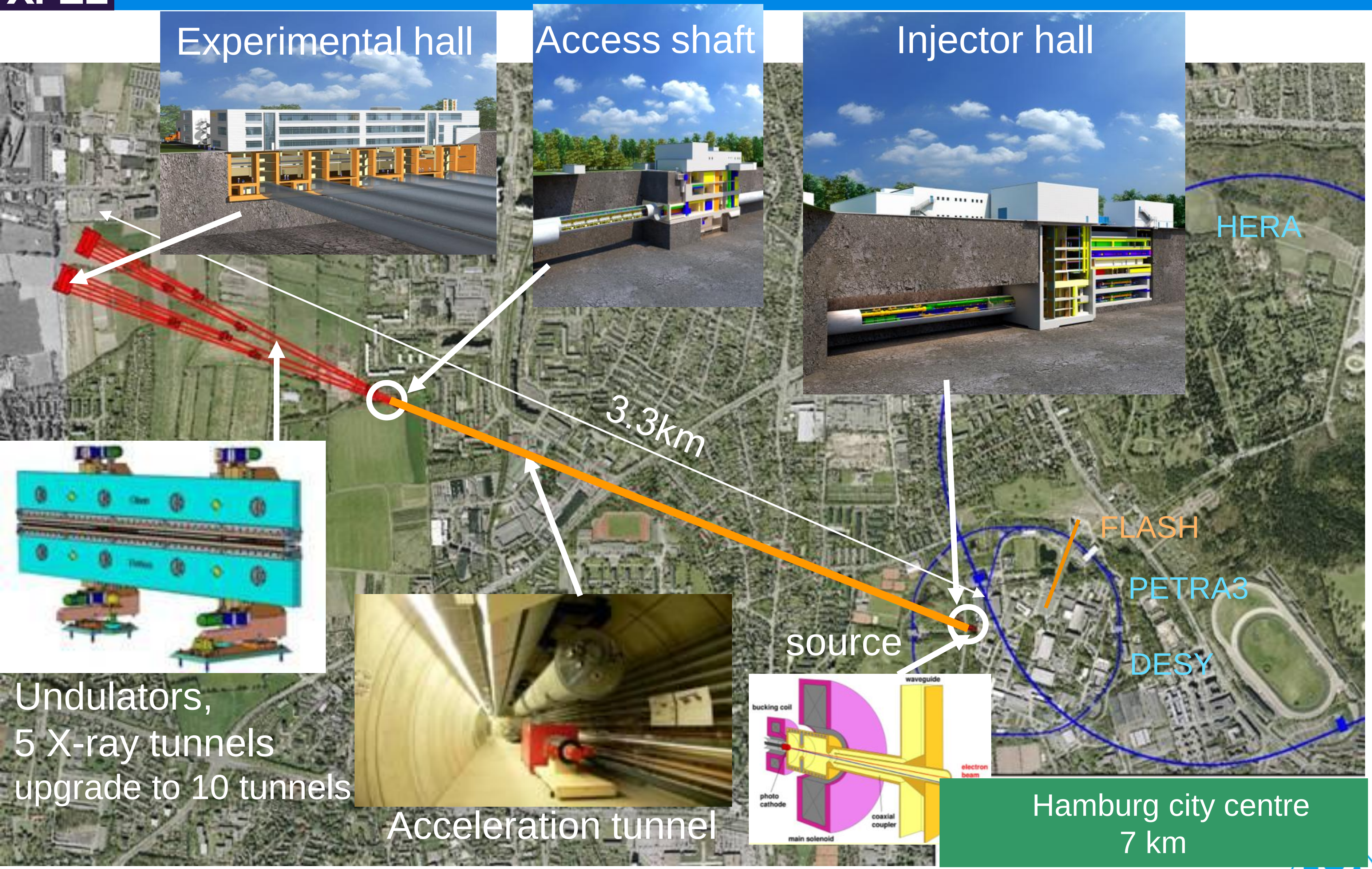
Electron-source:
- Laser to a photo cathode
- Immediate acceleration

Bunch compression
- Position to energy
- Different path-length through magnetic chicanes

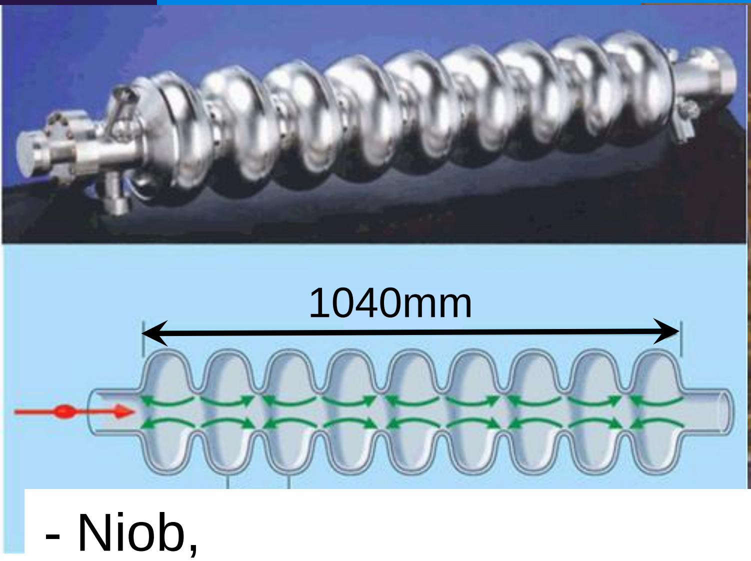
Undulators

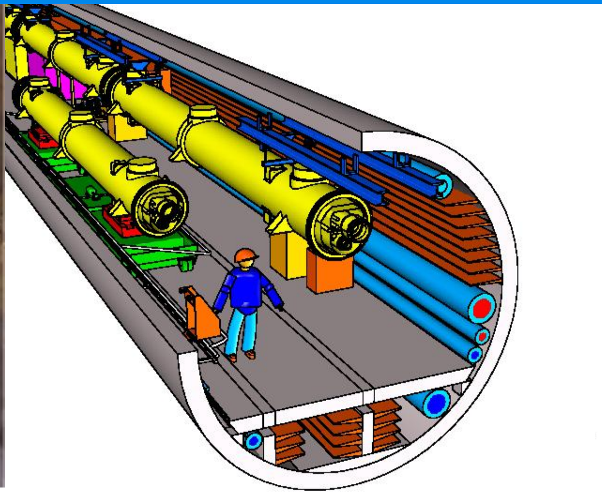
Acceleration
By superconductive RF-cavities: 1.3GHz

The European XFEL:



The Cavity





- Niob,
- electro polished

Operating conditions:
- RF frequency 1.3 GHz
- accelerating field 20-25MV/m
- superconductive, T=2K

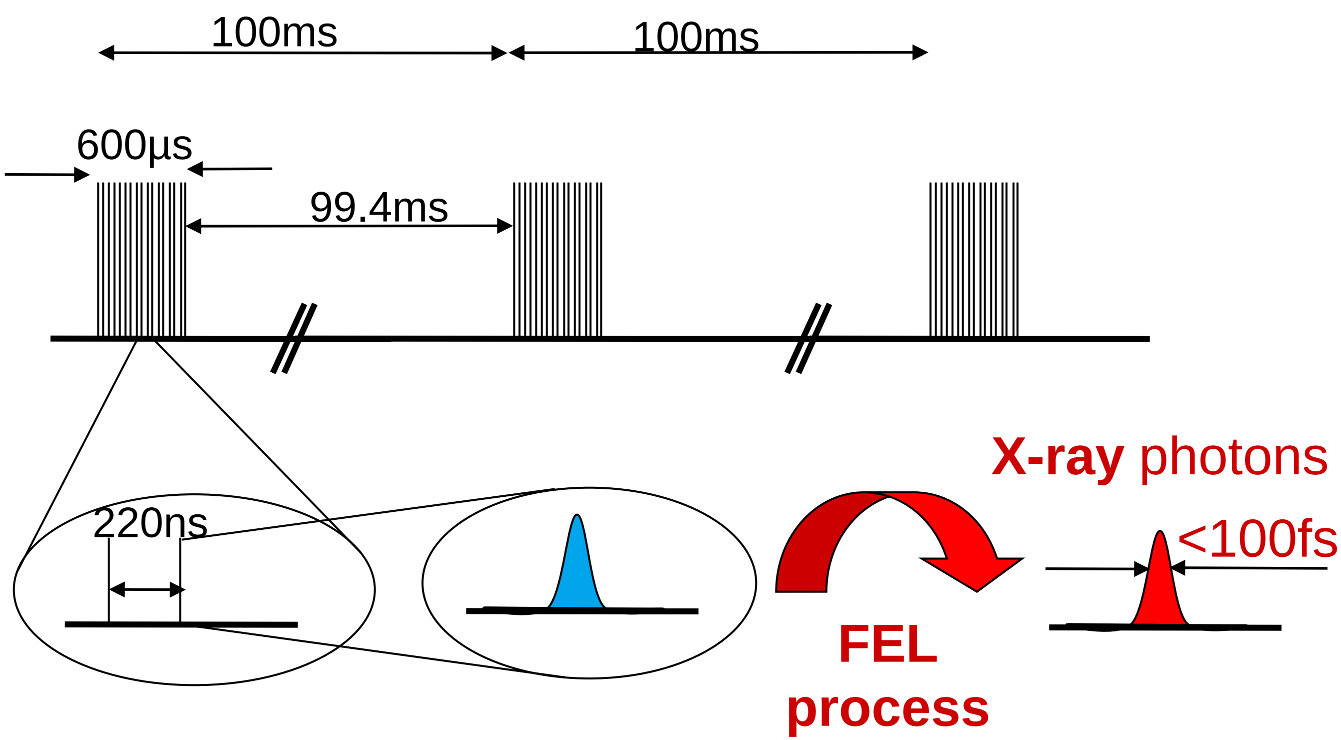
Heat production
- Need duty cycle:
  600μs e-beam with 10Hz
  ⇒ bunches in trains

Cryostat with
- 8 cavities
- quadrupol magnet,
- couplers
- diagnostics

101 cryostats in the tunnel

Contracts for 600 cavities signed with industry
Kick Off: September 7th 2010

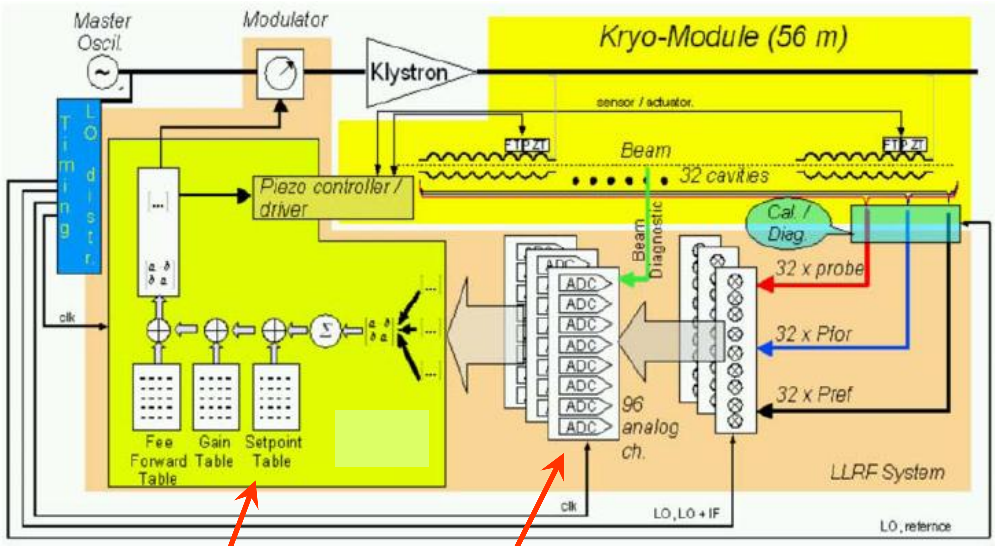
Train structure



- **>** Advantage: 27 000 bunches/sec,
  LCLS,SCSS: 60-120 bunches/sec
- **>** Consequence: All systems have to handle 220ns bunch to bunch 4.5MHz operation for 27k-bunches/sec.

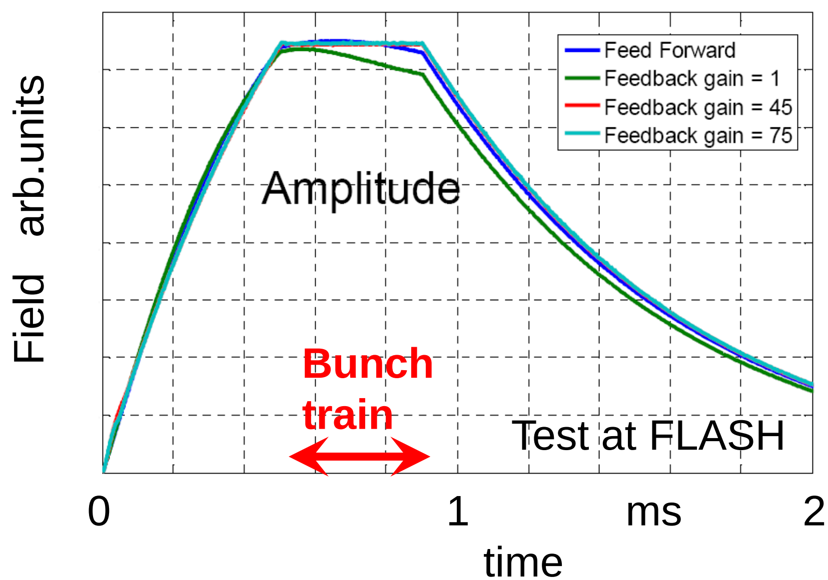
LLRF: Radio frequency control

W.Koprek, LLRF09, Tsukuba, Japan, EuCARD-PRE-2009-003



Train structure:

- Charging cavities: 10Hz for 2ms
  pulsed Lorentz-force detuning
- Load by beam pulsed: 600µs @ XFEL
  field energy used to accelerate e^-,
  control of recharging
  constant field during train
- Compact bunches: Very stable field
  Amplitude 0.01 %
  Phase 0.01 ^{0}
  at injector



96 analogue information's
ADC's: 14bit, ~100MS/s

Complex mathematics:

- feed back loops
- feed forward during train, train to train
- low latency: few 100ns

⇒ FPGA's, DSPs, high data throughput
⇒ high performance data links

xTCA as platform

K. Rehlich, IEEE-Real-Time conf. 2010, Lisboa, Portugal

High performance digital standard: Telecommunication

- ATCA: Advance Telecommunication Computing Architecture: 2002

Features:

- Backplane: many multi gigabit serial links
- Configurable network
- Redundancies: Power, CPU, MCH
  Uptimes >99.999%
- Carriers for 1-8 AMC
  Advance Mezzanine Cards
- Hot swap

µTCA

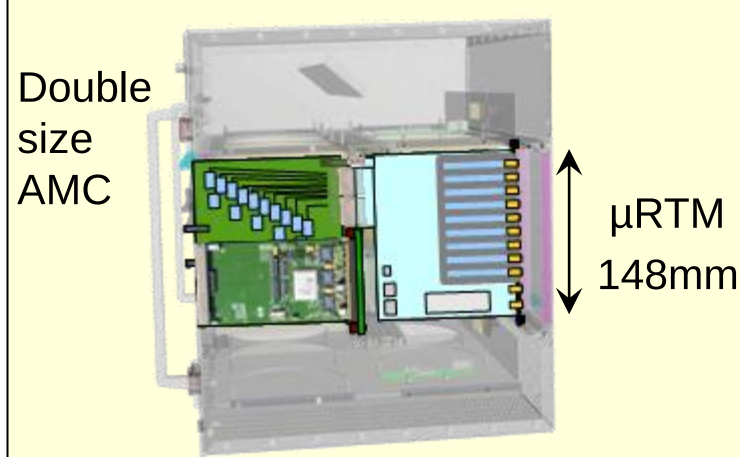
Scalable to
- Small systems
- Features like ATCA
- modules = AMC's

A standard for physics

- Science(European XFEL)+ Industry
  PICMG® Specification MTCA.4

Features:

- Based on µTCA
- More space
- Synch. clocks on backplane
- Rear access by µRTM's
  µRear Transition Modules

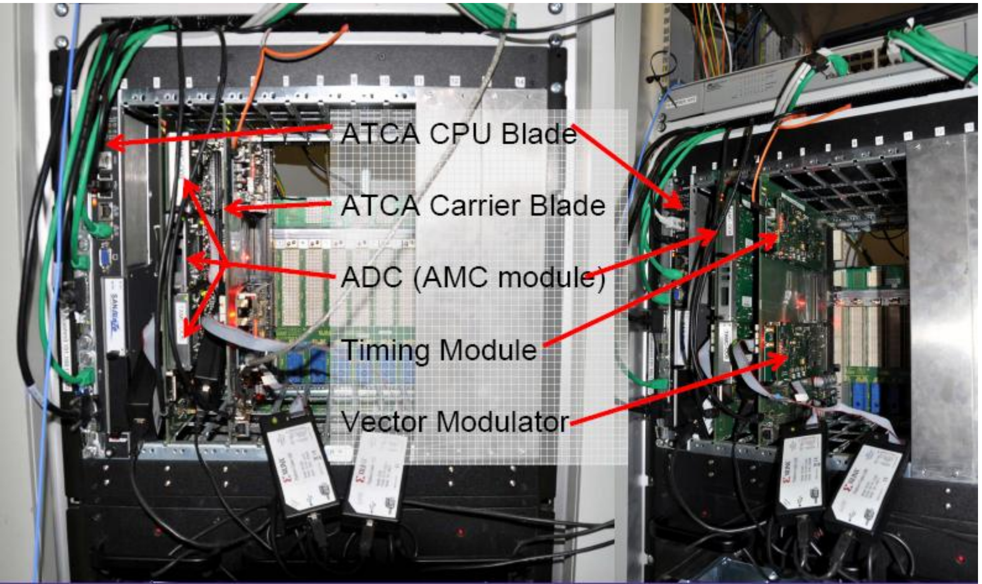


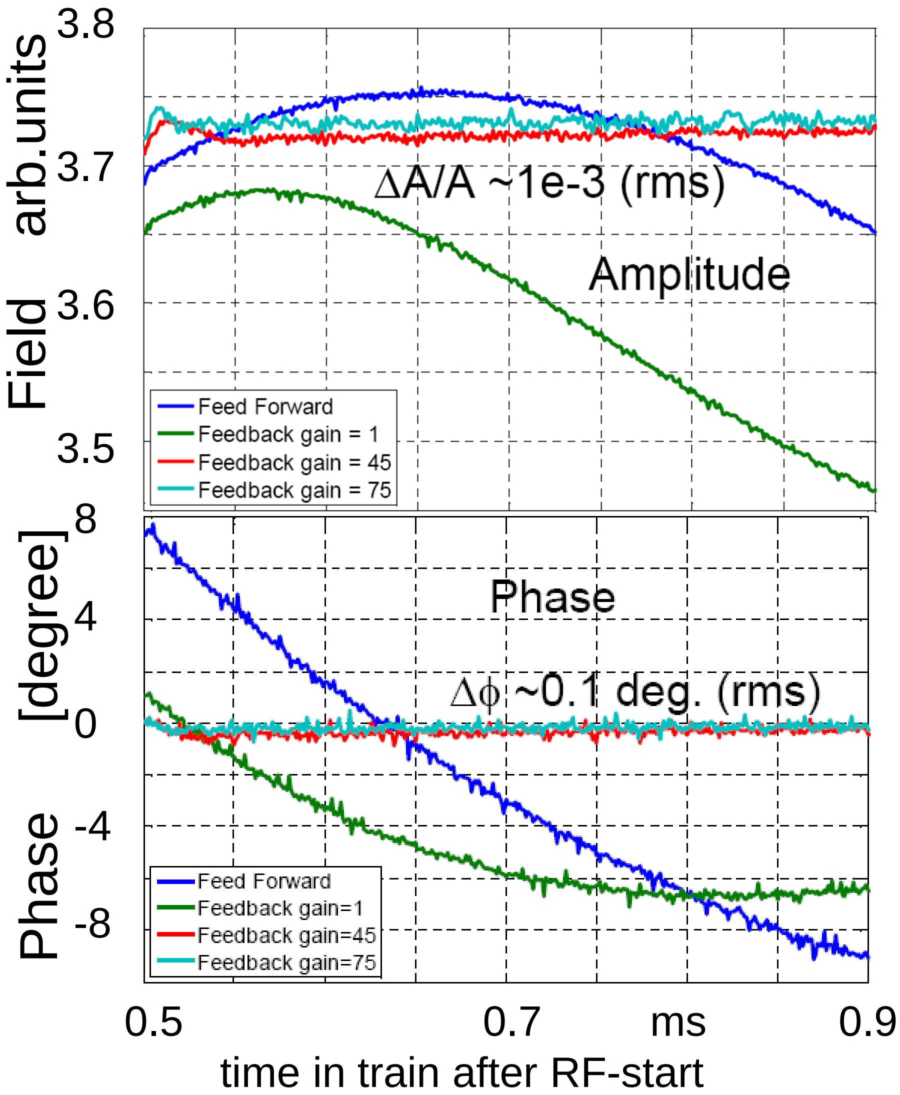
LLRF: ATCA trials at FLASH, main accelerator

W.Koprek, LLRF09, Tsukuba, Japan, EuCARD-PRE-2009-003

Prototyping and first trials with ATCA

Stability needs regulation with:
- Feedback and feed forward,
- High amount of fast data handling



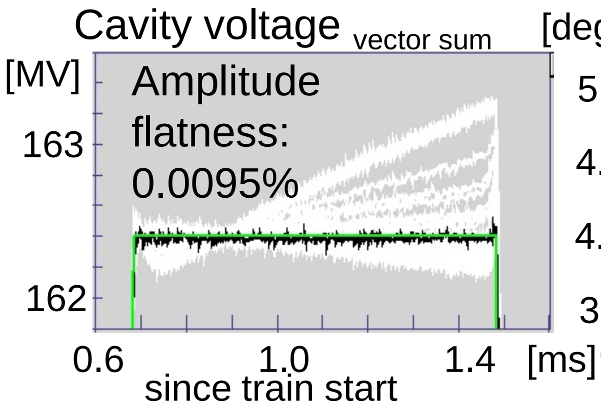


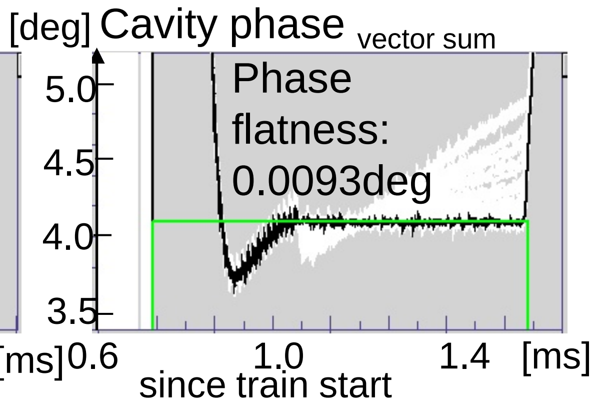
LLRF: Injector Performance at FLASH

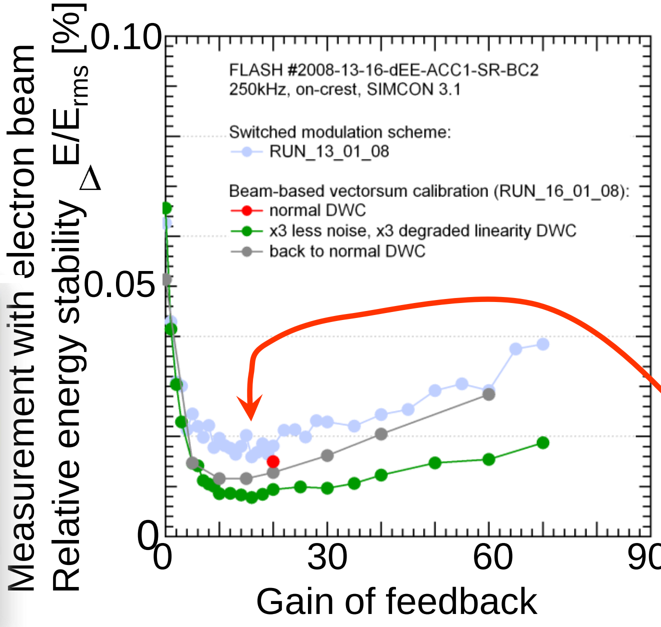
C.Schmidt, F. Ludwig, et. al.

Today's system

Learning **Feedforward** Performance: Pulse-to-Pulse (ACC1)







Feedback:

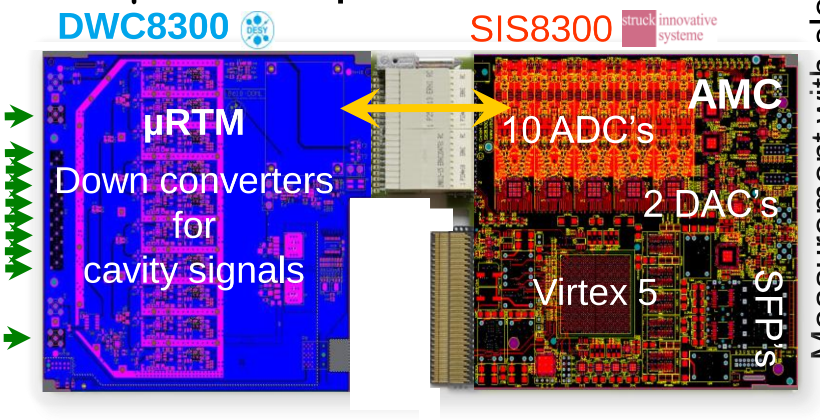
Optimized between
- high for regulation
- low for sensor noise

Requirement reached:

$\Delta E/E|_{e\text{-beam}} = 0.008\%$

Next generation:

µTCA in production

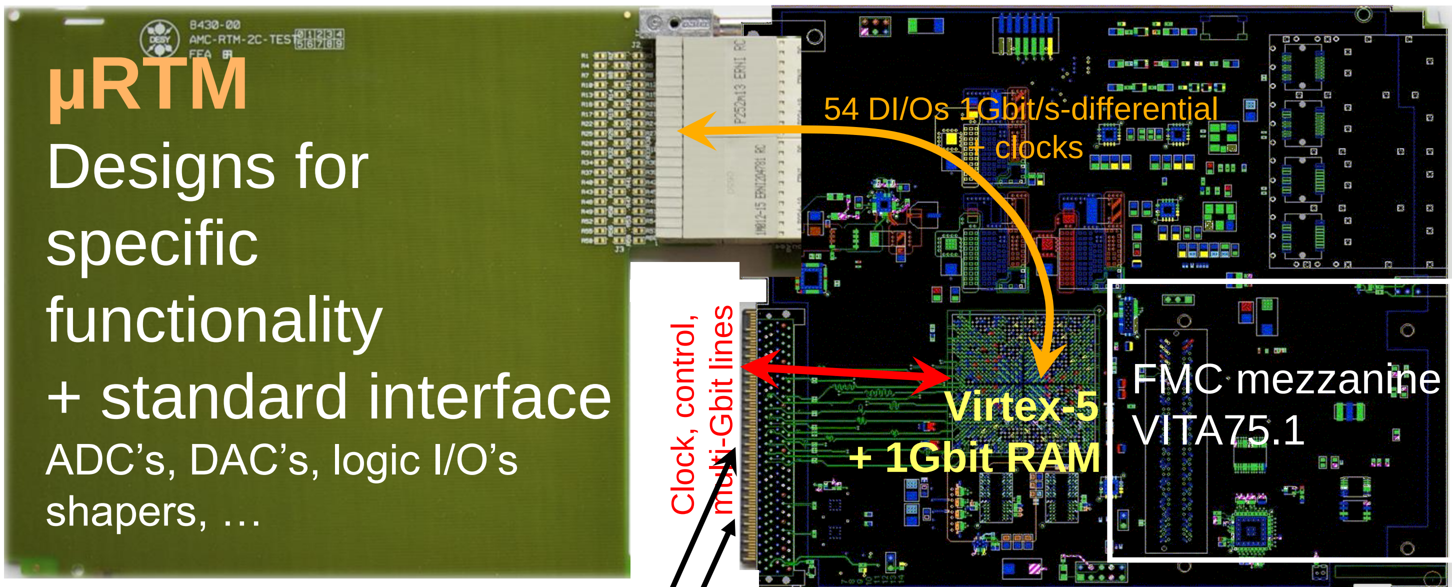


XFEL standardization of AMC boards

P.Vetrov et al., IEEE-Real-Time conf. 2010, Lisboa, Portugal

DESY AMC 2

In prototype production



Connector to backplane of µTCA-crate:

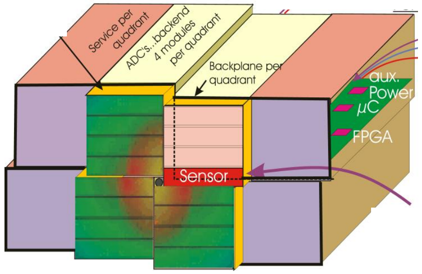
µRTM: Rear transition module
- User specific hardware
- Simpler design

AMC: Front boards:
- double width standard
- A few standard hardware developments: digital interface, ADC's, carriers
- Custom and industrialized designs
- Code as VHDL for hardware drivers application in higher level (MATLAB)

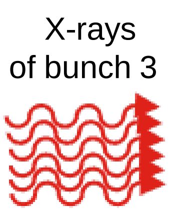
DESY-AMC1
as real prototype
Virtex-5, RAM, 125MS/s ADC's and DAC's

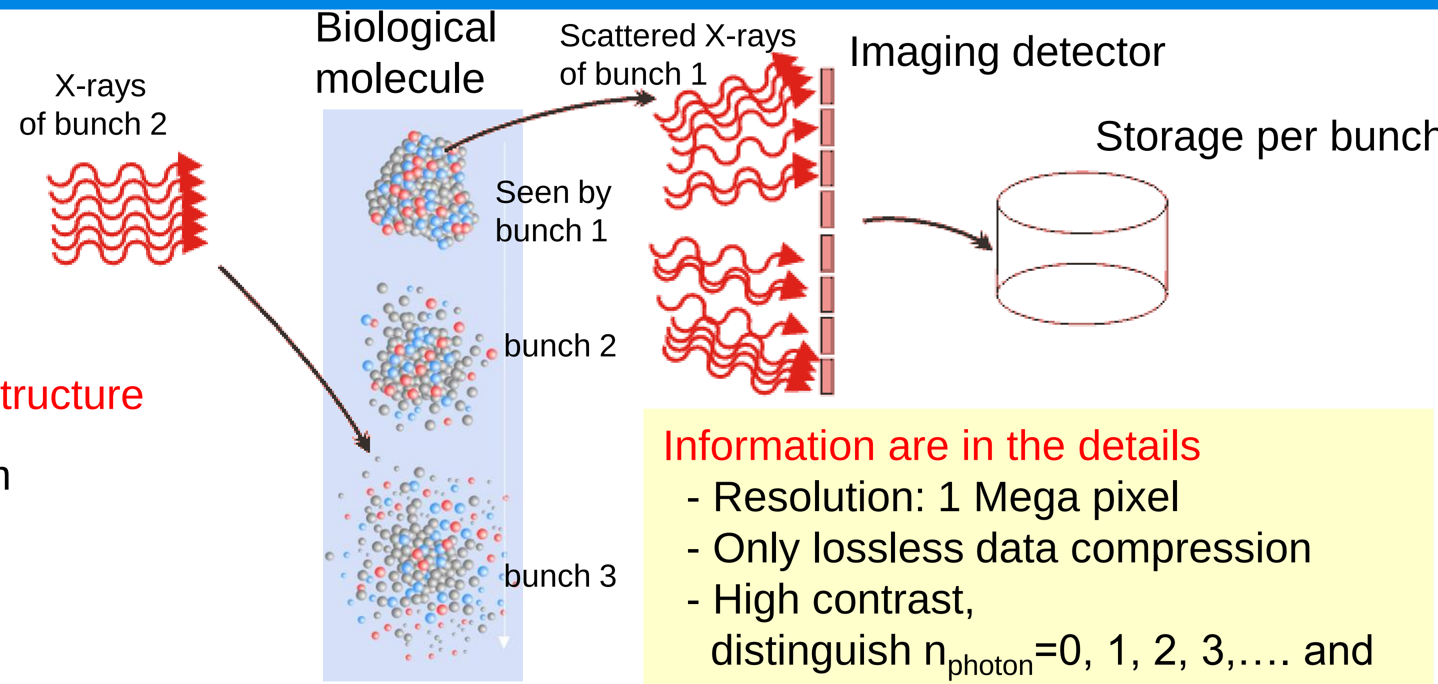
Outline

- Motivation for new X-ray sources and detectors
- X-ray Free Electron Laser: Sources of the new 4th generation European XFEL
- Detectors
  2 dimensional cameras,
  one is AGIPD: Adaptive Gain Integrated Pixel Detector
- Control and Data Acquisition for detectors
- Status of the project
- Outlook

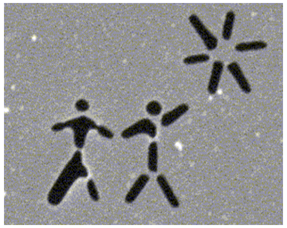


Detectors for the dream: 2-dimensional cameras



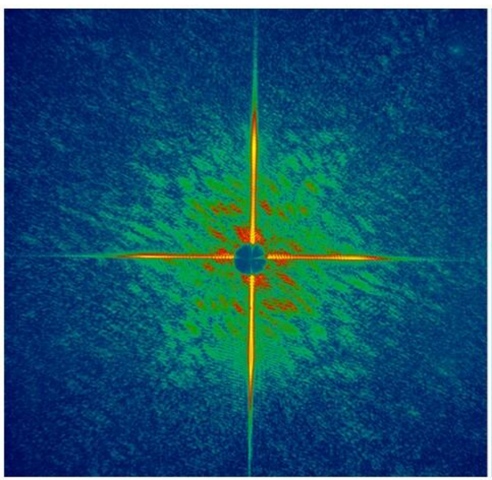


Picture of a nano-structure

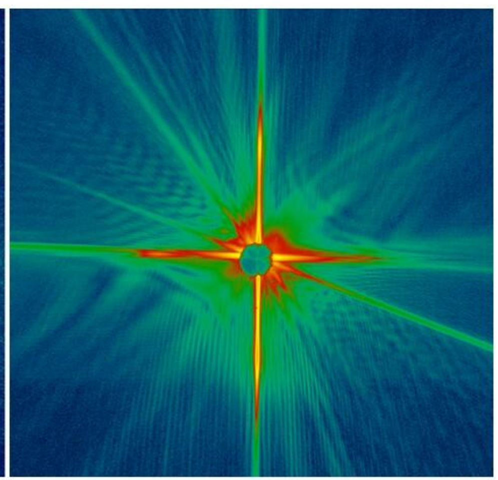


Taken at FLASH

First hit



melted foil



Information are in the details

- Resolution: 1 Mega pixel
- Only lossless data compression
- High contrast,
  distinguish n_{photon}=0, 1, 2, 3,…. and
  for high signals statistical limit

$$resolution < \sqrt{n_{photon}}$$

- Many pictures, but objects differ
  e.g. in position/orientation x,y,z,θ,φ
- Complex analysis before combining,
  only offline?

Consequences:

- Need to store every 220ns a picture
- Select the best ones to reduce to
  reasonable data volume 80Gbit/s

User requirements

Unit, Order of magnitude

		Different physic cases				
		Pump/probe none crystalline	Pump/probe crystalline	Coherent diffractive imaging	Single Particle Imaging	X-ray Correlation Spectrosc.
Photons and radiation						
E_{photon}	keV	6-15	12	0.8-12	12.4	6-15
Quan. Effic.	%	> 80				
Rad. Toler.	10^{16} photons	1	1	2	0.2	0.02
Geometry						
Camera size	Target-angle	200^0	120^0	120^0	120^0	0.2^0
Pixel size	Mrad	7	100µm	0.1	0.5	0.004
No. of pixels	kilo x kilo	0.5 x 0.5	3 x 3	20 x 20	4 x 4	1 x 1
Dynamics for sensor and electronics						
Local rate	10^4 photons /pixel/picture	5	300	10	1	0.1
Global rate	10^7phot./pict	3	1			
Noise		Single photon resolution, << statistics				
Phot. spread	**pixel**	<1	<100µm	<1		
Picture rate	/train, /time	1, 10Hz	1, 10Hz	All, 27kHz	1, 10Hz	All, 27kHz

Requirement to detector:

500 µm Si

Exceed 1GGy at sensor surface

Pixels 100-500µm
Target-detector: 1-5 meters
1mega-pixel

Demanding dynamics !

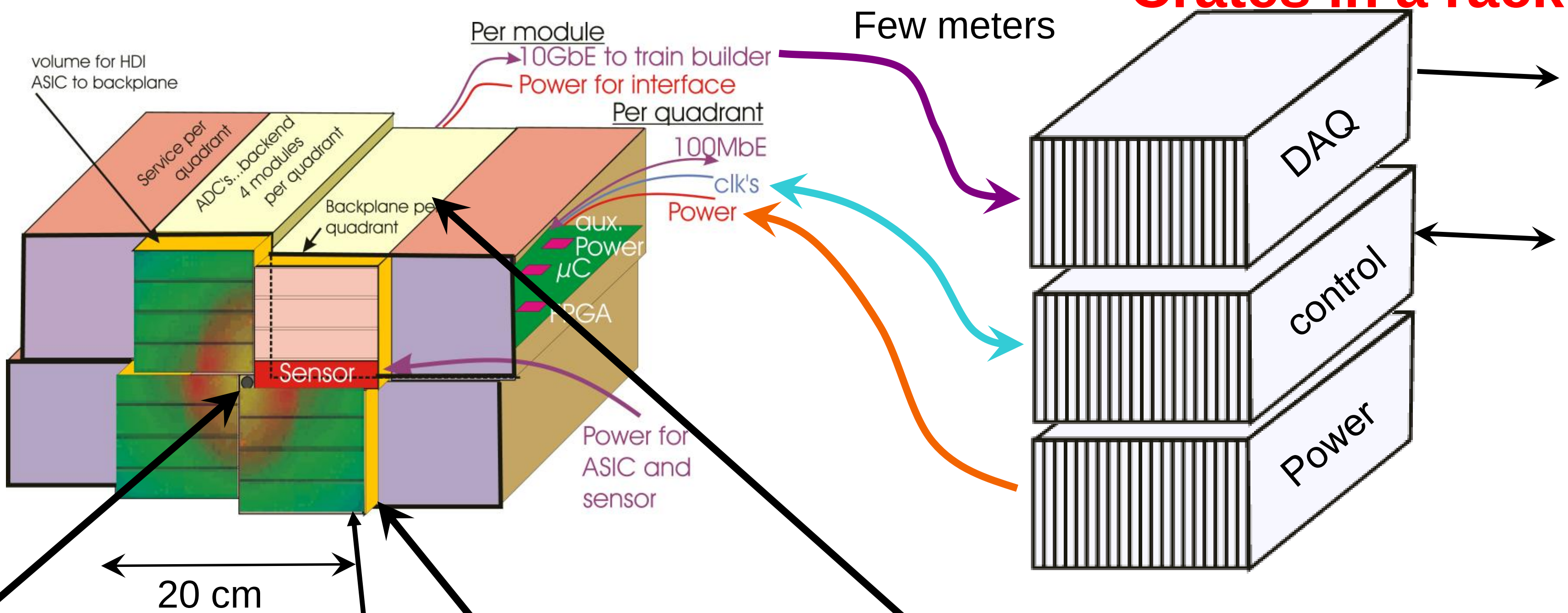
10^9 e-h-pairs in less than a pixel

Possible total?
Pict-pict: 220ns

Need a few detectors to cover all
Same challenges look not feasible: compromises, future

General detector concepts: Mechanical view

Camera head at the beamline ⟷ Crates in a rack



Quadrants
Arrangement with or without a hole for remaining X-rays

Focal plane
Sensors with bump bonded ASIC's, everything until a fast signal storage

Vacuum barrier
Moderate Scattering of X-rays

Board level electronics
- control of ASIC
- data formatting
- power

Analogue, FPGA's, μC
Mechanical depth low importance

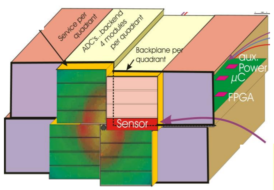
General detector concepts: Electrical and Connectivity

European XFEL

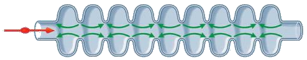
Bump bond/pixel

Copper cables
Clocks, TCP/IP-100MbE

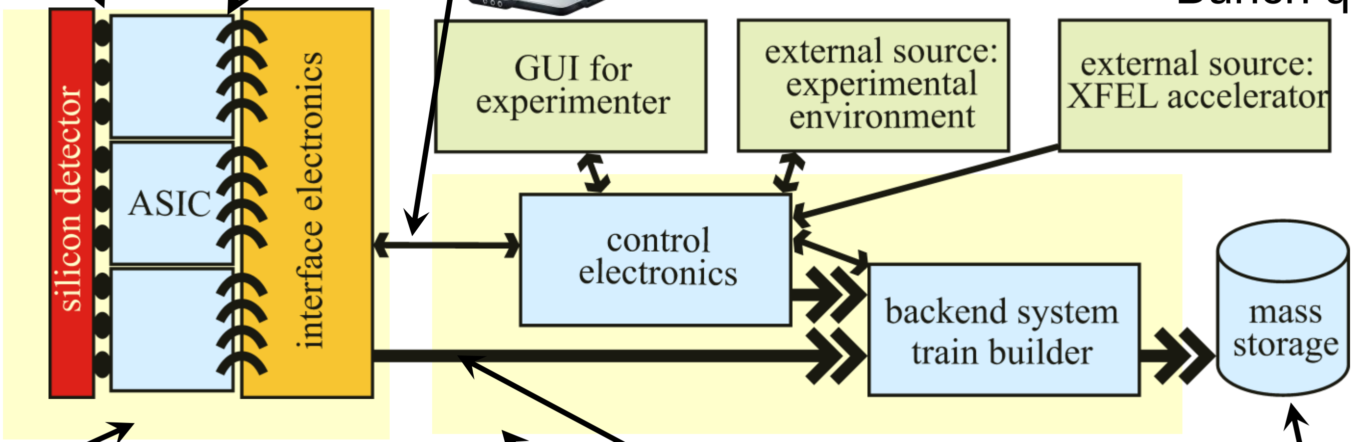
Wire bonds to a
High-Density board



Environment
Scattering quality



Sync. clocks
Bunch quality



Fibre optics
UDP-10GbE

Camera head
- Three consortia for cameras
- Each covering multipurpose science, each not all, all differently specialized

Crates in racks
Common development for all at XFEL-experiments

IT-center

DESY

Three consortia for 2 dimensional cameras

AGIPD

Adaptive Gain Integrated Pixel Detector

Institutes: Bonn(University), DESY, Hamburg(University), PSI(Villingen)

Reference: B. Henrich, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.06.107

DSSC

DEPMOS Sensor with Signal Compression

Institutes: MPI-HLL Munich, DESY, Heidelberg(Univ.), Poly. Milano, Bergamo(Univ.), Siegen(Univ)

Reference: M. Porro, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.02.254

LPD

Large Pixel Detector

Institutes: STFC/RAL, Glasgow(University)

Reference: S.R.Burge et al., Large Pixel Detector for the European X-ray Free Electron Laser, 11th European Symposium on Semiconductor Detectors, June 2009 conference proceedings.

Common items: Sensor-studies, ASIC in 130nm-technology, DAQ-systems

Different physics by different technical approaches

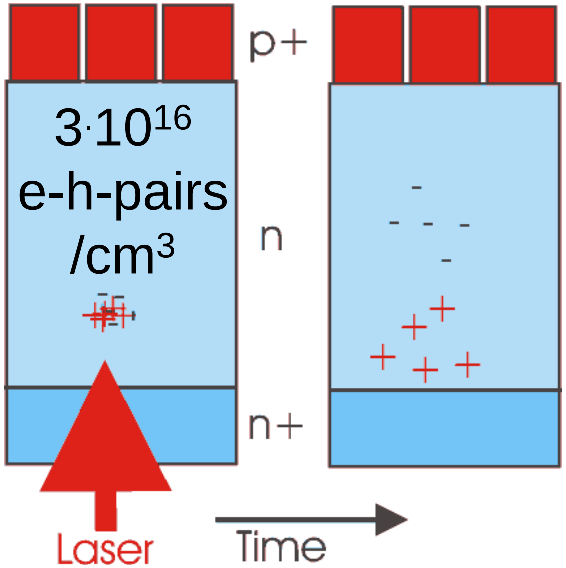
	AGIPD	DSSC	LPD
Pixel	200 x 200µm²	236µm hexagons with a DEPFET	500 x 500µm²
Approach for dynamic range	Automatic gain switching	Compression by DEPFET in pixel	3 parallel gains
Storage per bunch	Analogue with analog ASIC-out.	Digital, 1ADC/pixel	Analogue with digital ASIC-out.

Sensor

J. Becker, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.01.082

Charge explosion:

Electrostatic forces cause
Widening of charge cloud

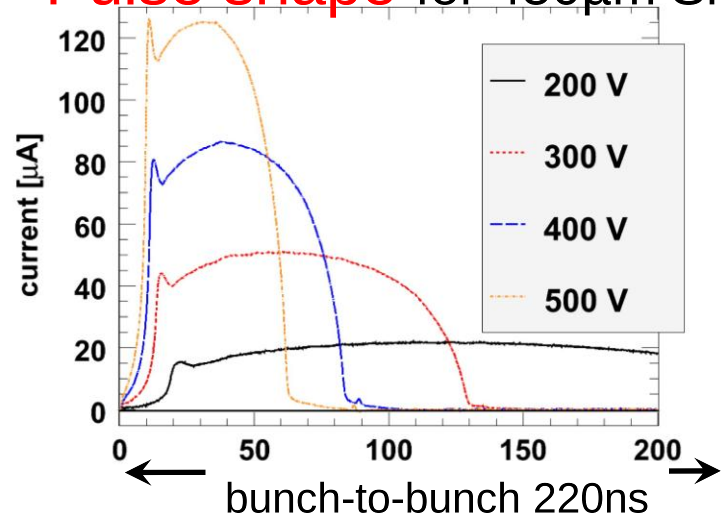


Longitudinal causes
- Tails to next bunch
- Charge losses out of integration time
- Pile up

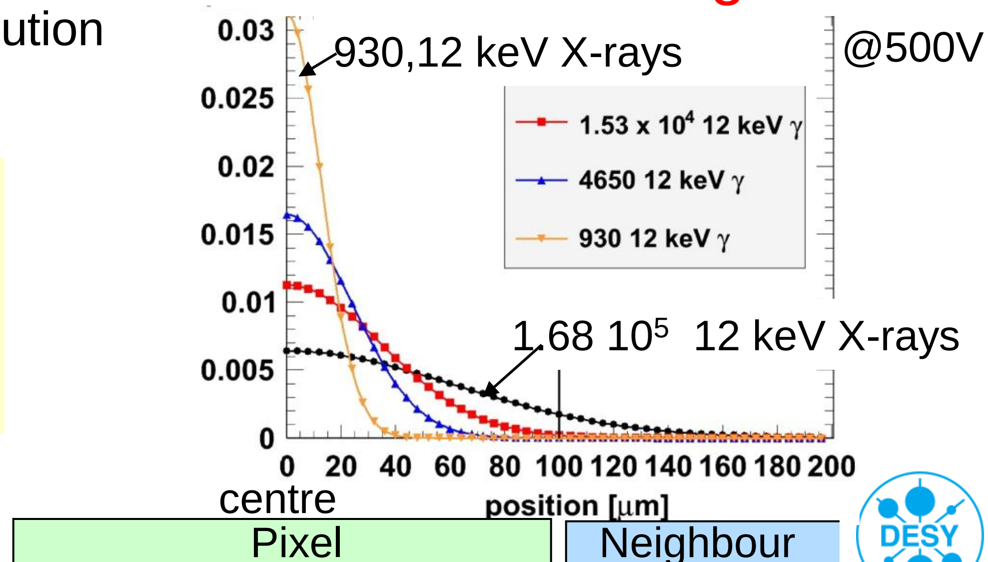
Lateral worsen spatial resolution

500V for 500µm thick Si-sensors
Sufficient to keep charge
in pixel and in time of bunch
(200µm-pixel, 220ns/bunch)

Pulse shape for 450µm Si

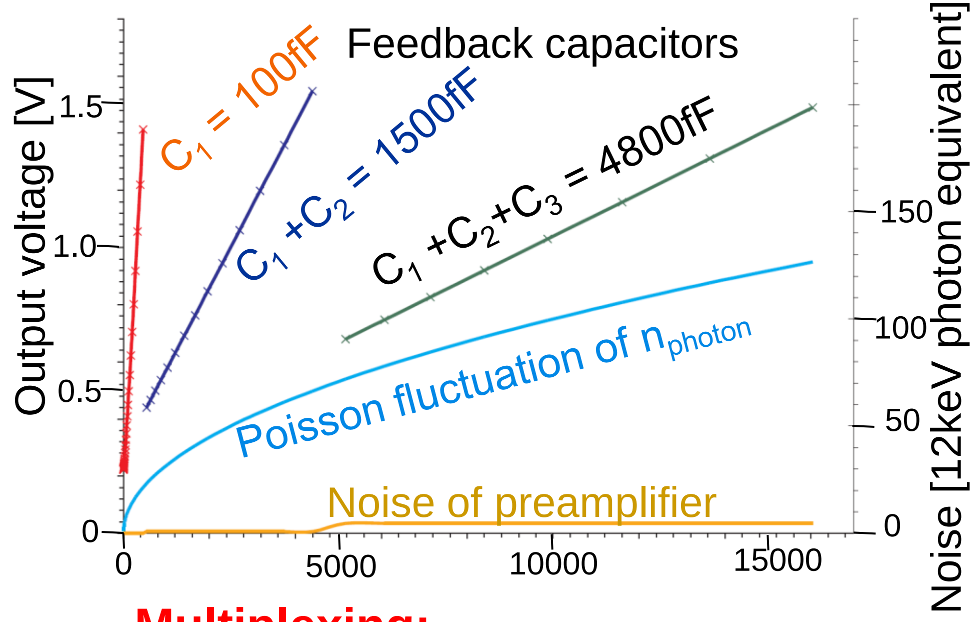


Lateral widening

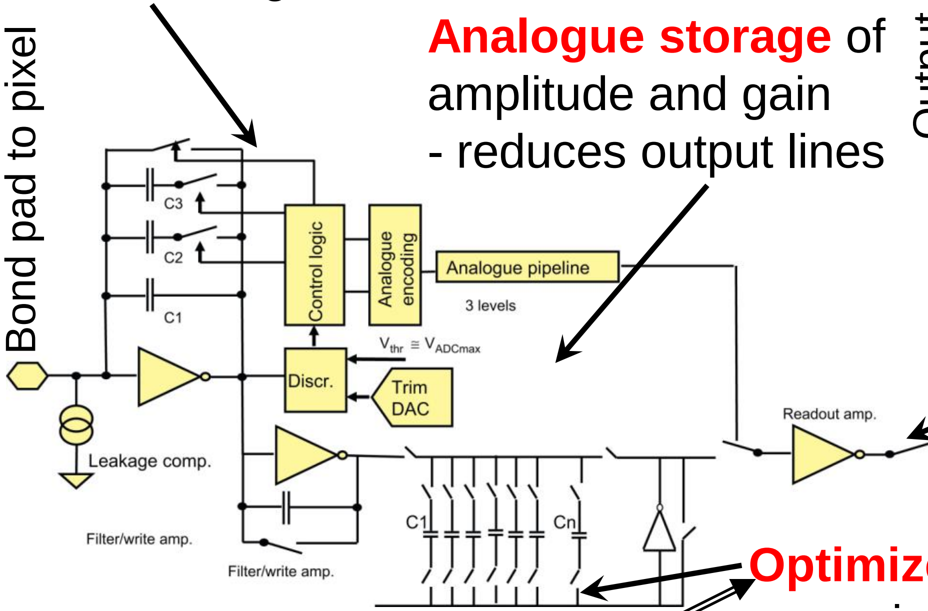


ASIC

Automatic gain switching:
- Gain switches, when output exceeds threshold
- Adding instead of replacing capacitors avoids charge losses



Analogue storage of amplitude and gain
- reduces output lines



Multiplexing:
Just one differential output
For 32 x 32 pixels

Optimized capacitors to store
maximum number of picture of a train
not all 2700 will be possible
realistic: ~ 200

Random address overwriting allows handling of an external decision of best scatterings

Constraint

Everything has to fit behind the pixel 200µm x 200µm

Board level electronics

Modular structure of AGIPD: 16 modules for 1Mega Pixel

1 Module: Sensor: 512x128 pixel, 10.3 x 2.8 cm^2
16 bump bonded ASIC's, each for 64 x 64 pixel, each 4 outputs

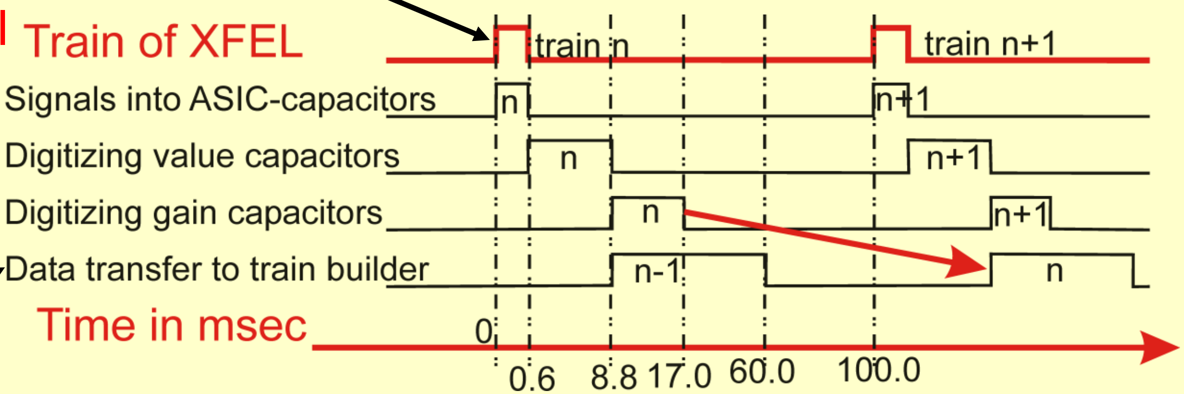
PCB's for each module:

- Digitizing 64 parallel signals: 14 bit 50MS/s
- Sorting data and transferring to DAQ : 10GbE
- Controlling the ASIC's
- **Synchronizing activies** to train structure of accelerator

1. X-ray info into capacitor/ASIC

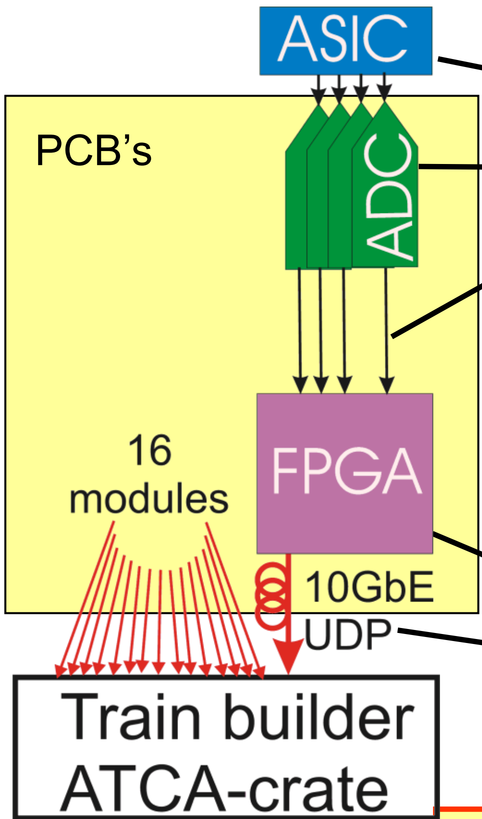
2. Digitize most critical within 8.8ms

3. Gain-bits (3 states) on same lines/ADC's saves connections and space



4. Digital activity delayed by one train
- Allow access to full data for sorting, selecting
- May be no activity while digitizing the critical values (2.)

Signal rates



Devices or links in		Rates per		
module	Detector head	link	module	Detector head
16	256			
64	1024	0.05	3.2	**51.2 GS/s**
64	1024	0.7	45	**720 Gbit/s** While digitizing (10% duty cycle) Data written to RAM by
1	16			
1	16	5	5	**80 Gbit/s** Continuously

Very high internal data rates require plenty parallel lines

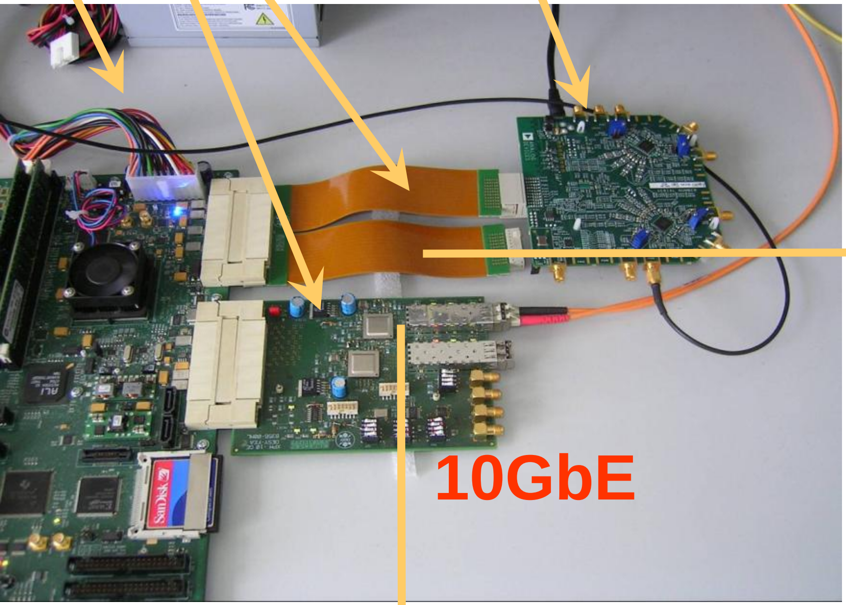
Still high continuous data flow to crates:

requires modern data transfers: 10Gbit/s on fibres

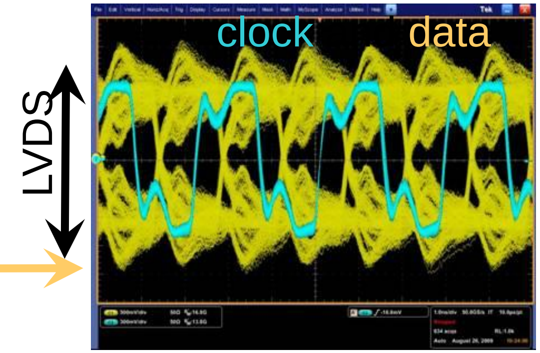
and high performace crate electronics: xTCA

Evaluation of high speed data transfers

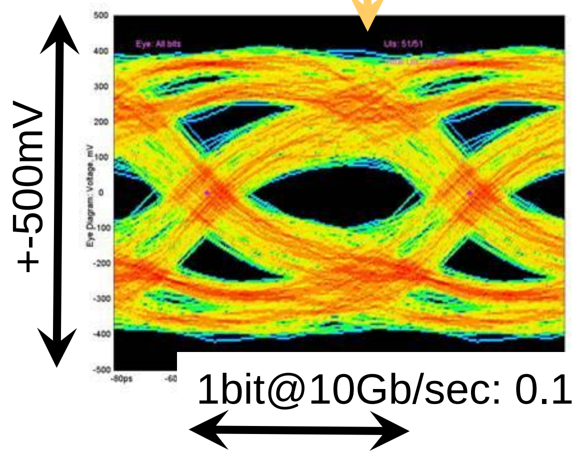
XILINX evaluation board + custom VHDL-UDP-core
+custom designs+ ADC-evaluation board



ADC: 700Mbit/s



Performance limited by no-impedance on XILINX-evaluation board
Eye diagram is well open



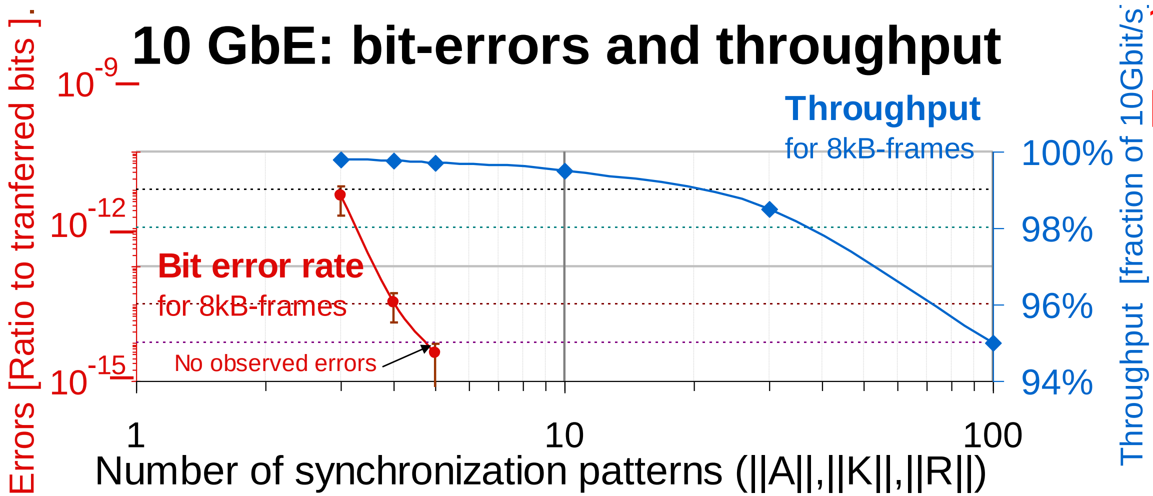
10 Gbit-Ethernet

… Measurement is limited by 16GHz-scope
Performance is better
Eye diagram is well open

Links are OK.

- Need no ideal setup
- Freedom to optimize system setup mechanics, modularity,…

Performance of technical evaluation tests



~ 55% -throughput needed

Error rate:

Measurement limit: $<5 \cdot 10^{-15}$

Converts to train losses

1 train out of 20 000 is OK

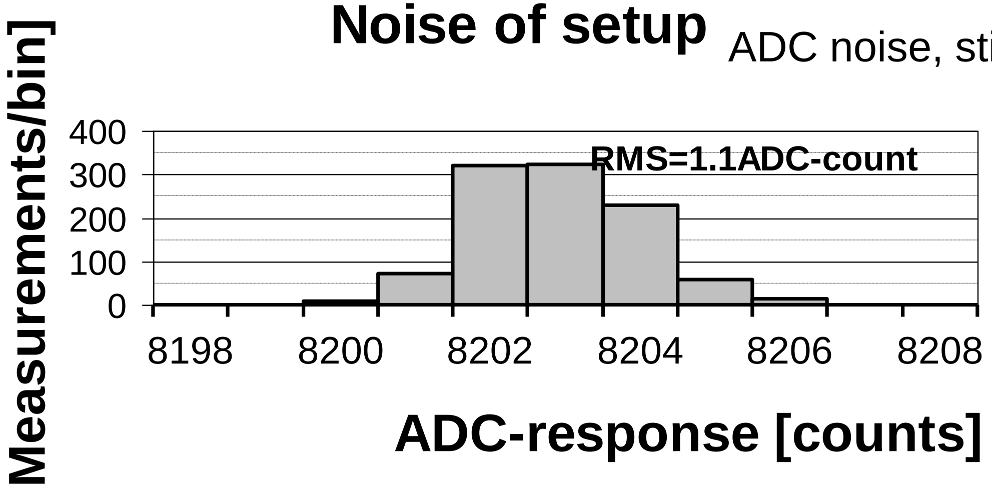
Also for using UDP,

no time to repeat,

next train as good as lost

Noise of setup

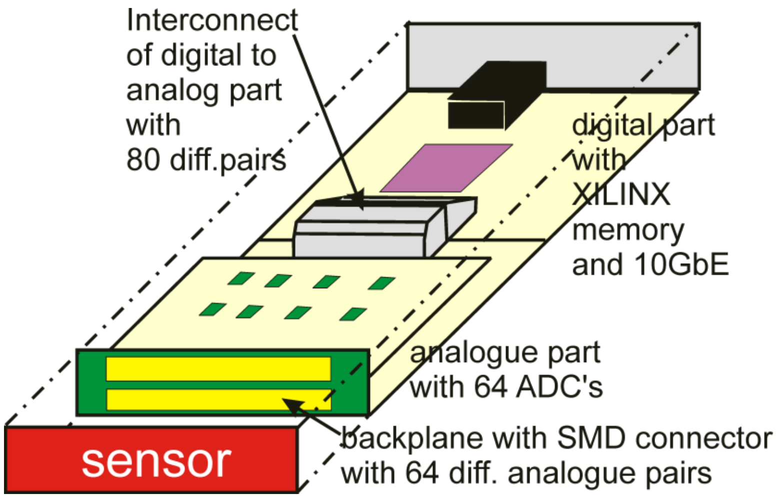
ADC noise, still like chip-data sheet



Evaluation test successful

Now, converting to the complex circuit and layout of full module

Modular electronics of a module



Using a backplane between sensors and Interface electronics as vacuum barrier and guiding common signals to the side

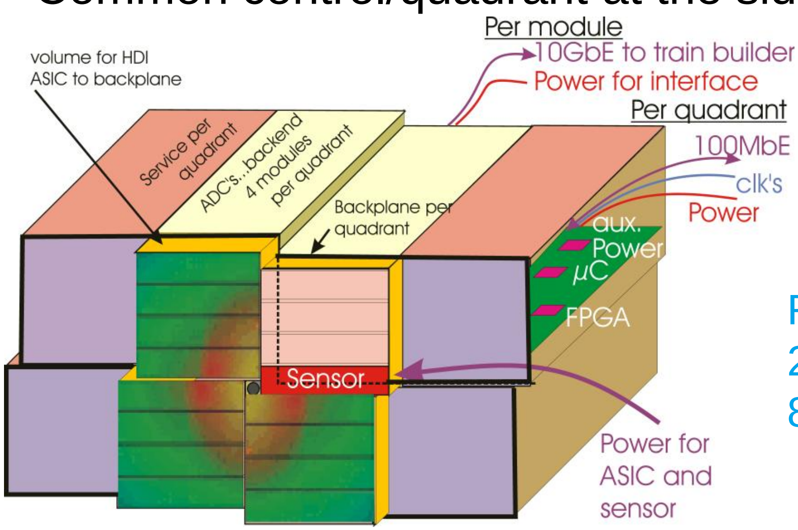
Separated digital and analog part
- Performance has shown, that connector is no problem at 700Mbit/s

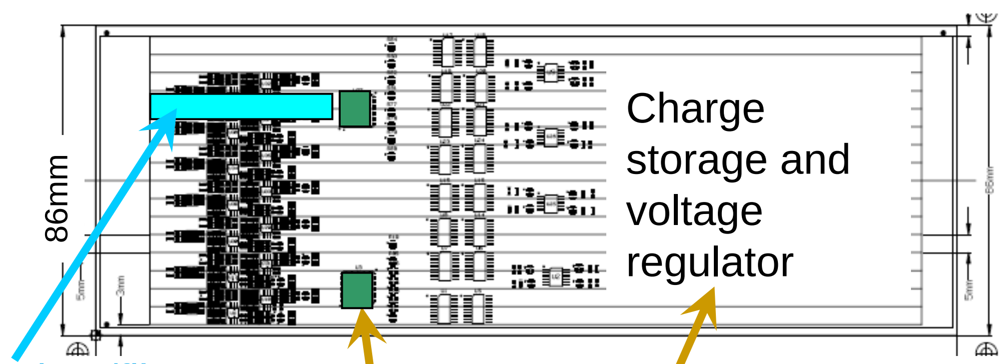
Therefore possible
- Disentangled developments, versions

Compact analog part by two parallel PCB's,
- dense layout of 16 filters/ADC's each side

Everything behind sensor
- stackable to 1MegaPixel and more

Common control/quadrant at the side





DSSC: DEPMOS Sensor with Signal Compression

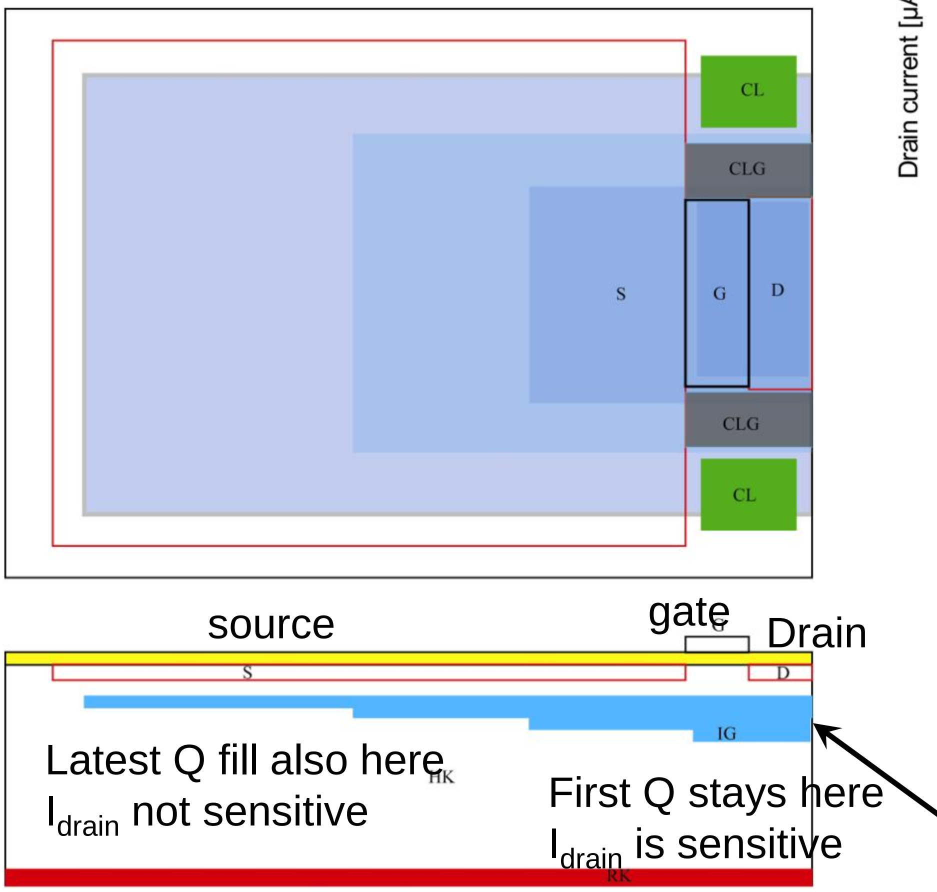
G. Lutz, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.03.002

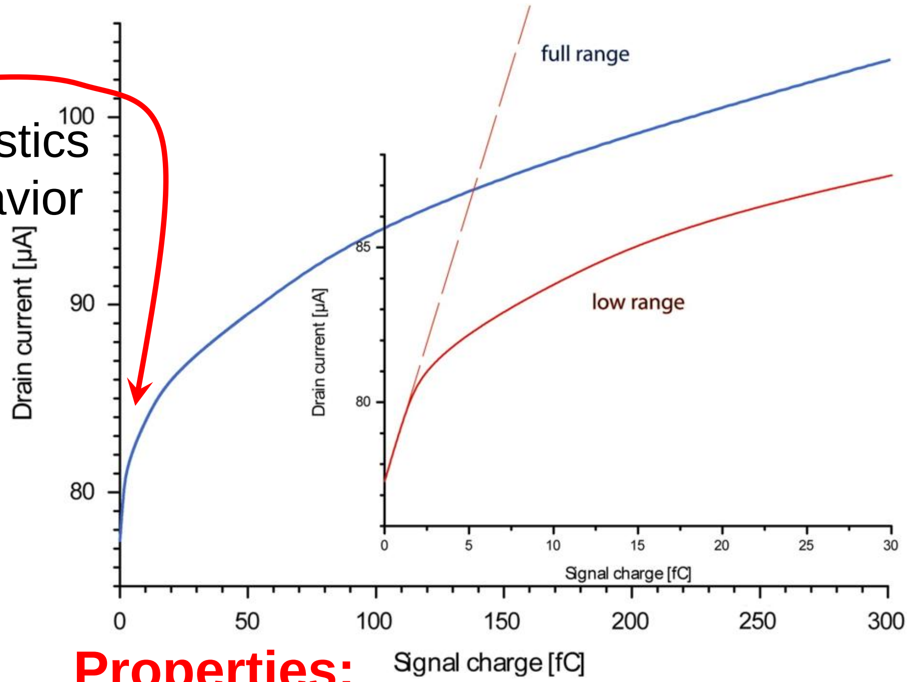
Mechanism for dynamics:

single photon distinguished: 0,1,2,3,….

high pulses: resolution better Poisson-statistics

Inside pixel a DEPFET with none-linear behavior





Properties:

- ADC/pixel : 8 bits within 220ns for dynamics up to 10 000 X-rays
- Storage depth: 512 or more in DRAM of ASIC
  all has to fit in area of one pixel
- Low noise due to DEPFET

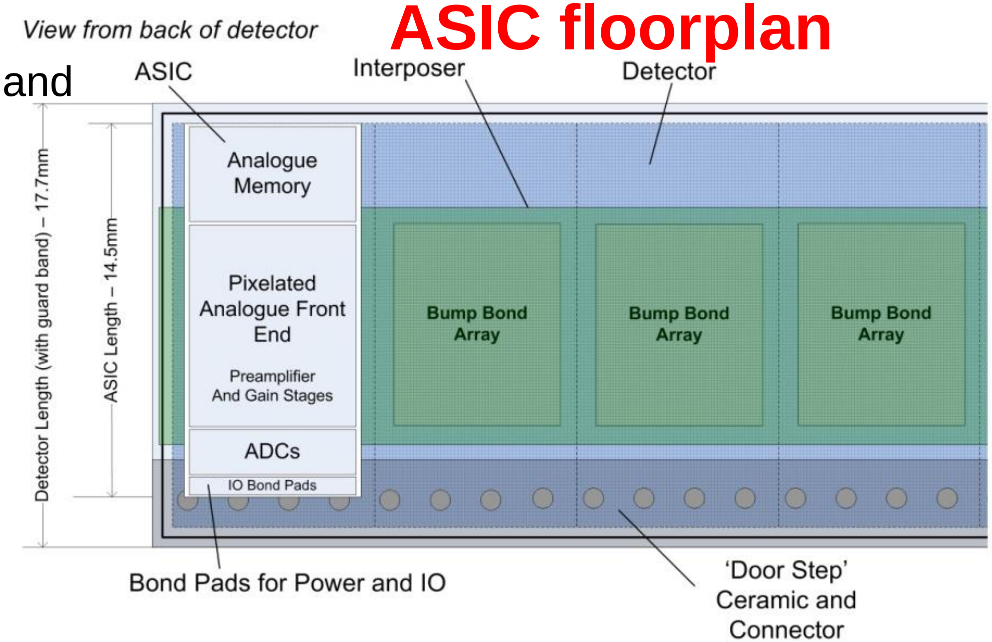
LPD: Large Pixel Detector

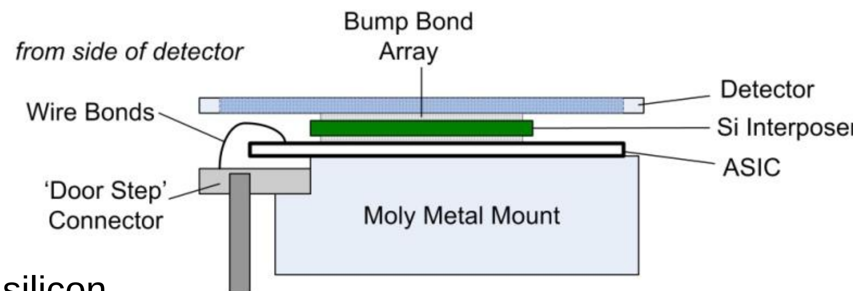
S.R.Burge et al., Large Pixel Detector for the European X-ray Free Electron Laser,
11th European Symposium on Semiconductor Detectors, June 2009 conference proceedings

LPD ASIC

- **512 Channels** per ASIC including preamp and gain stages connected to 500µm pixels
- High dynamic range,
  1 to 1x10^5 photons/pixel/pulse
- Full range is recorded by
  3 parallel gain stages - 1x, 10x and 100x
- Chip control is driven by a
  command word interface.
  e.g. 'Trigger' a frame capture.
- **512 frame memory depth - analog**
  continuously stores all three gains, saving whenever a trigger is received.
- Readout is split between **sixteen 12-bit ADCs**
- Output **data rate 94Mbps** per ASIC
- Designed in **IBM 130nm** technology.

ASIC floorplan





interconnect structure of a detector module

sensor covers full area !

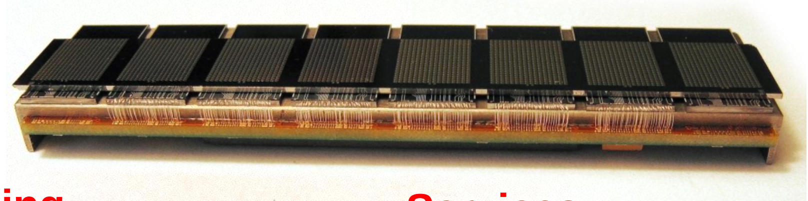
Benefits of the Design

- Large pixel size **reduces radiation dose**/unit area of silicon.
- Large memory depth allows storing **more frames/train**
- Cyclic memory write process gives the ability to **deal with lag in the trigger signal** up to the full memory depth.
- Command word interface allows **expanded modes of operation**, e.g. alternate reset timing

LPD: Large Pixel Detector
System components

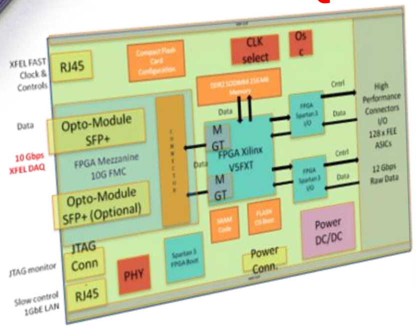
The full system is complex,
many design challenges have been taken on and realised by groups in the Technology department at Rutherford Appleton Labs.

ASIC Module

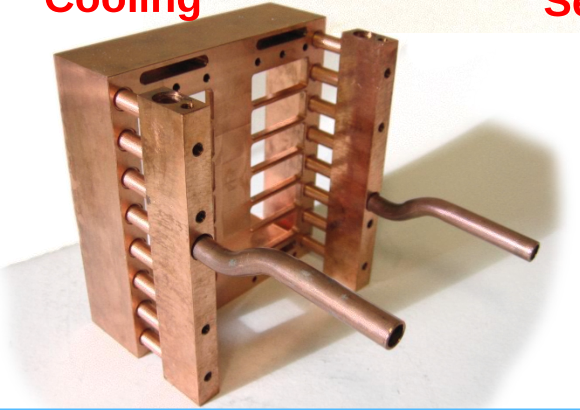


Detectors

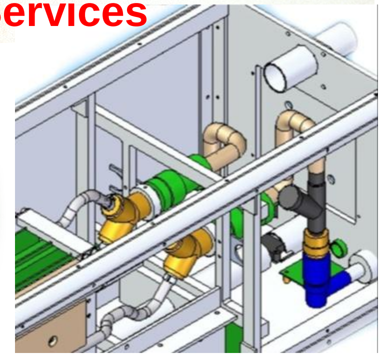
FPGA - DAQ



Cooling

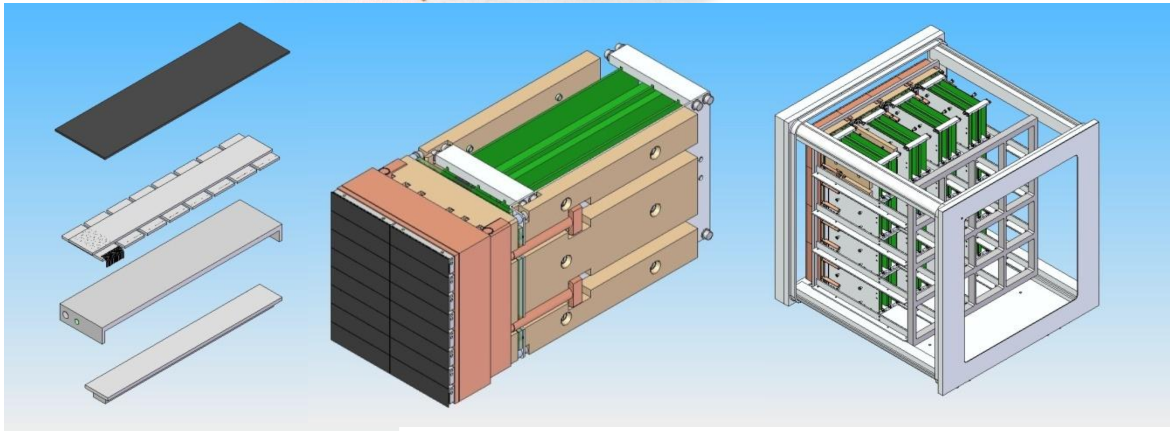


Services



LPD Full System

- Designed to be scalable.
- 8 ASICs are bump bonded to the back of a Silicon Detector module with 4,096 pixels
- 65+ Thousand pixels per super-module (8x2modules) Includes Cooling Unit, FPGA and Power Cards
- 1+ Million pixels (4x4 Super-modules) per detector.



8 Chips	128 Chips	2048 Chips,
4,096 Pixels	65,536 Pixels	1,048,576 Pixels
Scale = 6.4cm	Scale = 12.8cm	Scale = 51.2cm

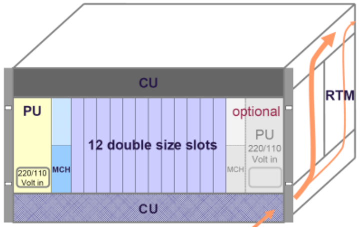
Outline

> Motivation for new X-ray sources and detectors

> X-ray Free Electron Laser: Sources of the new 4th generation
European XFEL

> Detectors
2 dimensional cameras,
one is AGIPD: Adaptive Gain Integrated Pixel Detector

> Control and Data Acquisition for detectors

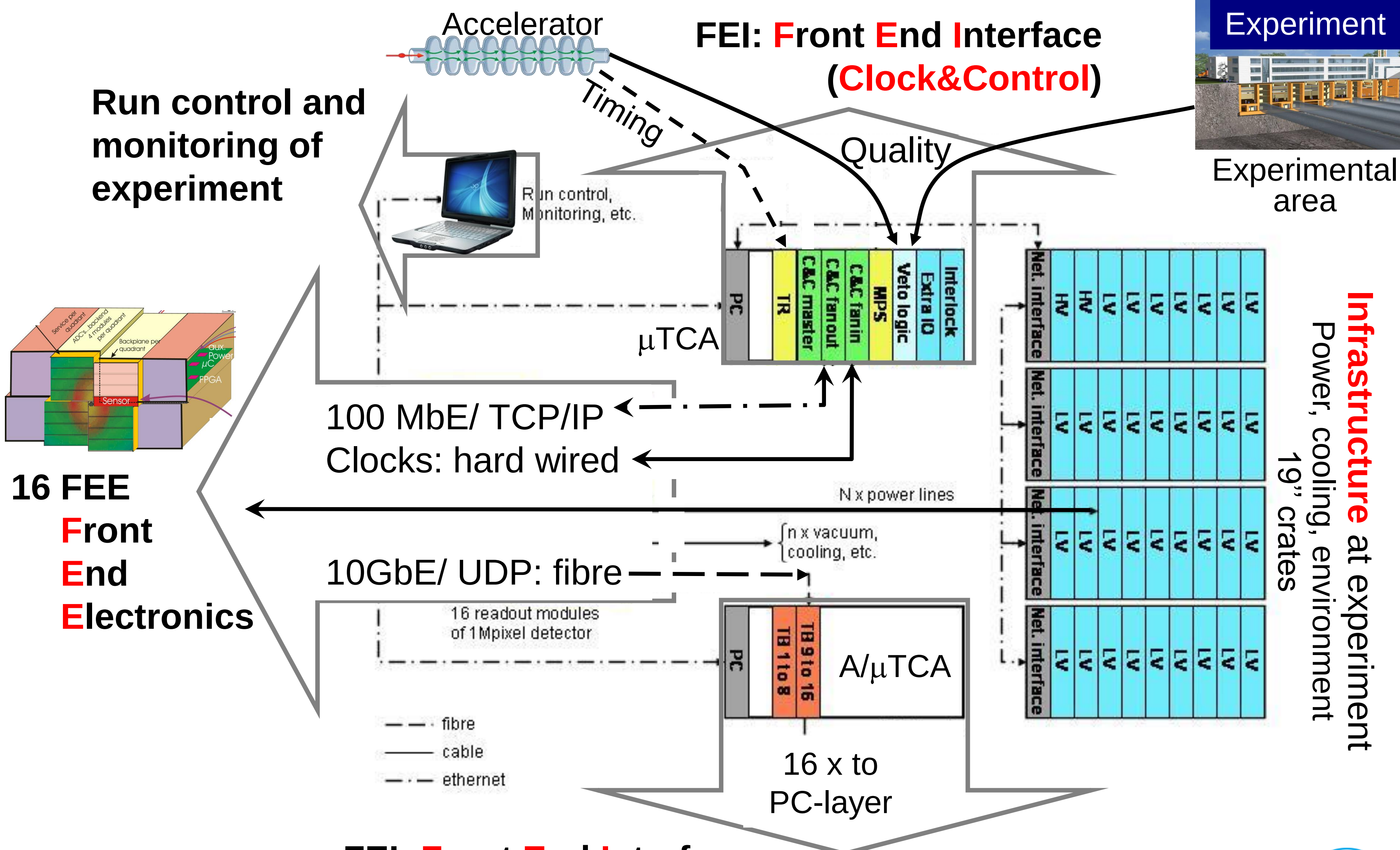


> Status of the project

> Outlook

Targeted DAQ for cameras

XFEL-work package 76: C.Youngman http://www.xfel.eu/project/organization/work_packages/wp_76/

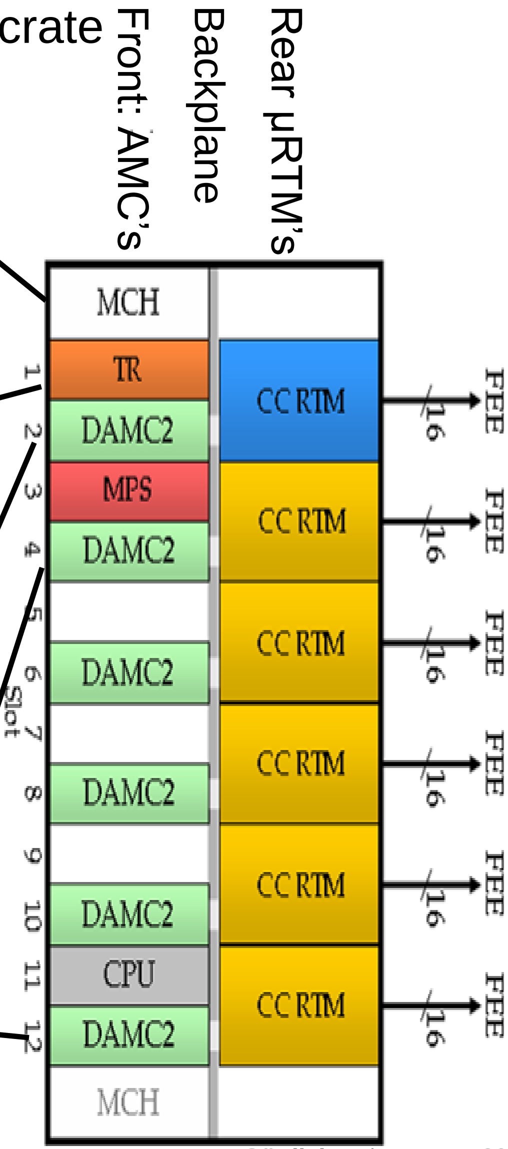


FEI: Front End Interface
(Train builder) for readout

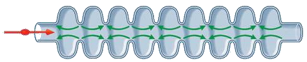
Clock&Control Hardware Structure

µTCA for physics

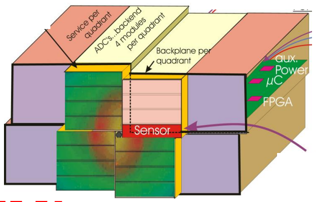
12 slot crate



- > µTCA **C**arrier **H**UB
  - Management of µTCA
  - Clock distribution for synchronization to accelerator
  - Configuring high speed network, PCIe
- > **T**iming **R**eceiver board
  - Receives from accelerator the timing and train information



  - Generates onto bussed lines
    - Continues clock 99MHz
    - Bunch clock 4.5MHz
    - Telegrams
- > DAMC2 digital card host:
  - CC master board
  - Additional CC slave boards
  - Command to FEE: 22bit/bunch



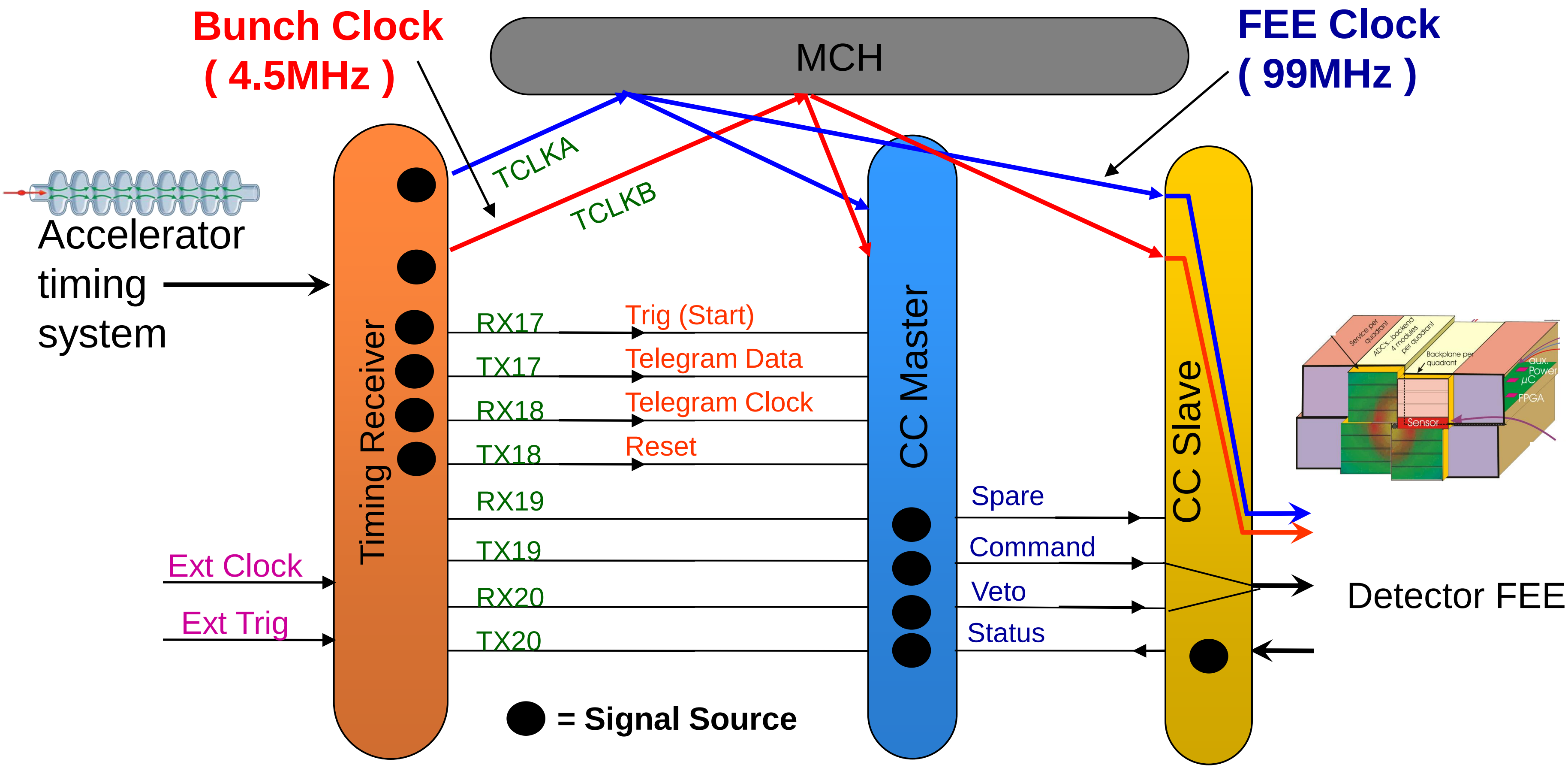
µRTM's:

- drivers
- receivers
- connectors to camera and sensors
- scalable to more than one Mega-pixel

CC: Hardware Structure

Signal distribution by backplane and MCH

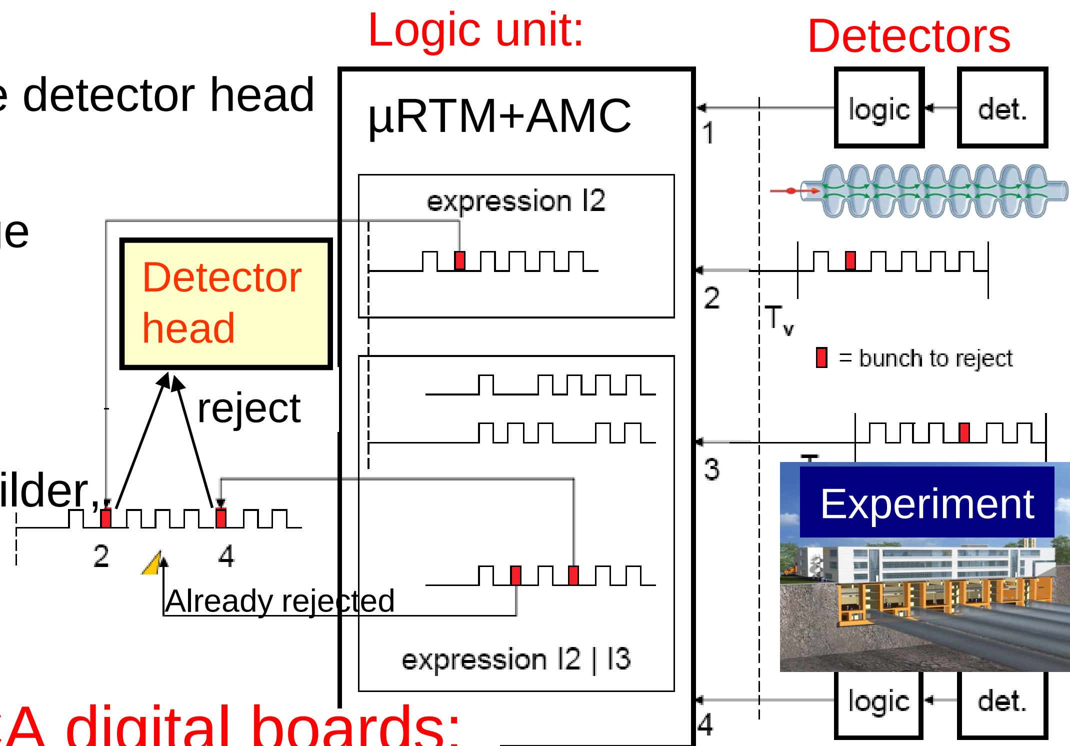
Following xTCA, PICMG®, MTCA.4



The veto system

> Purpose:
- Delete low quality images at the detector head

> Aim:
- Optimize storage pipe line usage
  200-512 cells/2700 bunches
  Most important for AGIPD
- Keep pictures with best quality
- Reduce data volume to train builder,
- i.e. similar to HEP FLTriggers



> Implementation using µTCA digital boards:
- Sources - send conditioned signals
  - differ in delays 0µs to 7µs due to positions along XFEL
- Cameras - request a fast response ⇒ send “reject” at first valid veto.
- Logic unit - evaluates equations
  - generates rejected bunch number: one/bunch or idle as 22bits
- For AGIPD - Clock and Control system distributes the number
  - Detector head does the memory management

Veto in detector head

ASIC:

Essential is an ASIC with **random access storage**

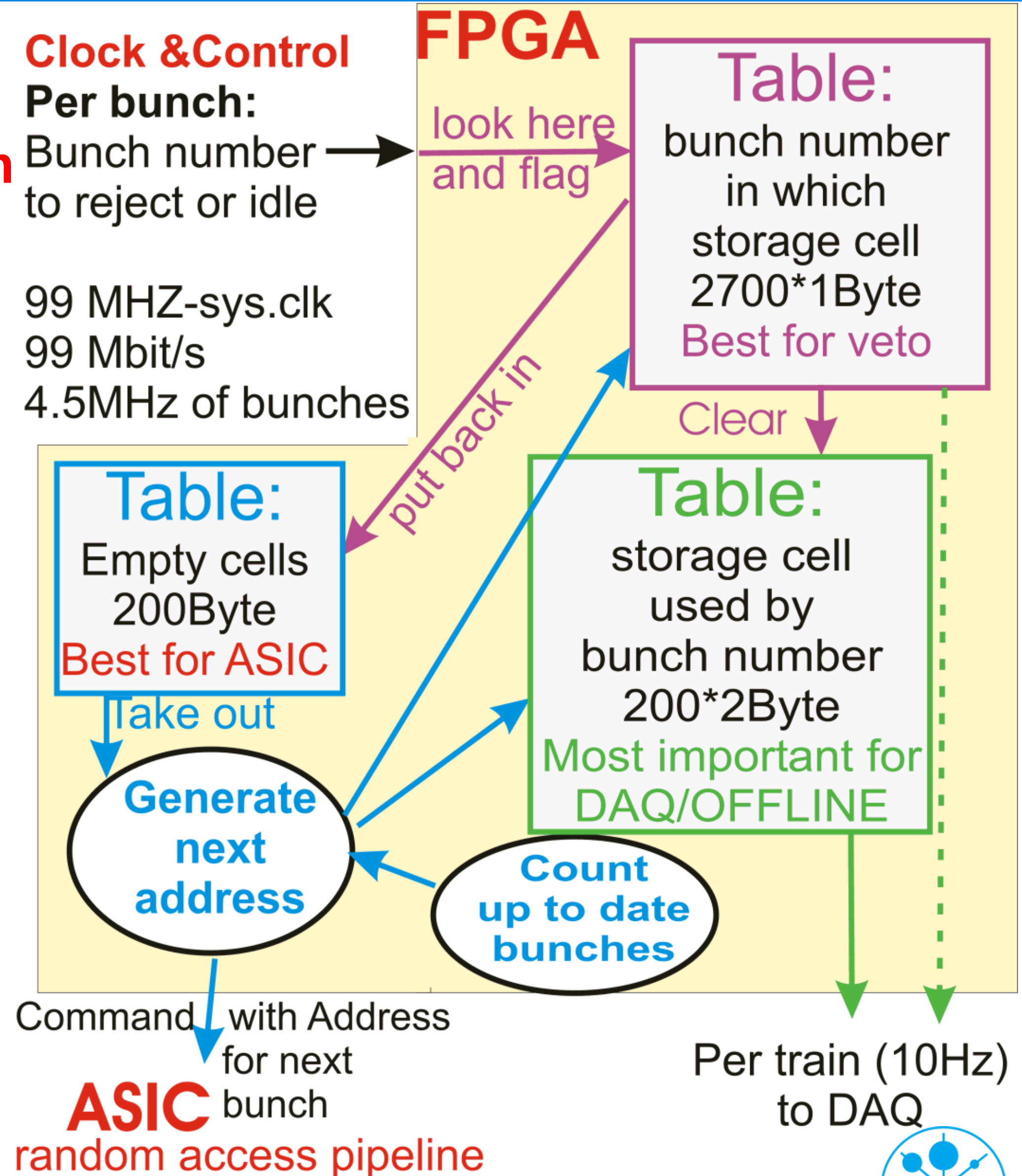
Logic support (FPGA)

With two parallel actions (220ns):

- generating address for ASIC for next bunch/storage
- clearing rejected

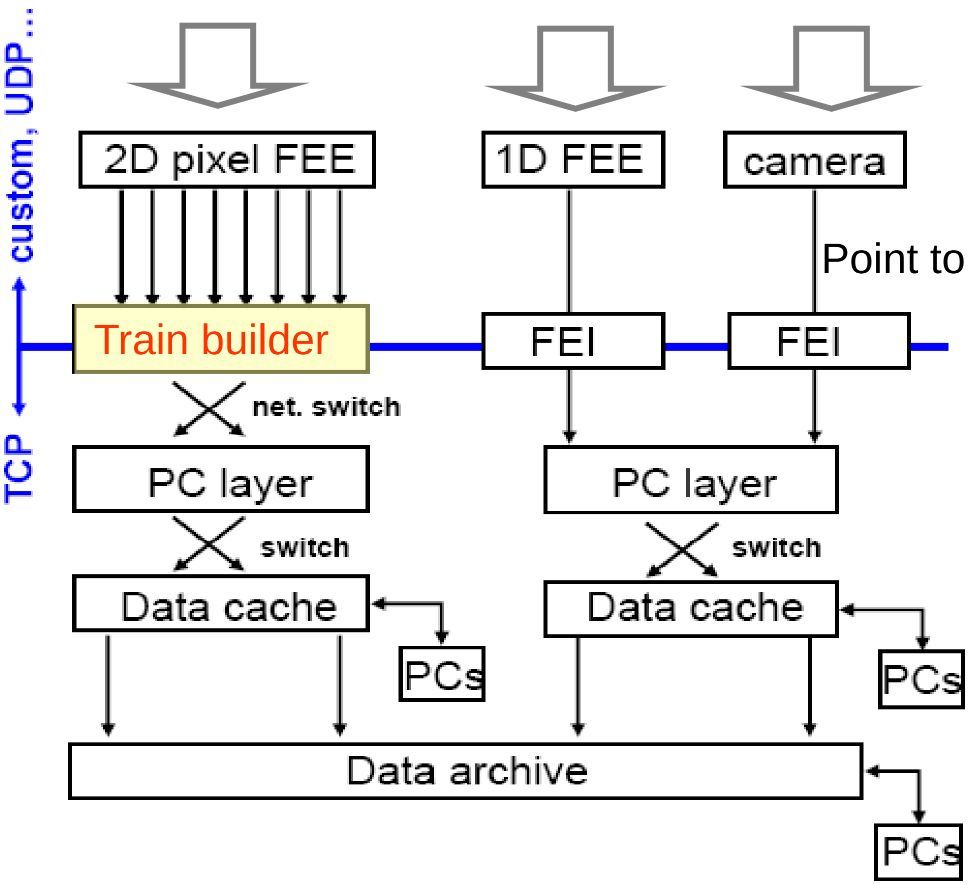
Supported by a consequent update of tables for three different tasks:

- Reject
- write actual bunch
- DAQ/OFFLINE (online kept or generated while data transfer)



Multi layer readout architecture used

Frame: 2MB 2kB 2MB
Train: 1GB 5MB 2MB
@PC 10GB/s 50MB/s 20MB/s : Typical throughputs



5 Layers

- Front End Electronics FEE
- Front End Interface FEI or TB
- PC layer
- Data cache
- Data archive

Train builder:

Full train to ONE PC

FPGA
cross point switch

scheduled switching
point to point

Layer functionality

- FEE = Front End Electronics
  - Detector side interface to control & readout
- FEI = Front End Interface
  - DAQ side interface to control & readout
  - Protocol conversion: custom to TCP
  - Frame and Train building
  - Data processing
- PC layer
  - On-the-fly data processing and monitoring
  - File formatting and aggregation
- Data cache
  - 2 day deferred commit to data archive
  - Processing, monitoring and quality control
- Data archive
  - Offline data processing

Processing implies reduction

= compression | rejection

Design generic DAQ and DM systems assuming 10PB/year data volume with the possibility to scale it in the range of 5 to 100PB/year for all beam lines

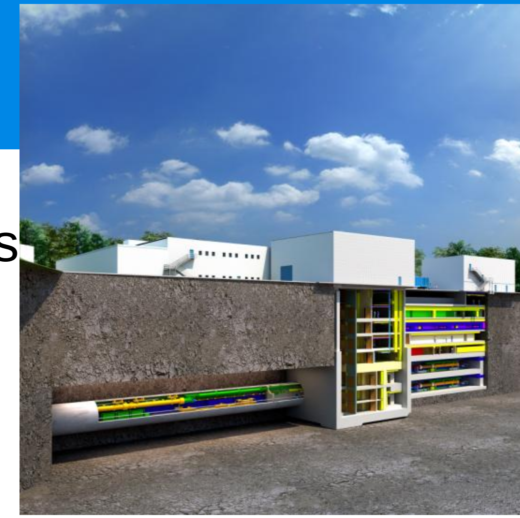
Outline

- Motivation for new **X**-ray sources and detectors
- **X**-ray **F**ree **E**lectron **L**aser: Sources of the new 4th generation
  - European XFEL
- Detectors
  - 2 dimensional cameras,
  - one is AGIPD: **A**daptive **G**ain **I**ntegrated **P**ixel **D**etector
- Control and Data Acquisition for detectors
- Status of the project
- Outlook

Start of the project

- January 2009: Start of civil engineering on three sides

Hall and shafts are there,
Civil engineering continues

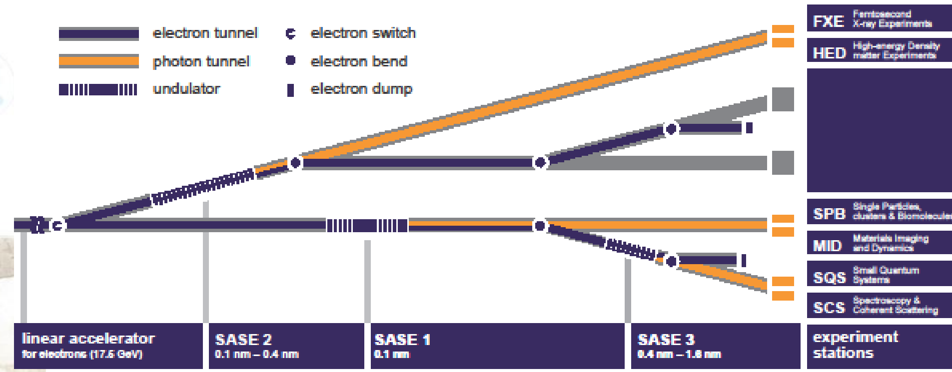


- November 2009: European-XFEL founded as GmbH (German limited)
  8 countries joint the Eu-XFEL-GmbH, more coming

European XFEL

Status of the project

> September 3rd 2010: First photon tunnel drilling finished



Many more to be done,

by two drilling machines

2012	Buildings getting ready for installation
2013	First beam in injector
2014	First beam in linear accelerator
2015	First SASE, first experiment
2016	‘Full’ User operation

Outlook

- European XFEL will deliver the highest peak brilliance and bunch rate.
- Need of excellent accelerator performance: Size and energy of bunch.
- Dedicated regulations in modern technologies needed.
  Developments and tests at FLASH are on going with good results.
- That leads to the use of modern standards in science: ATCA, μTCA.
  Adapting them to the needs (PICMG®) and first modules are available.
- Demanding dedicated detectors (Pixel cameras) are being developed.
  Ongoing developments for full chain with high signal and data throughput:
  - Sensors, ASIC's, detector heads and DAQ systems
  - e.g. 4.5MHz picture rate, 80 Gbit/s out of small detector heads
- All the effort opens new fields of science:
  Capturing a scattering picture with one flash of X-rays.

- Thanks to all the work packages and consortia for providing material
- More information on www.xfel.eu
  http://hasylab.desy.de/instrumentation/detectors/index_eng.html