The Versatile Transceiver

Feasibility Demonstration

(Project phase II update)

Versatile Link

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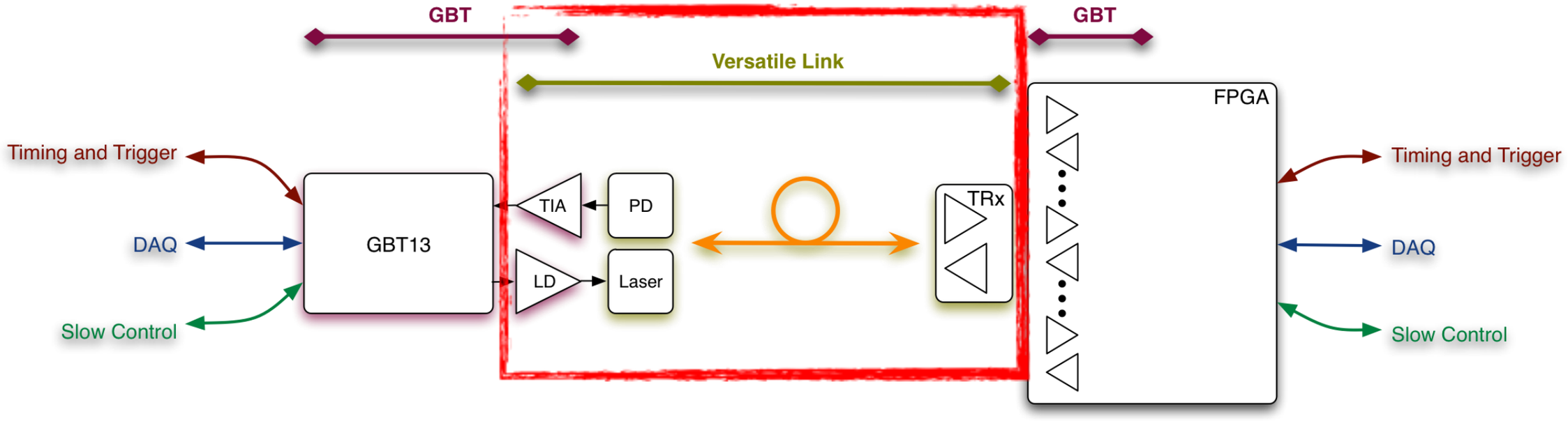
CERN

Overview

- Versatile Link Project re-cap
- Versatile Transceiver Packaging
- Front-end Component Functional Testing
- Radiation Testing
- Summary

Versatile Link Project

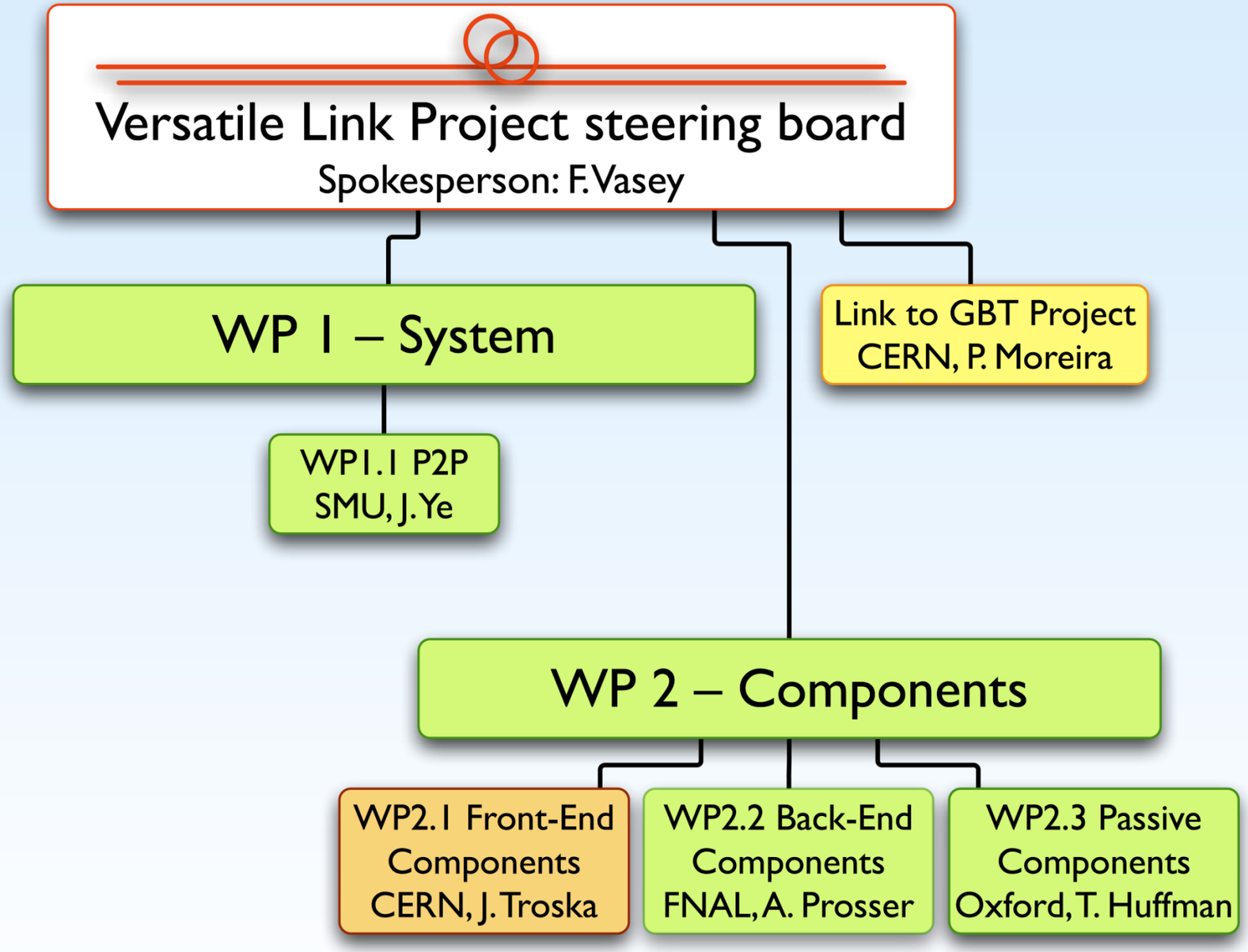
- Optical Physical layer linking front- to back-end
- Bidirectional, ~5Gbps
- Versatile
  - Multimode (850nm) and Singlemode (1310nm) versions
  - Point to Point and Point to Multipoint architectures
  - Front-end pluggable module
- Joint Project Proposal submitted to ATLAS & CMS upgrade steering groups in 2007 and endorsed in 2008
- Kick-off mtg in April 2008
  - Phase I: Proof of Concept *(18mo)*
  - **Phase II: Feasibility Study *(18mo)***
  - Phase III: Pre-prodn. readiness *(18mo)*



On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

Project Structure and Partners

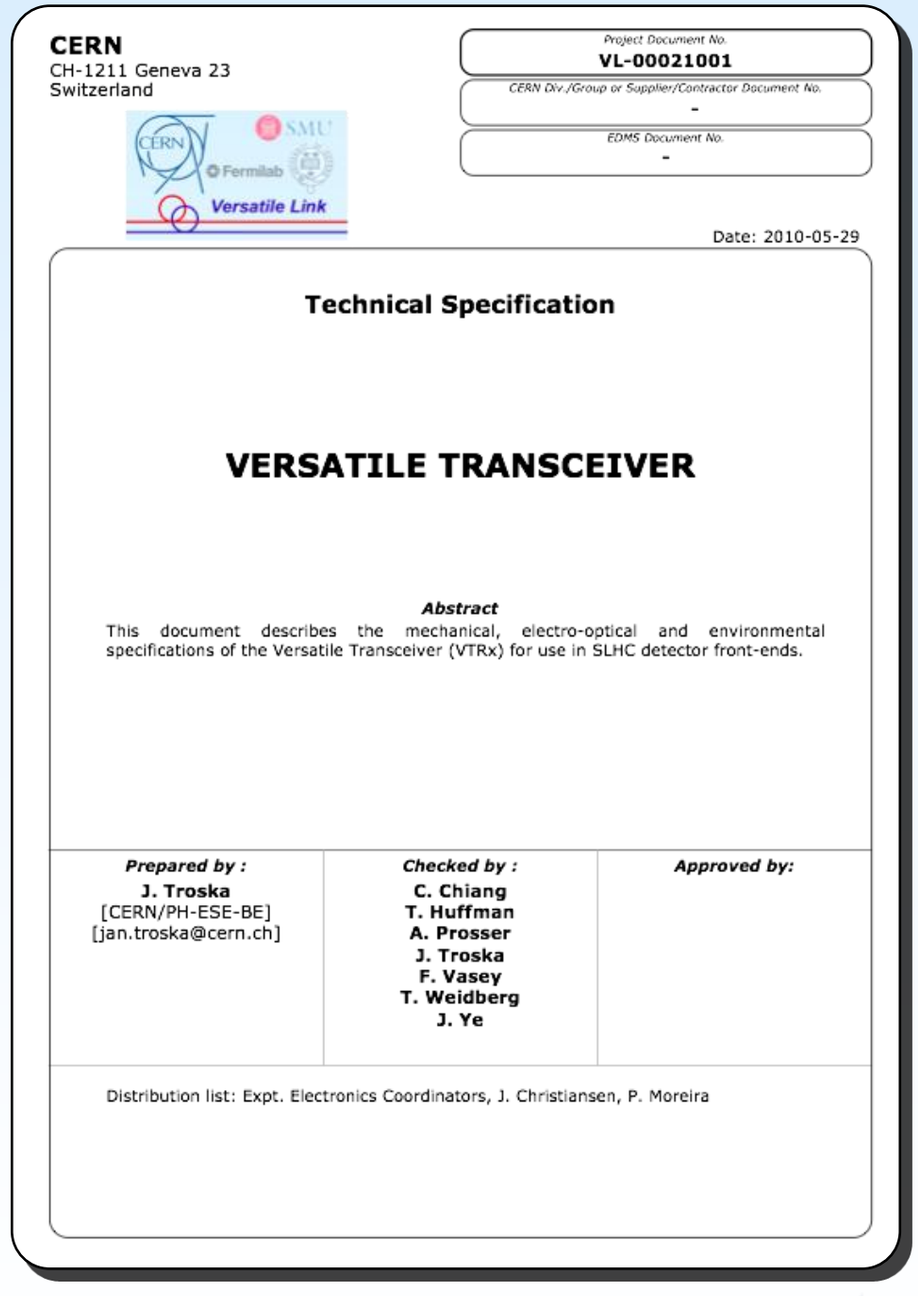


Dr. A. Xiang, "Link Model Simulation and Power Penalty Specification of Versatile Link Systems" – session B4
A. Prosser, "Parallel Optics Technology Assessment for the Versatile Link Project" – poster session
N. Ryder, "The Radiation Hardness of Specific Multi-mode and Single-mode Optical Fibres at -25 deg. C to full SLHC doses" – session B5b

WP2.1 Front-End Components

Versatile Link

- Deliverables for the end of Phase II (April 2011)
  - Detailed Versatile Transceiver (VTRx) specification
  - Detailed specifications for the sub-components used inside the VTRx (Laser diode, Photodiode, Laser Driver, Receiver Amplifier)
  - Shortlist of variants for VTRx flavours (wavelength, fibre type) and associated sub-components
  - Full radiation test results for the sub-components for all shortlisted variants of the VTRx. A range of irradiation sources will be used to give confidence that the VTRx will withstand the SLHC Tracking detector environment.
  - VTRx packaging design and fabrication containing validated optoelectronic sub-components and custom radiation-resistant electronics (Laser Driver and Receiver Amplifier). ASICs could for example be sourced from the GBT project



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Switzerland

Project Document No.
VL-00021001

CERN Div./Group or Supplier/Contractor Document No.
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EDMS Document No.
-

Date: 2010-05-29

Technical Specification

VERSATILE TRANSCEIVER

Abstract

This document describes the mechanical, electro-optical and environmental specifications of the Versatile Transceiver (VTRx) for use in SLHC detector front-ends.

Prepared by :	*Checked by :*	*Approved by:*
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Distribution list: Expt. Electronics Coordinators, J. Christiansen, P. Moreira

Spec almost ready for 1st distribution

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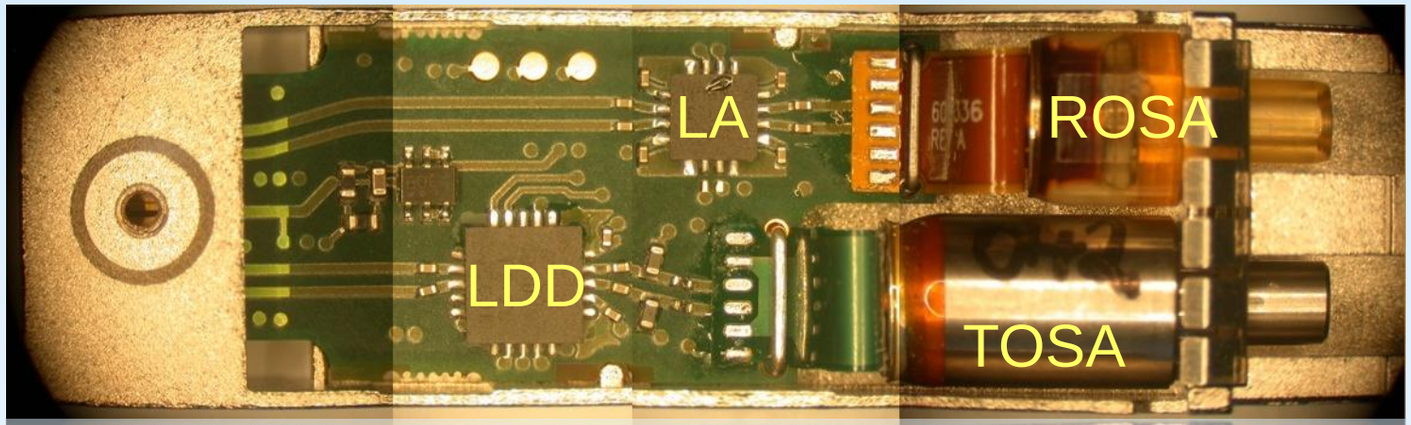
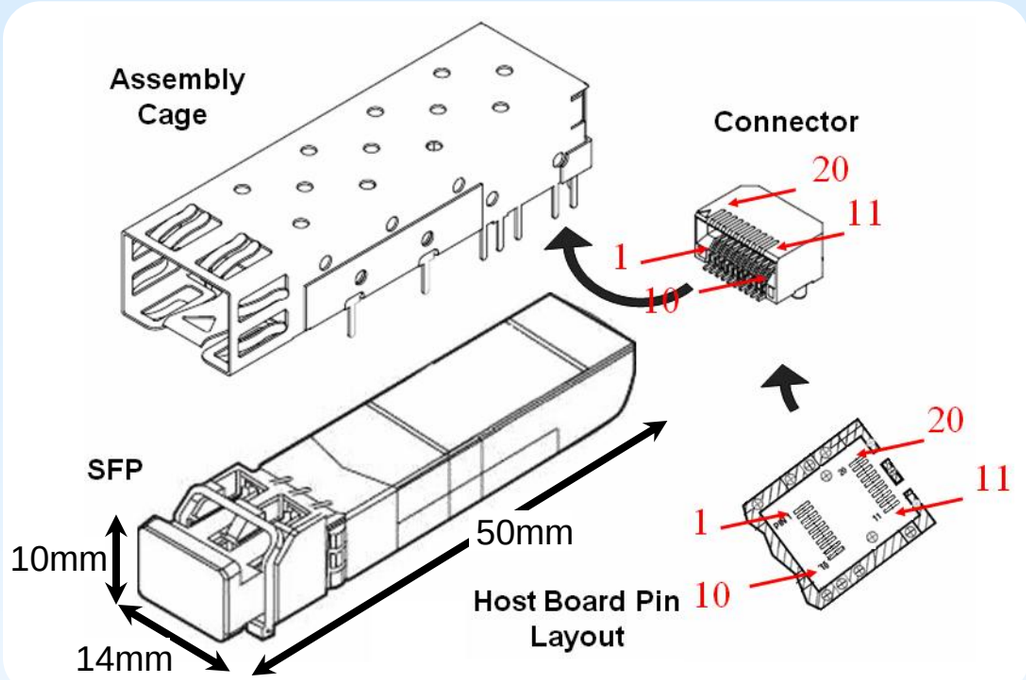
VTRx packaging overview





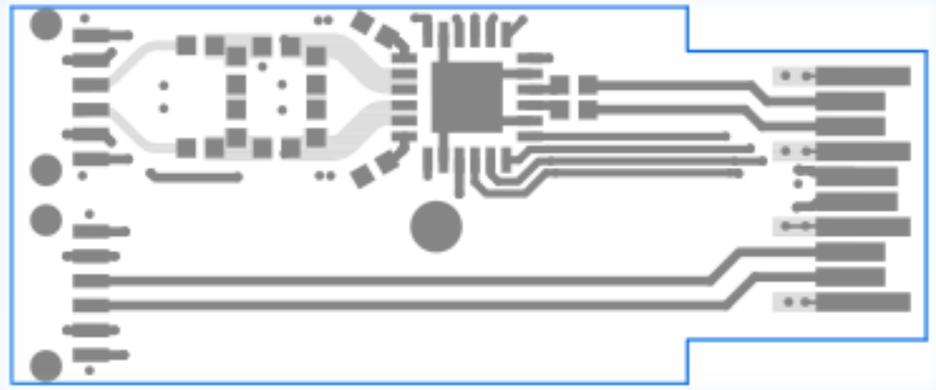
- Based upon commercial SFP+ standard for 10G transceivers
- ASICs
  - Laser Driver (LDD) - GBLD
  - TIA - GBTIA
  - LA - not foreseen (inc. in GBTIA)
  - No microcontroller
- TOSA - Rad Hard Laser
- ROSA - Rad Hard PIN + GBTIA
- Keep Std. SFP+ Host board connector
  - No cage, alternate fixing T.B.D.
- Remove/replace material from std. SFP+ housing
  - Must test EMI tolerance and emission

VTRx

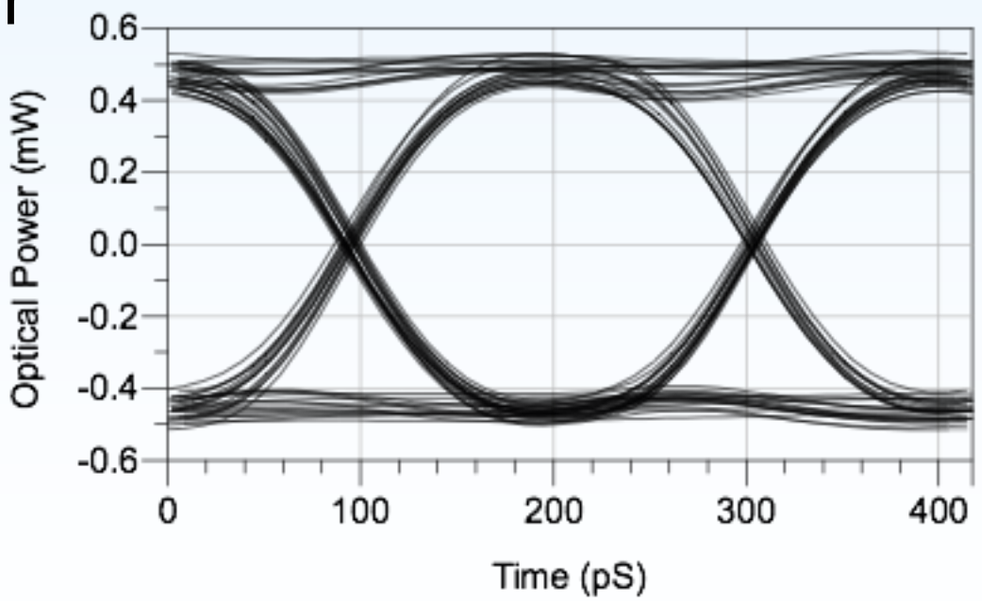
Components	**Pkg know-how**
GBLD	*Commercial Eval Boards*
GBTIA	*In-house Test boards*
Commercial LDD	*Industrial partnership*
Commercial TIA/LA	*VTRx prototype board*
ROSAs 850/1310nm	
TOSAs 850/1310nm	
Device modelling	

VTRx PCB design

- Based upon experience gained with commercial ASIC evaluation boards and our own versions of such boards, have built our own SFP+ size-compatible test PCB housing:
  - Commercial edge-emitting laser driver
  - Commercial TOSA
  - GBTIA-ROSA

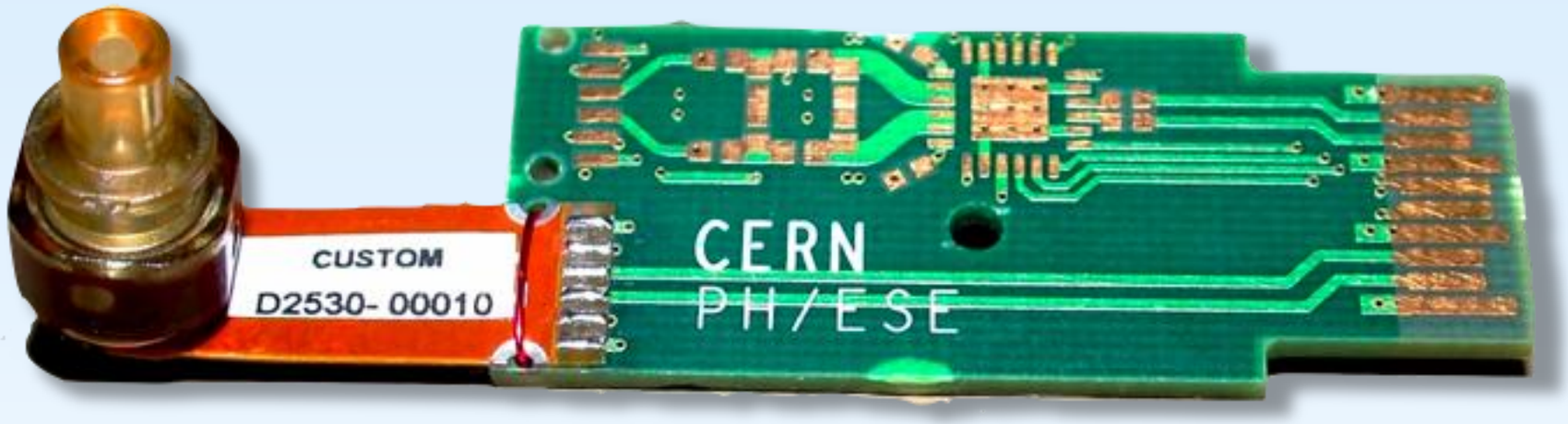


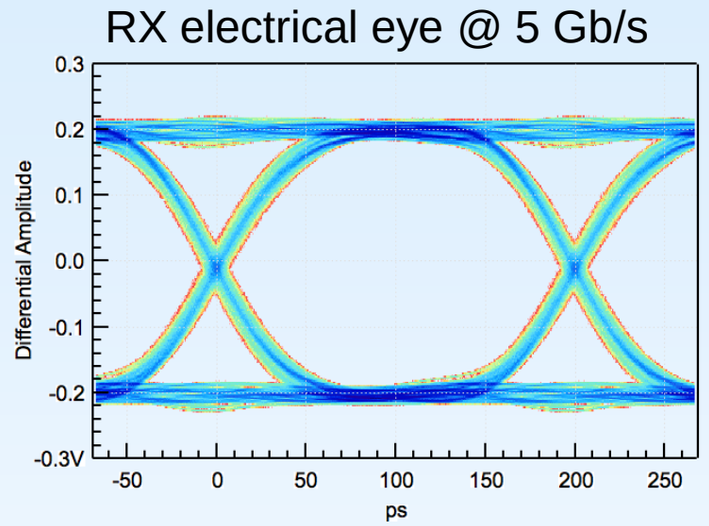
- PCB circuit simulations including the laser model were carried out to confirm the correct functionality of the board
  - Including optimization of the bias/matching network



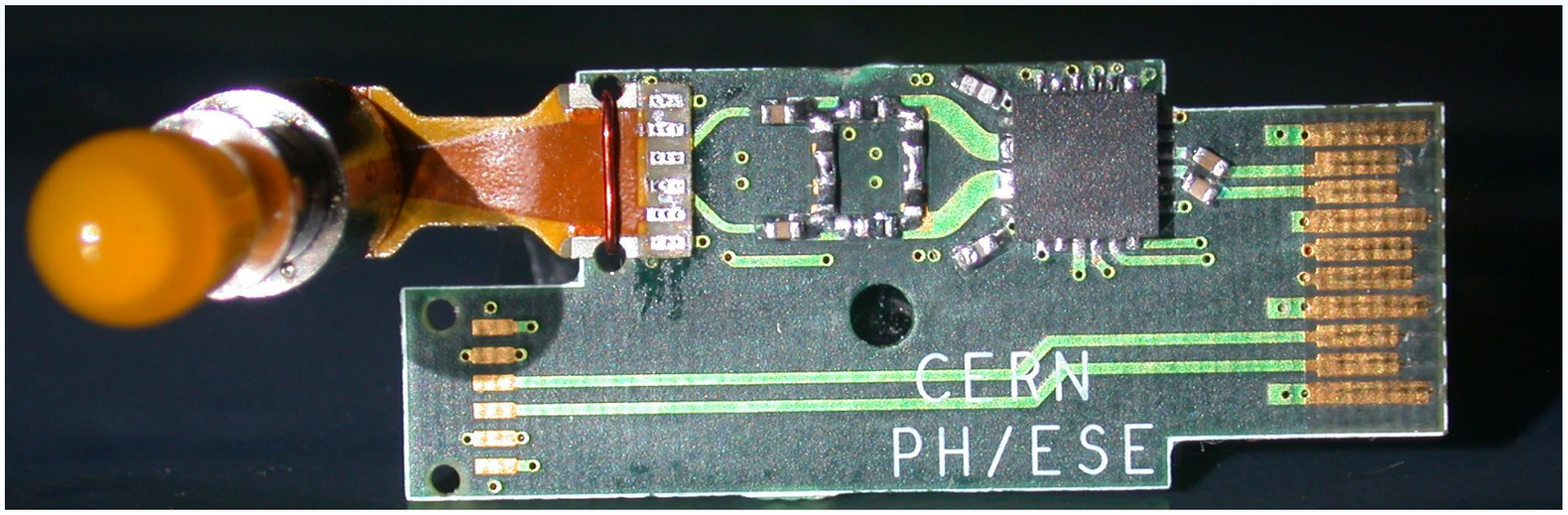
TOSA/ROSA integration on VTRx

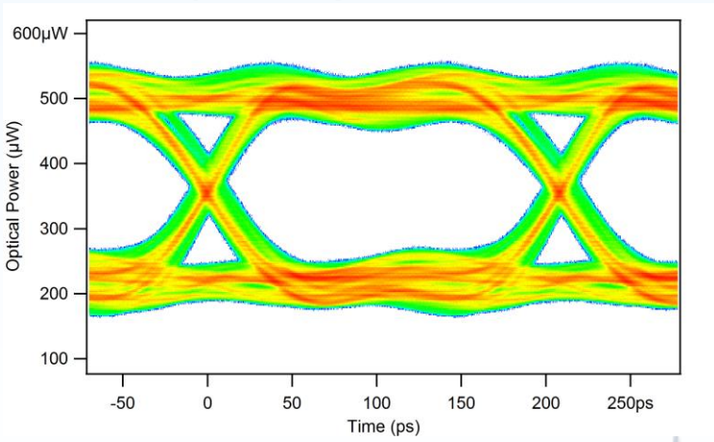
- GBTIA-ROSA on prototype VTRx PCB





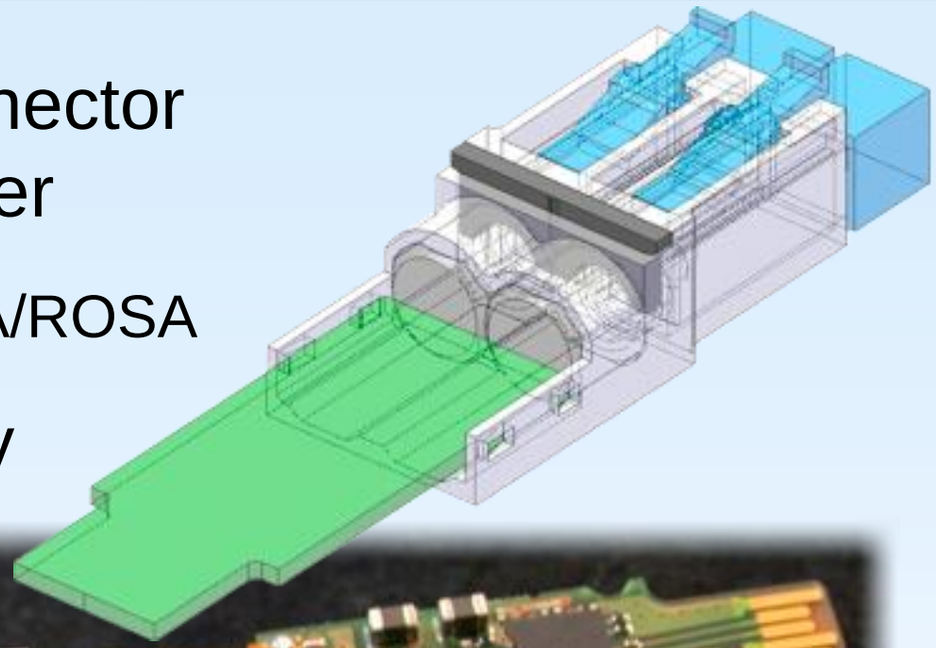
- TOSA and commercial Laser Driver on VTRx PCB

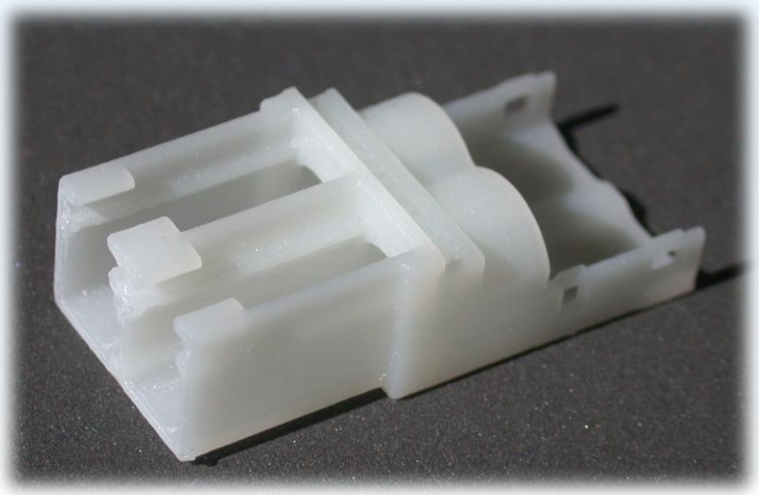


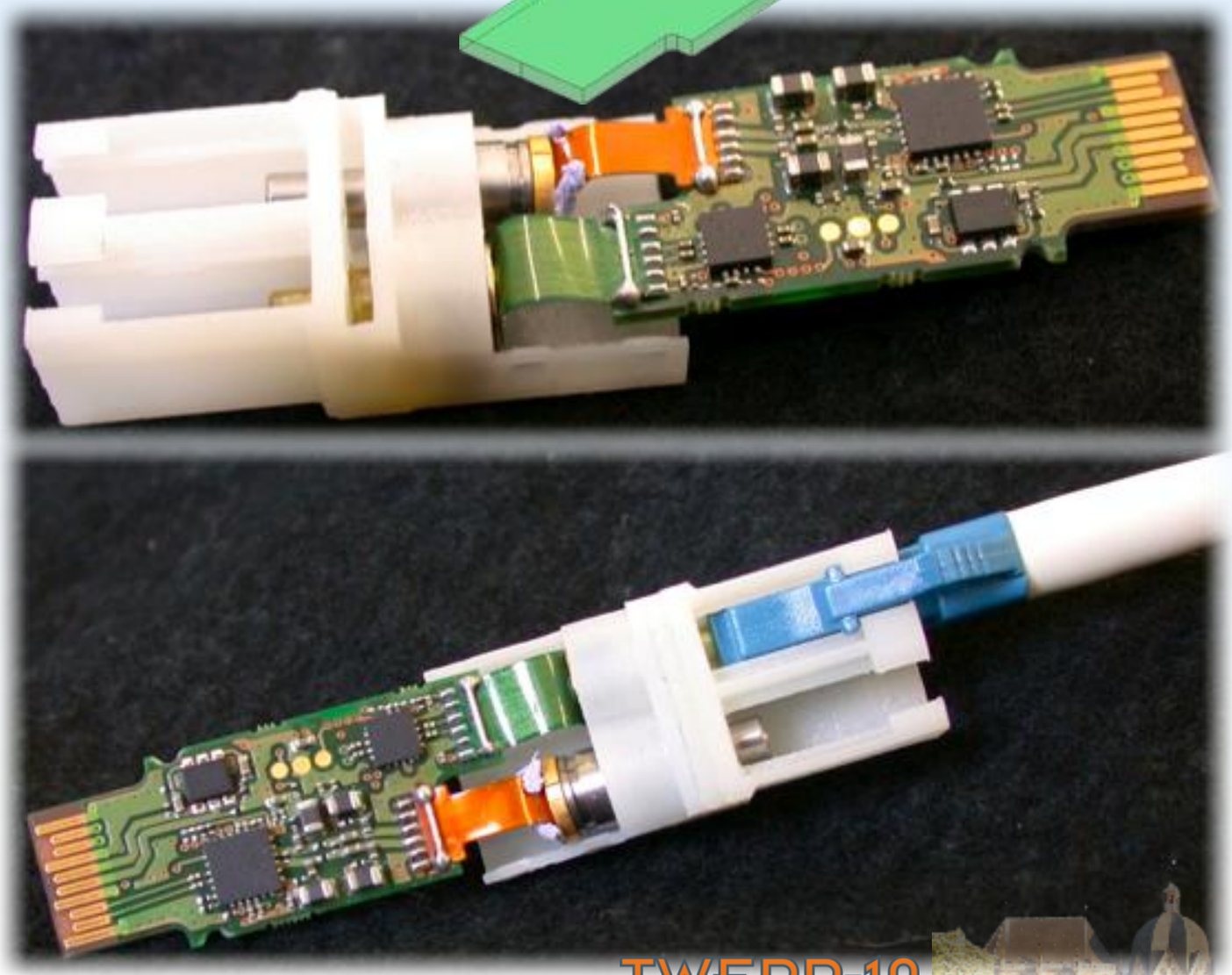


VTRx low-mass latch design

- Working on mechanical design of VTRx connector latch to reduce overall mass of the transceiver
  - Part mechanically associates connector and TOSA/ROSA
- Rapid prototype plastic samples successfully tested







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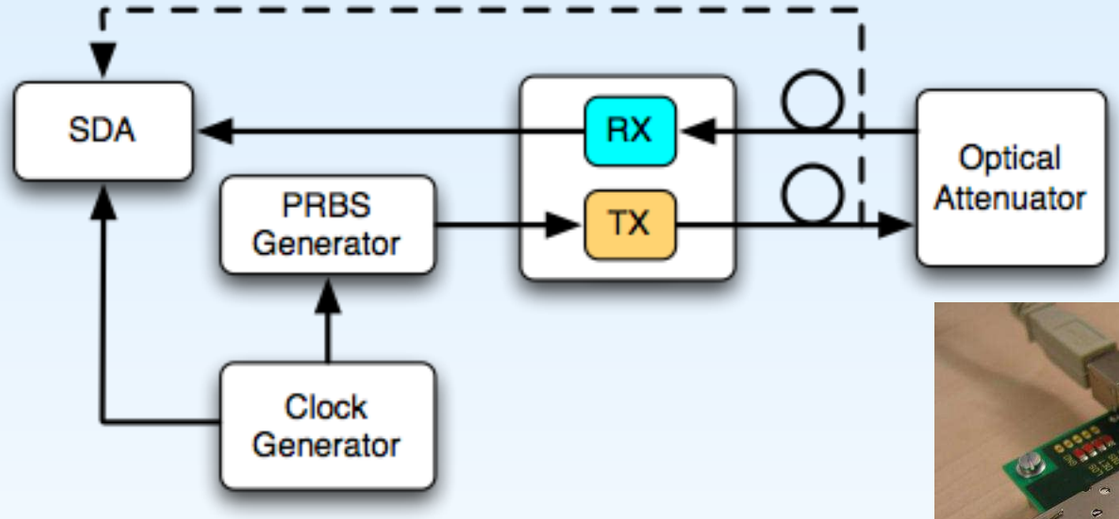
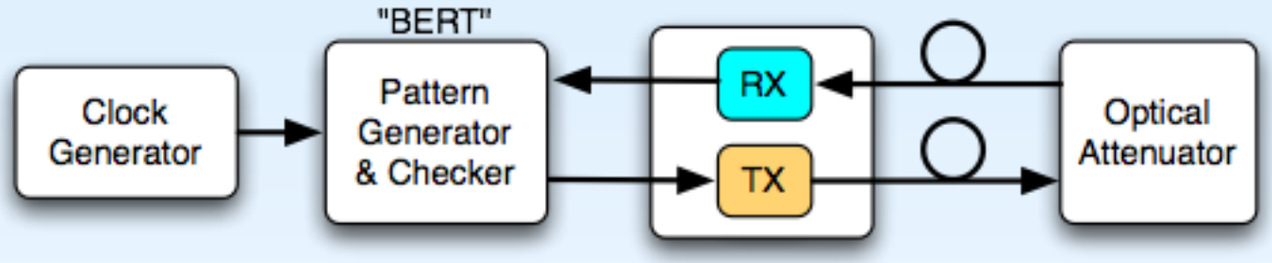
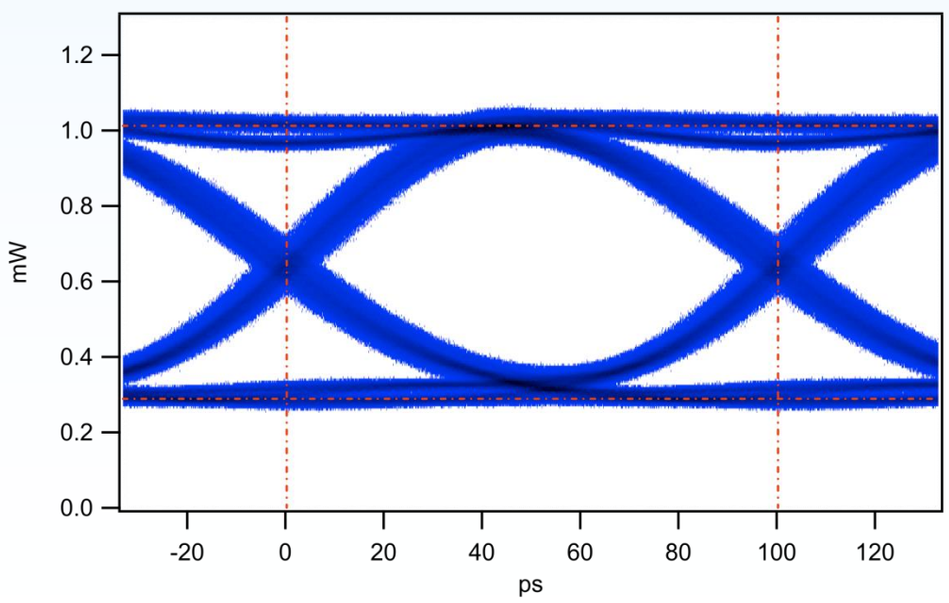
Functionality Testing Overview

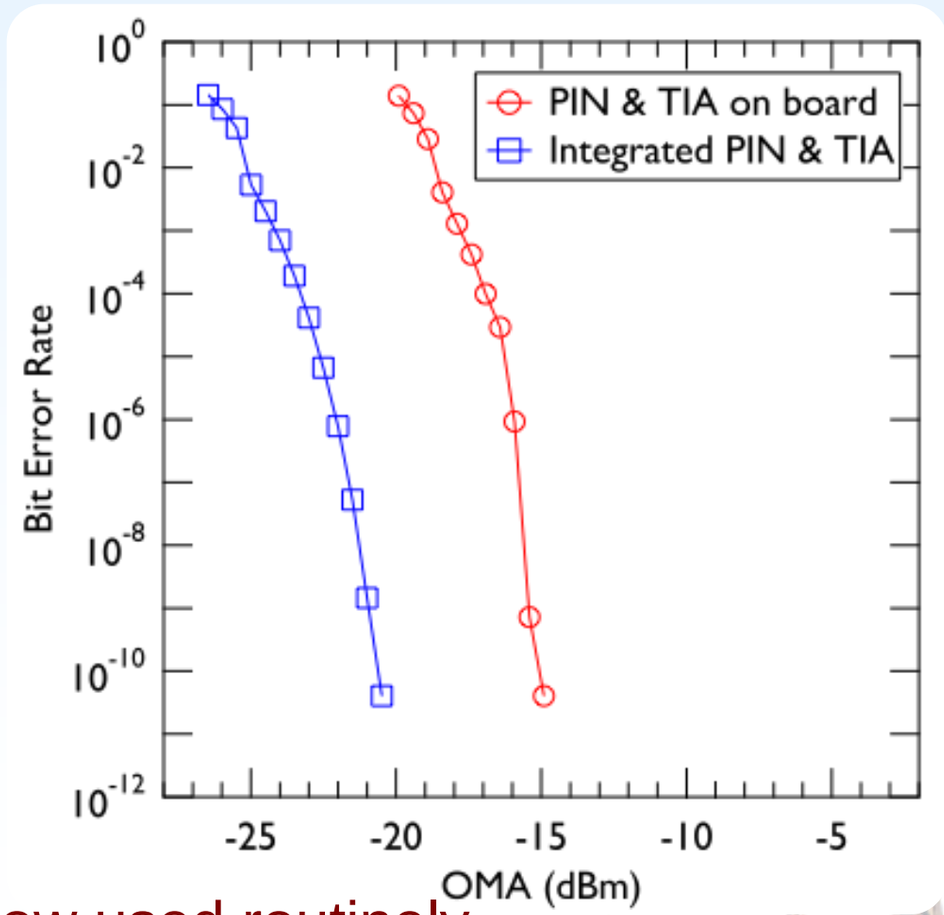
Versatile Link

1. Signal “Eye” Diagrams - optical for TX, electrical for RX
2. Bit Error Test (BERT)





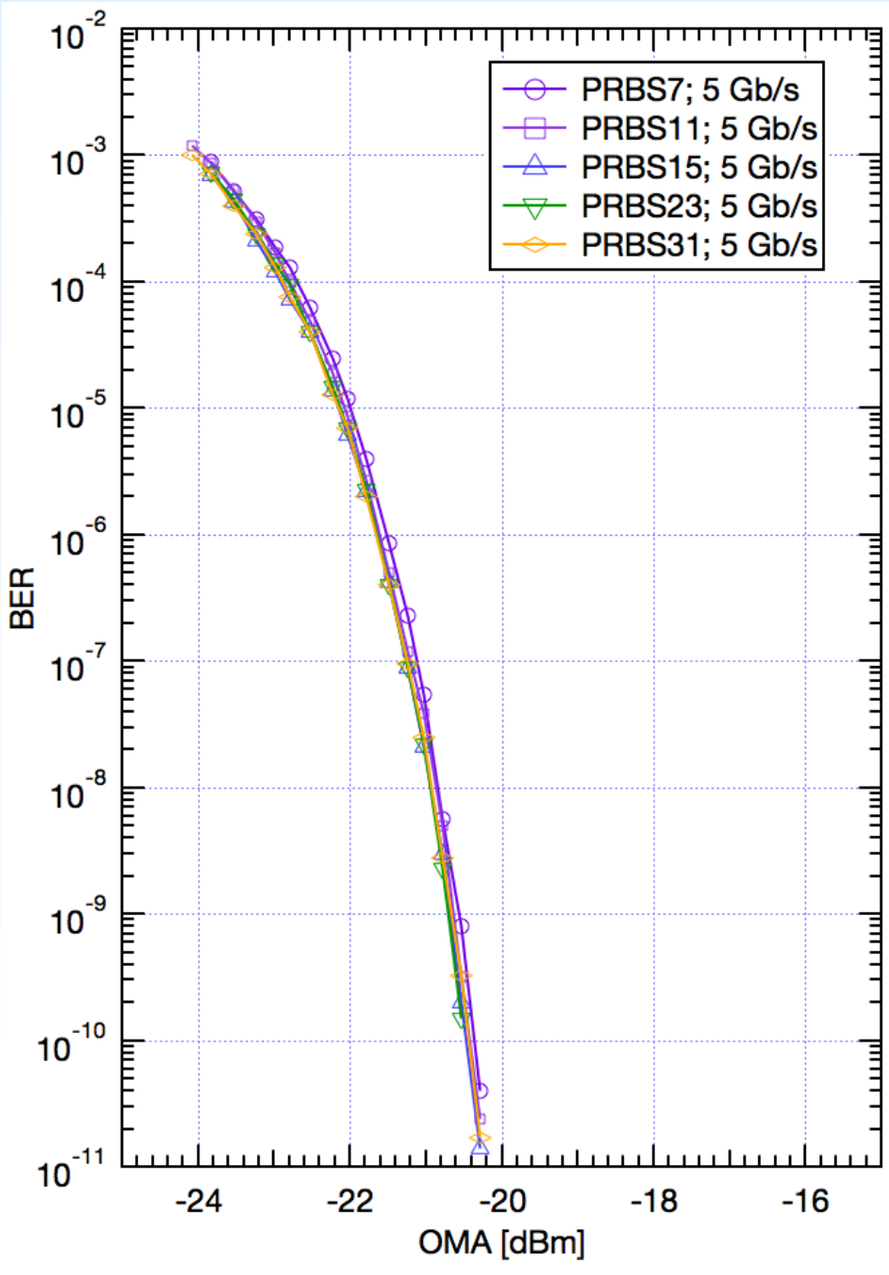


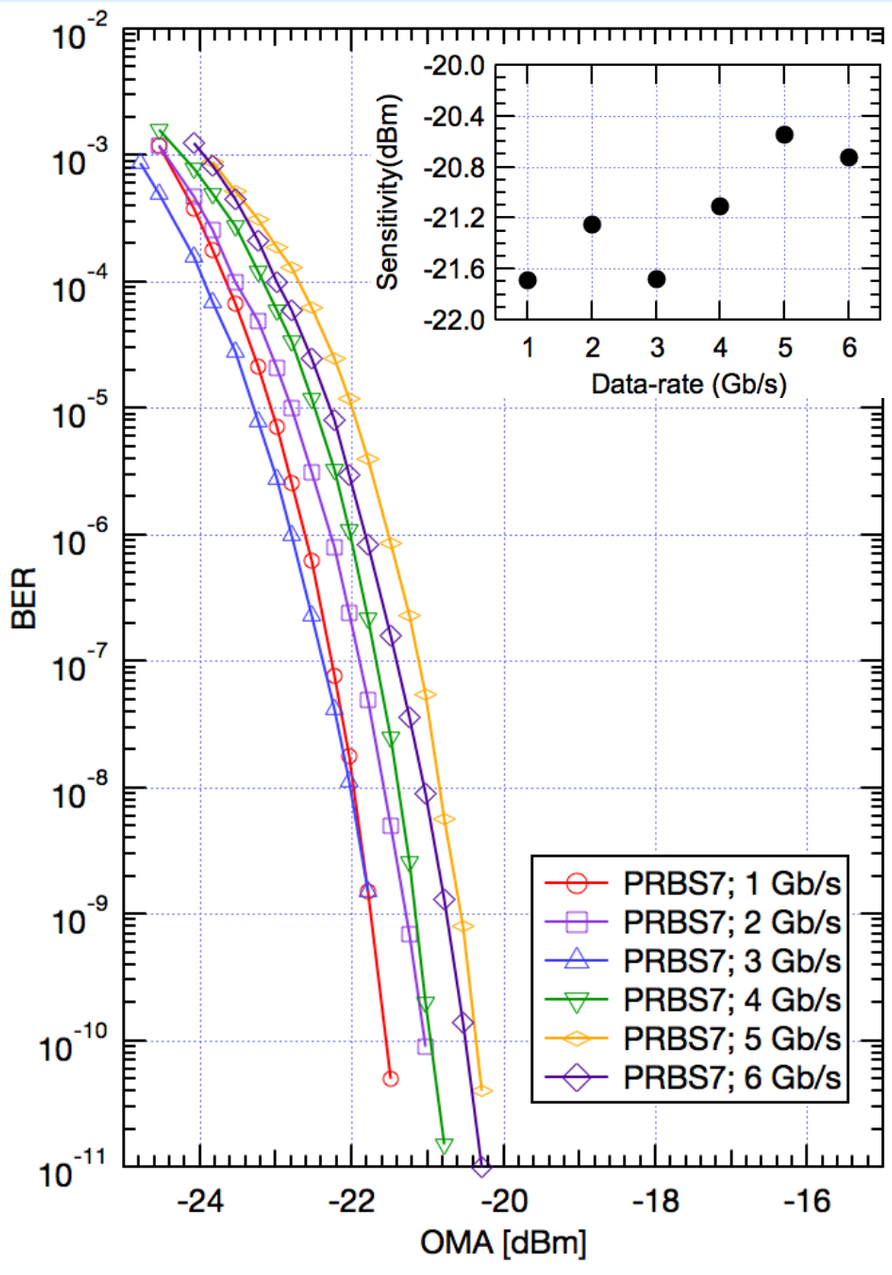


Test Methods now used routinely

GBTIA ROSA performance

- Evaluate impact of data-rate and pattern length on GBTIA ROSA sensitivity



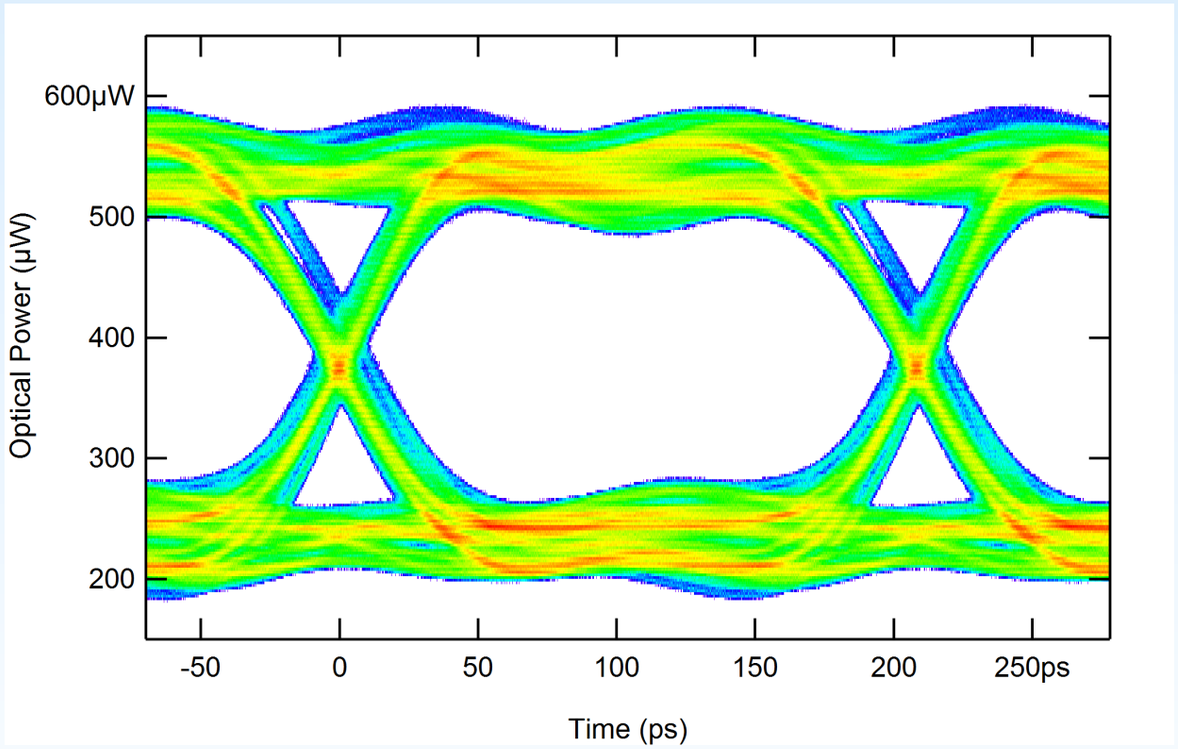


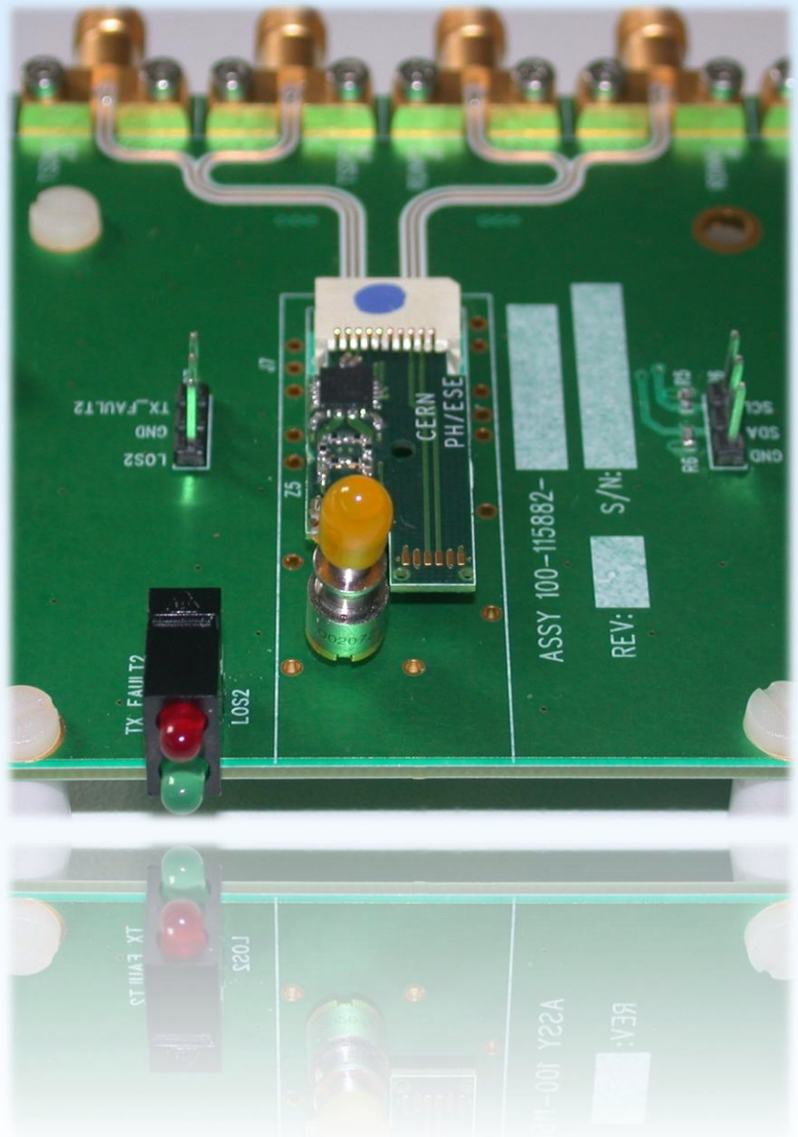
- Favourable comparison to bare-die tests
  - ROSA pkg not detrimental to functionality
- No pattern length sensitivity
- Expected reduction in sensitivity with data-rate
  - Acceptable magnitude

VTRx transmitter performance

Versatile Link

- SFP+ prototype using commercial EE laser and driver @ 4.8 Gb/s





DDj = 19.8 ps, Rj = 1.19 ps => Tj = 35.8 ps (0.17UI)

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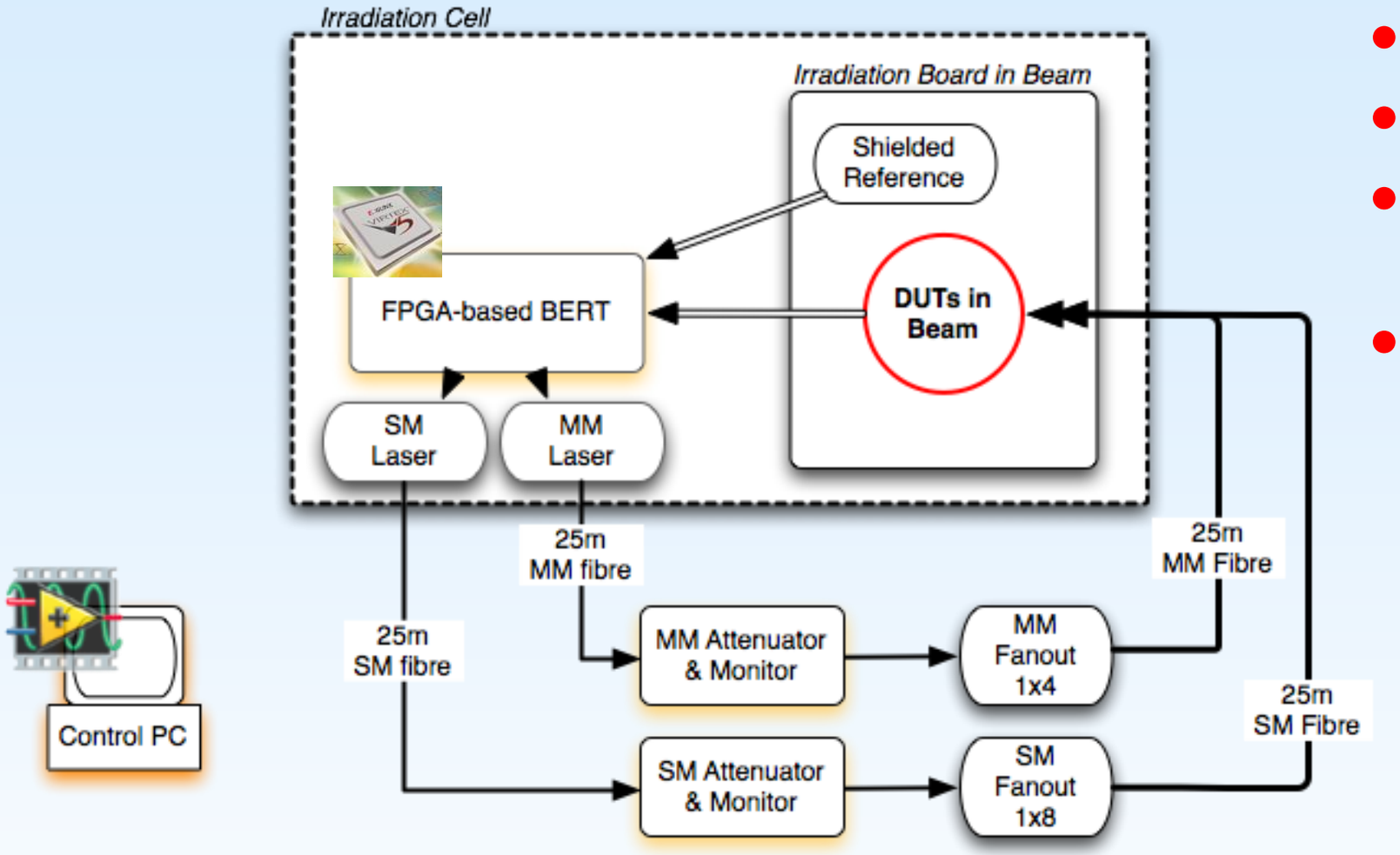
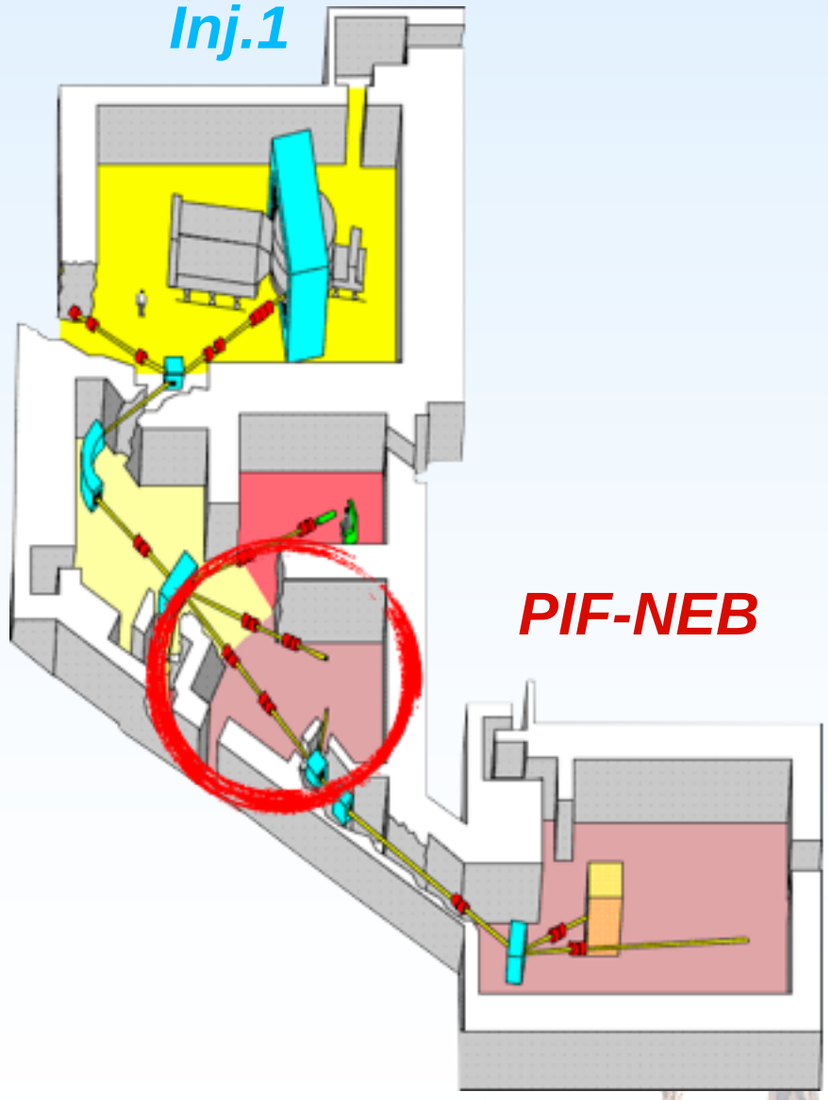
PSI Proton SEU Test



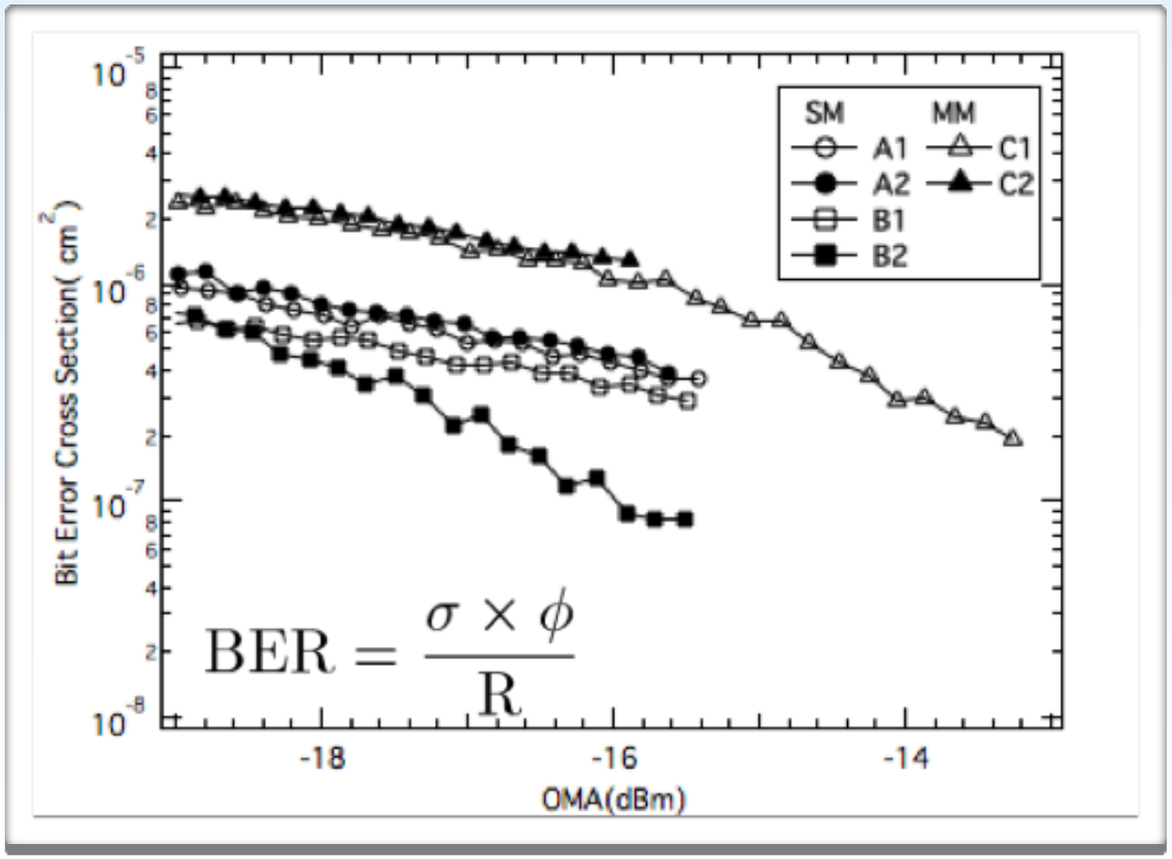
- 62.91 MeV p+ beam
- 1-4x10^8 p/cm^2/s
- ø 60 µm InGaAs PIN and GBTIA ROSA
- ø 80 µm GaAs ROSA



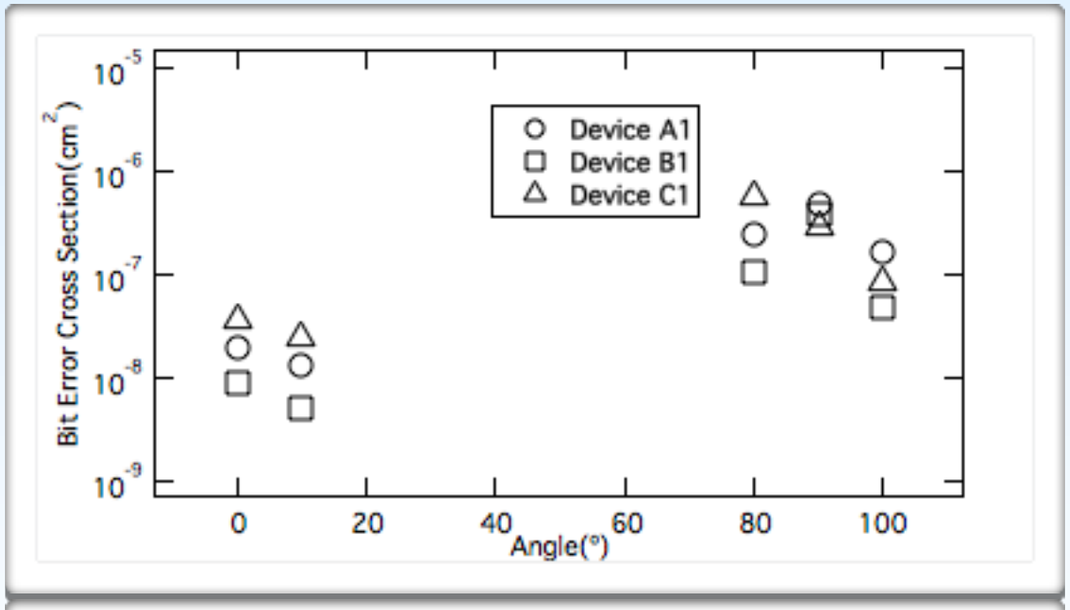
- Cross-check previous burst-error results & test GBTIA SEU immunity
- Xilinx Virtex-5 based BERT
  - Six channels, 2 Gb/s to 6 Gb/s
  - GBT encoding inc. FEC, Error logging
- Labview-based instrument control

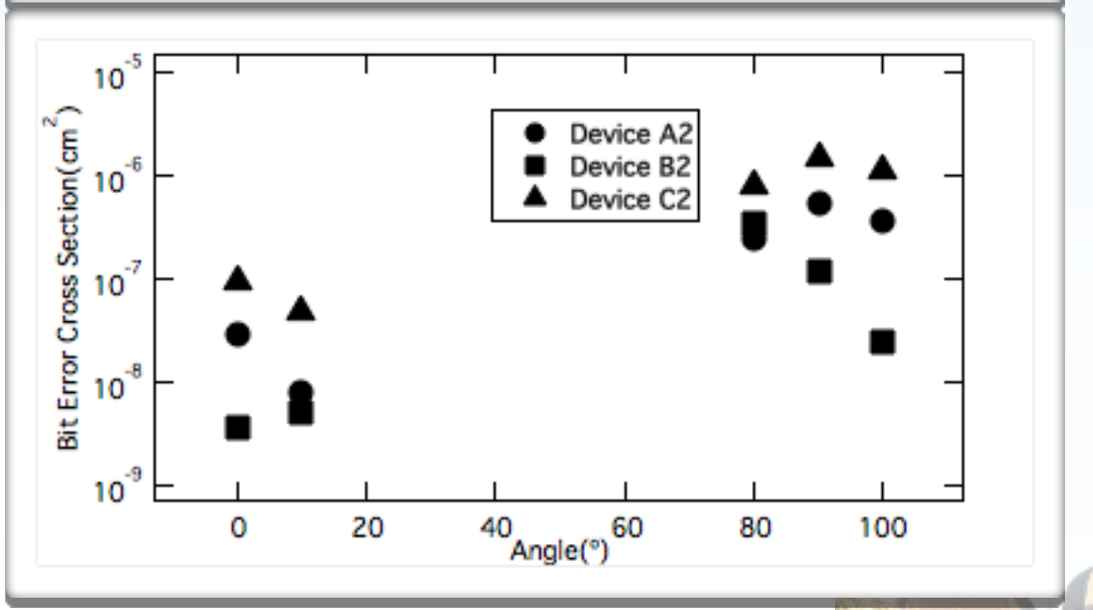
SEU test result preview (1/2)

- Similar overall trend but several orders of magnitude difference in response between devices
  - SM PINs A1 and A2, GBTIA ROSA B1 and B2, MM ROSA C1 and C2
- Best performance from GBTIA ROSAs (square symbols)



Results for near grazing incidence @ 3Gbps

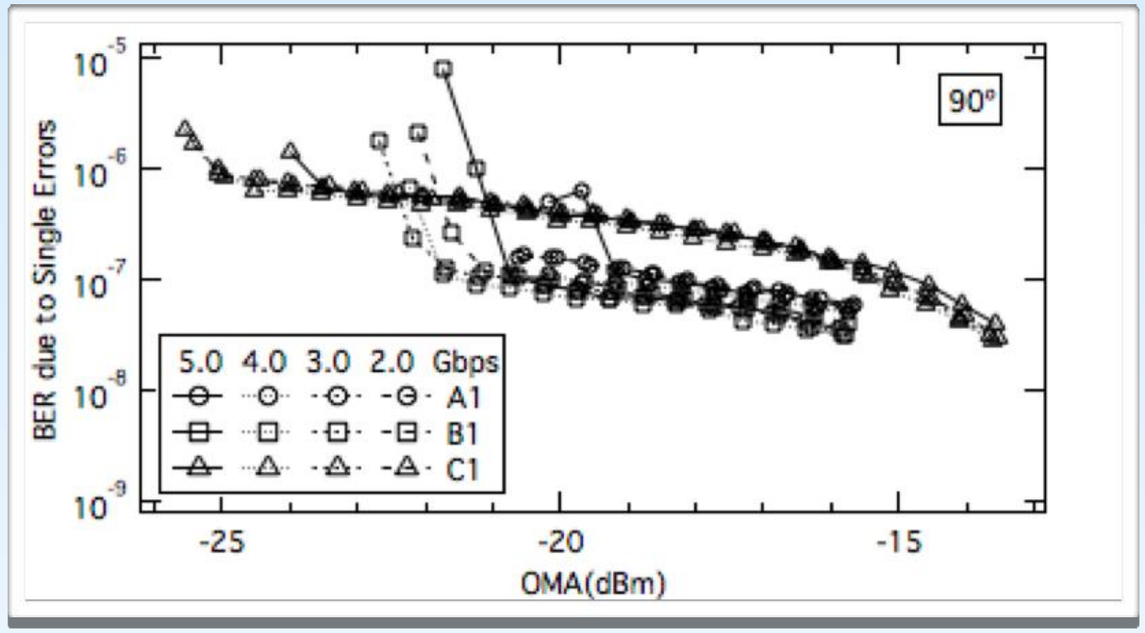


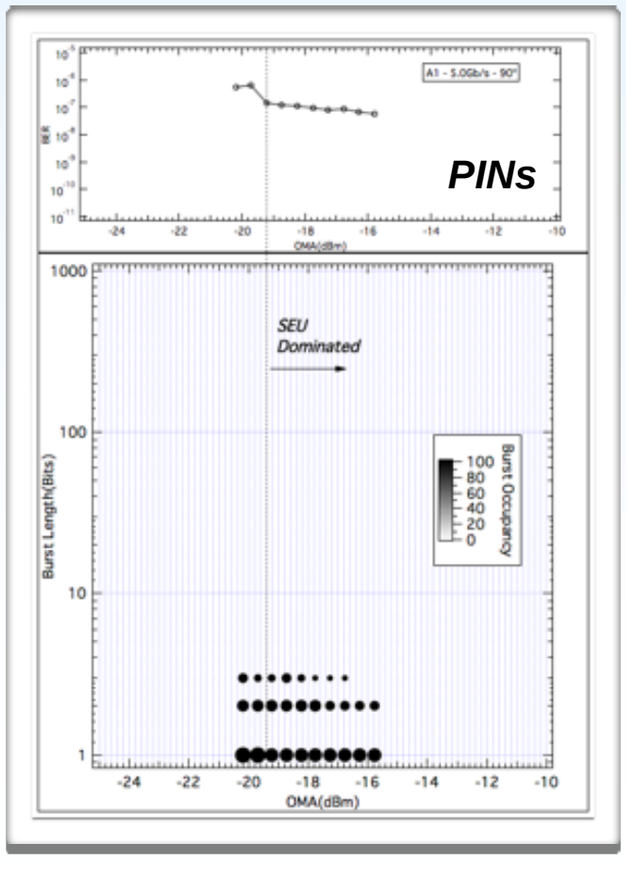


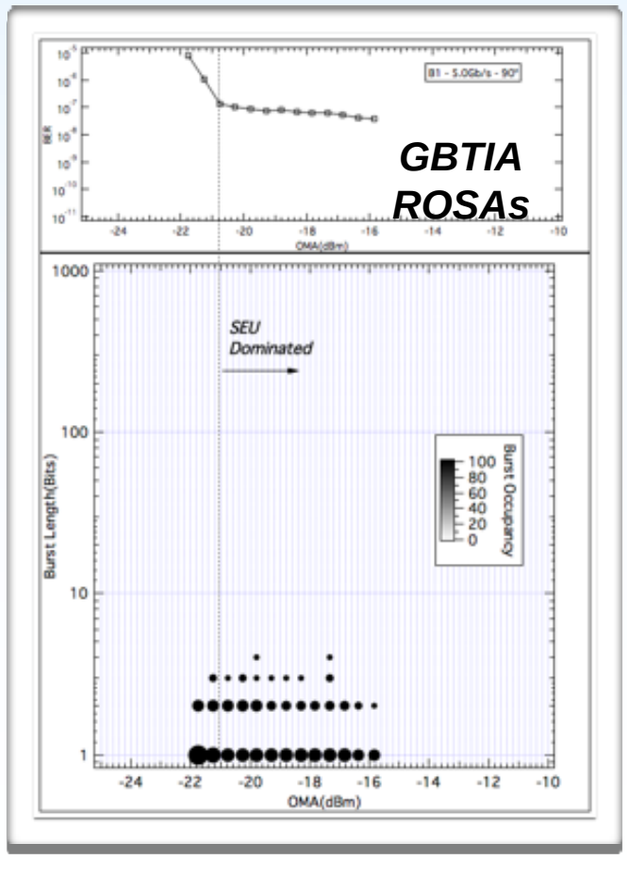
Bit Error Cross Section as a function of the incidence angle,
90 == grazing incidence
0 == normal incidence

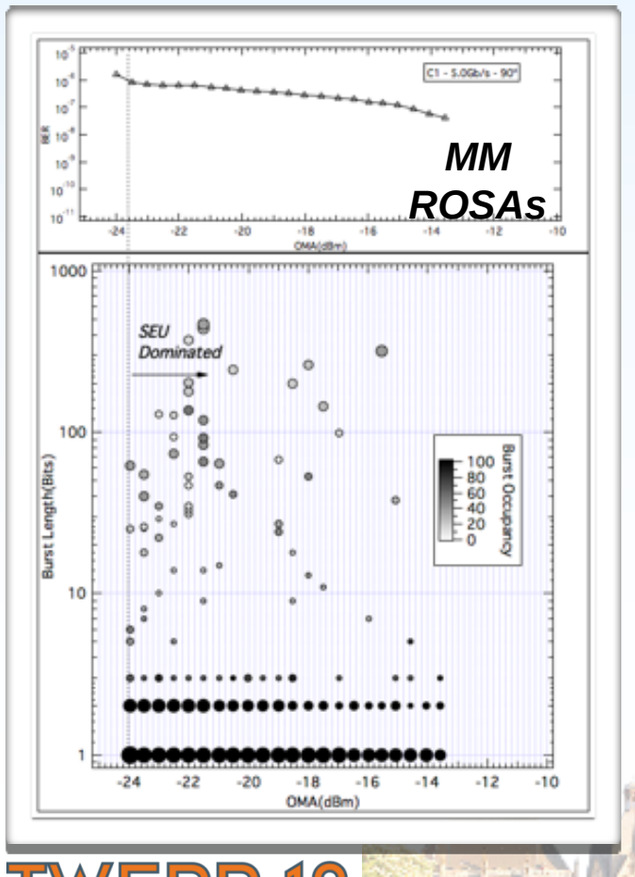
SEU test result preview (2/2)

- BER due to single bit flips is similar for all devices
- BER is independent of data rate within the range of investigation
- Burst lengths limited in PINs and GBTIA ROSAs
- Longer bursts seen in ROSAs with unshielded amplifiers



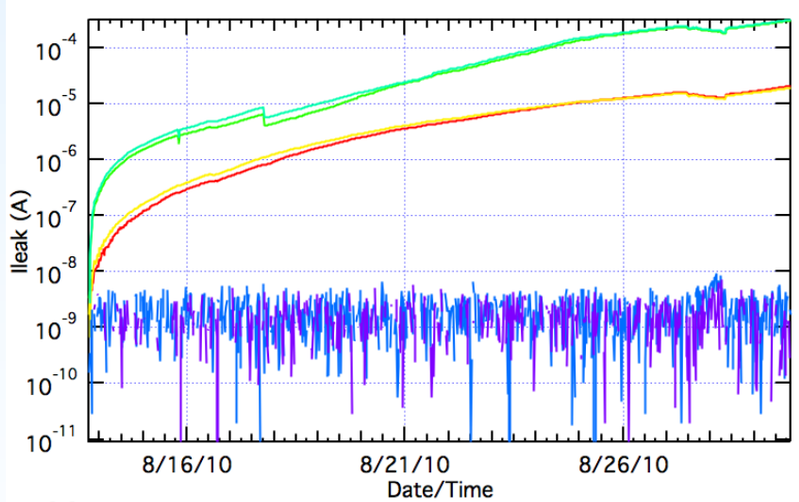


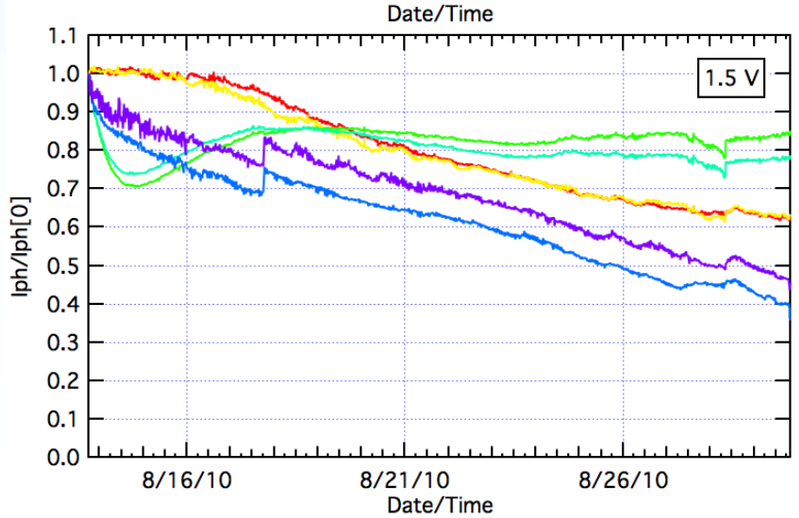




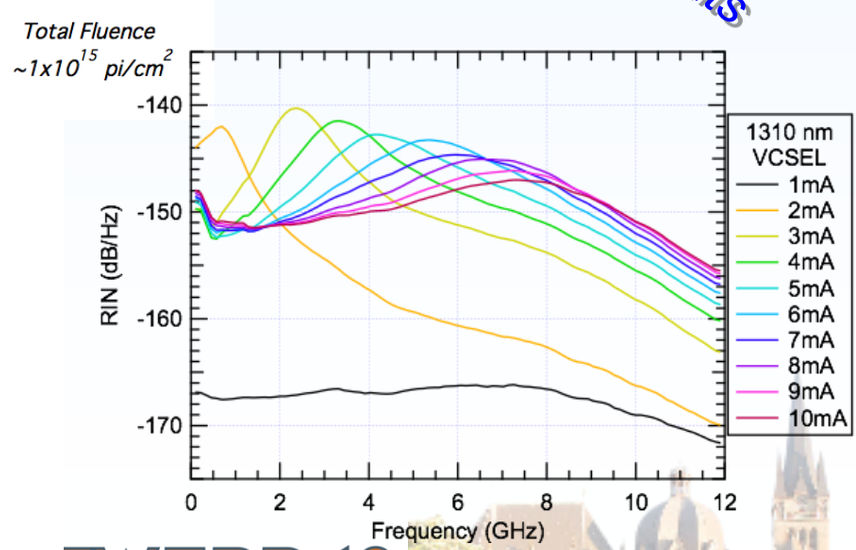
Pion Total Fluence Test (Aug. 2010)

- Cross-check influence of particle species on damage
  - NIEL scaling unproven for complex laser stoichiometry
- End of life prediction
- Online measurement of optical spectra & RIN
  - Track temperature effects & high-speed performance
- Example PIN results show typical behaviour:
  - decreased response
  - increased Ileak (InGaAs)





See Poster by P. Stejskal for discussion of laser results



Summary & future work

- In terms of our Phase II deliverables
  - Specifications for on-detector components
    - Available and under discussion within Versatile link project, soon to be distributed more widely
  - Packaging
    - In-house development of both PCB and mechanical pkg progressing well
    - Successful integration of GBTIA and PIN into ROSA
      - Detailed measurements of multiple devices in near future
    - Defining strategy for future variants (GBLD, TOSA types)
  - Functional test methods applied to testing of transmitters and receivers
    - Excellent performance of GBTIA ROSA
    - Performance limitation of current VTRx design being studied in simulation
  - Radiation Testing
    - SEU test results compare well with previous results
      - Burst errors not observed in GBTIA or high-speed commercial TIA
    - Pion test carried out, lots of data to analyse