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Progress and Advances in Serial Powering of Silicon Modules for the ATLAS Tracker Upgrade

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On behalf of the SP Community

Thanks to Martin Gibson (RAL), Richard Holt (RAL), Dave Lynn (BNL), Peter Phillips (RAL) and Giulio Villani (RAL)

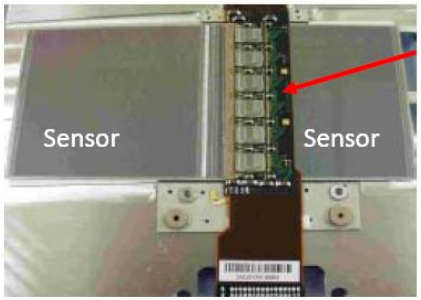
Outline

- powering issues for the ATLAS strip tracker upgrade
- the serially powered (SP) detector stave
- shunt regulator options
- protection against chain failure
- current source developments
- the SP stavelet program
- SP stavelet test results
- summary and conclusions

The present SCT

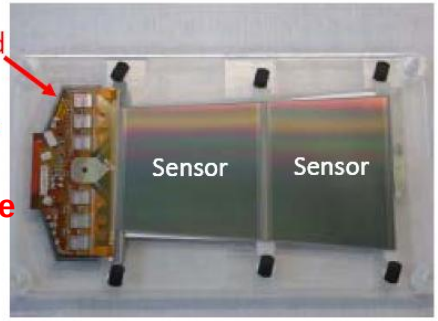
- 4088 Detector Modules
  - 3.2M channels
- Independent Powering
  - 4088 cable chains
  - 22 PS racks
  - 4 crates / rack
  - 48 LV and 48 HV channels/crate
- Overall efficiency ~40%
  - Cable R => voltage drops

current SCT module design



Barrel Modules

Kapton Hybrid
With 6 ABCD
readout chips
on each side
768 chan/side



Forward Modules

Upgrade Tracker:
need 34 M channels to cope
with increased luminosity

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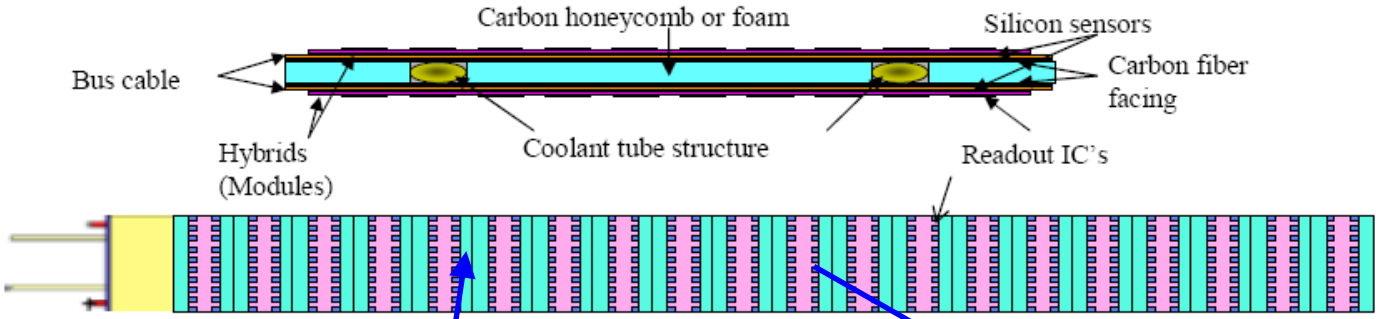
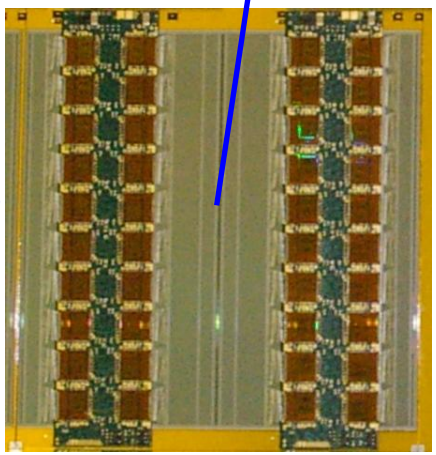
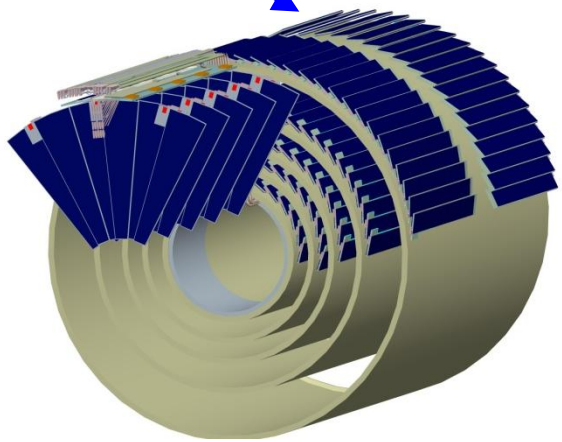
Upgrade strip tracker: Stave and Petal Concept



detector module:
10 by 10cm Si
4 columns of strips
40 ABCN-25 chips
5120 channels





detector staves arranged into barrels
detector petals arranged into discs

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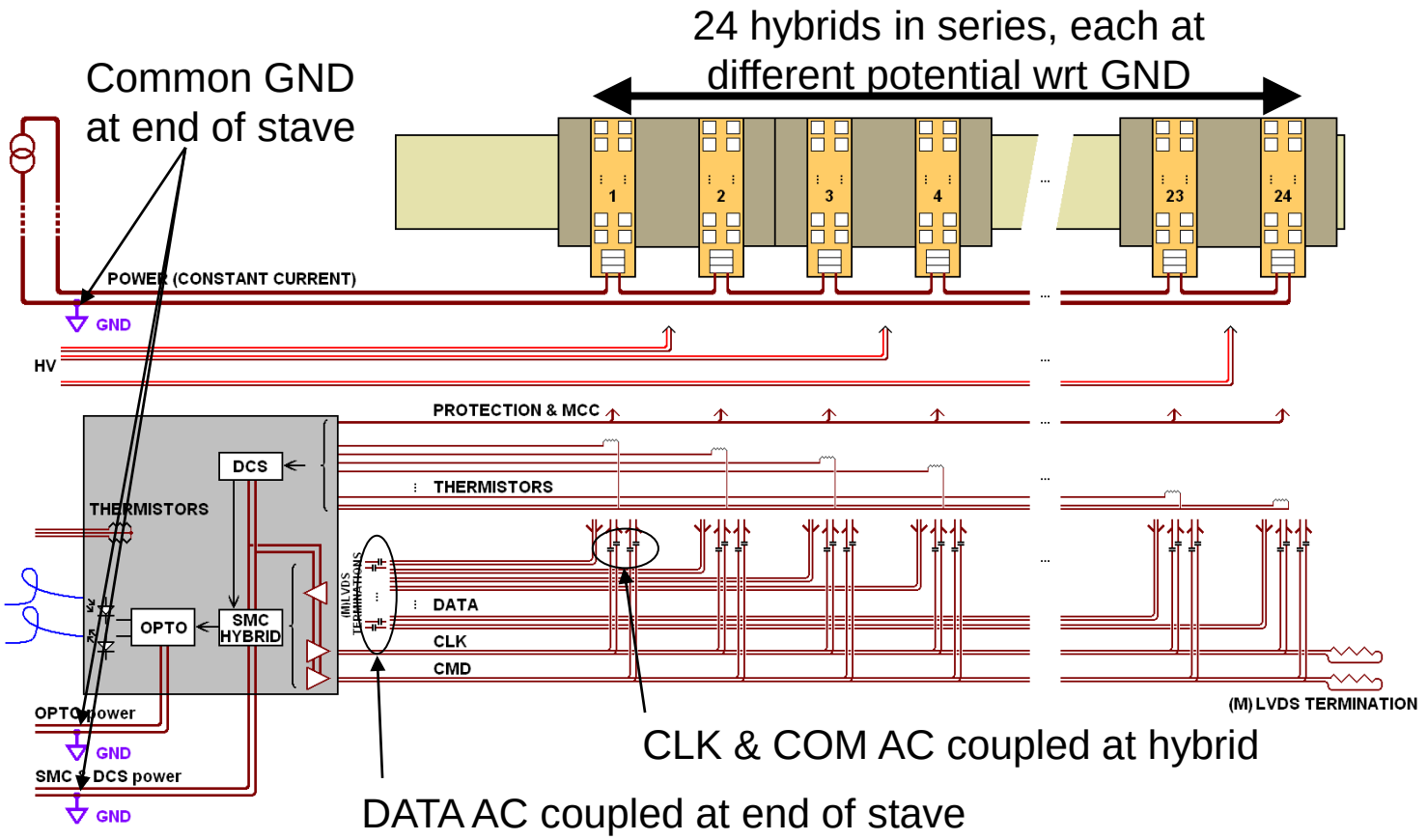
Serially Powered Stave Architecture



staves carry 12 detectors, 24 readout hybrids per side
each hybrid carries 20 ABCN ROICs
each module must carry a shunt regulator to keep supply V constant
powering by DC-DC converter is a competing/complementary option
currently prototyping 4 module “Stavelets”

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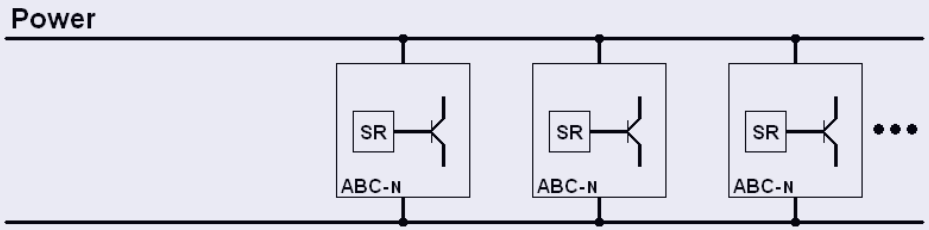
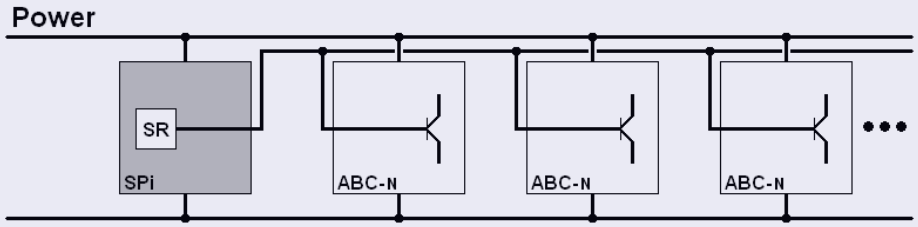
Shunt Regulator Architectures with ABCN-25

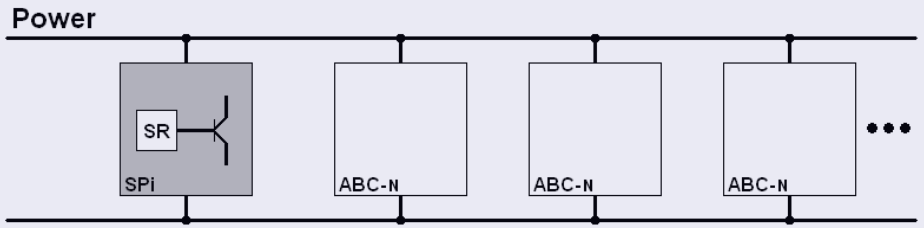
- **Hybrid with Shunt "W"**
  - Use each ABCN-25 integrated shunt regulator
  - Use each ABCN-25 integrated shunt transistor(s)



- **Hybrid with Shunt "M"**
  - Use one external shunt regulator
  - Use each ABCN-25 integrated shunt transistor(s)
    - Two (redundant) shunt transistors, 140mA each



- **Hybrid with SPi (or similar)**
  - Use one external shunt regulator
  - Use one external power transistor



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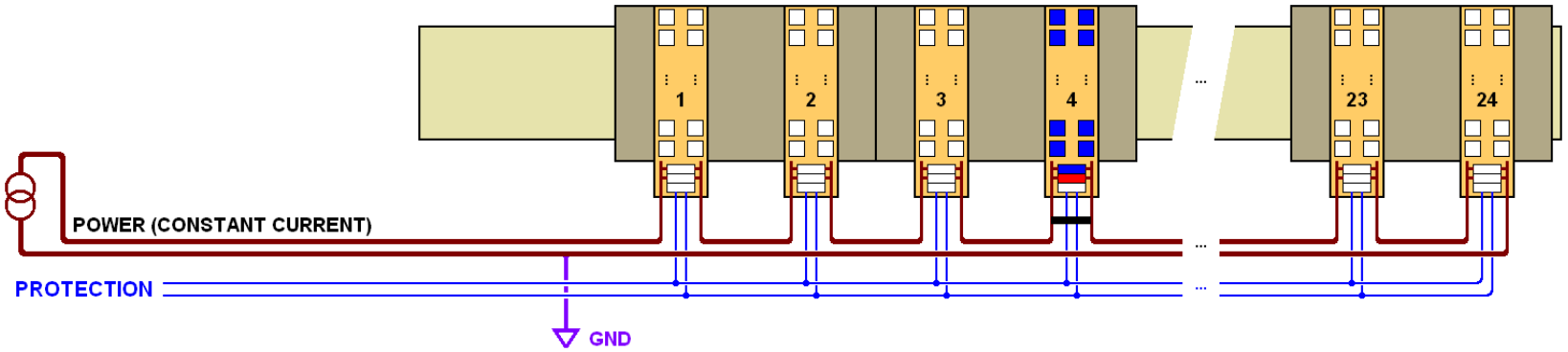
Protection of SP against faults



- What happens if a module fails open circuit?
- What happens if a module becomes a noise generator?
- How to turn modules on/off?

We could provide a system to “short out” each module under control of DCS

- Voltage across shorted module should be small
- Area of components and number of control lines must be small
- Protection circuit must draw minimal power when module active

- Automatic over voltage protection is desirable

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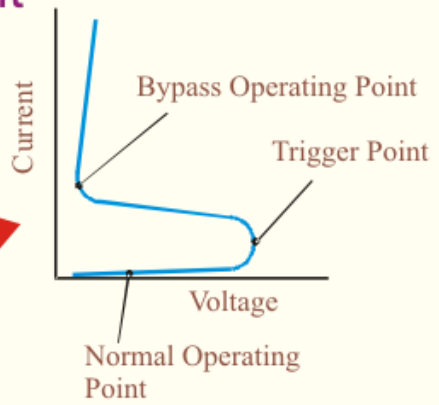
Power Protection Board(PPB) Circuit

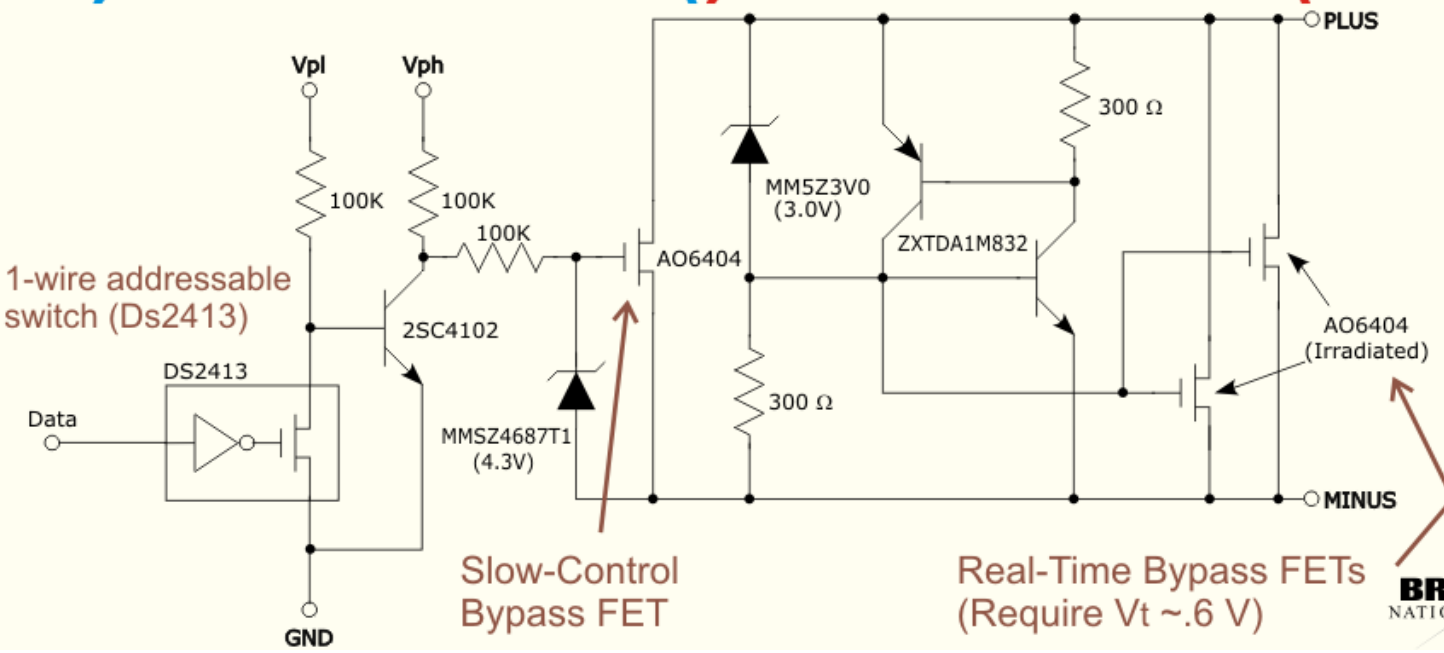
- Real-time circuit detects over-voltatge condition and latches Vds to less than 800 mV.
- DCS (or Maxim 1-Wire) enables user to short Vds to < 100 mV.

Note: Extra transistor 2SC4102 and pullup voltage are needed by 1-wire bypass because drain of output FET of the 1-wire device Ds2413 is rated only to 28 volts. Vph needs to be ~70V for 24 hybrids in series. Custom design would eliminate one transistor and pullup voltage.



DCS Enabled Bypass (V_{ds} < 100 mV)

Real-Time Bypass (V_{ds} < 800 mV)



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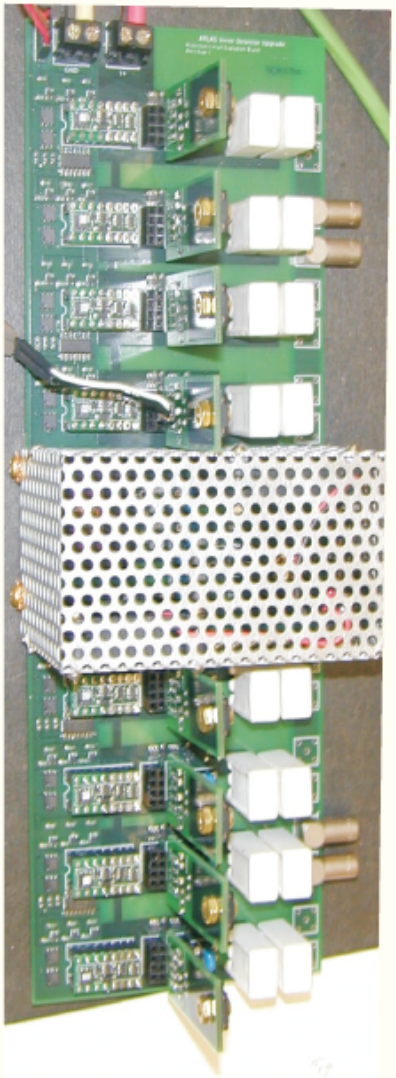
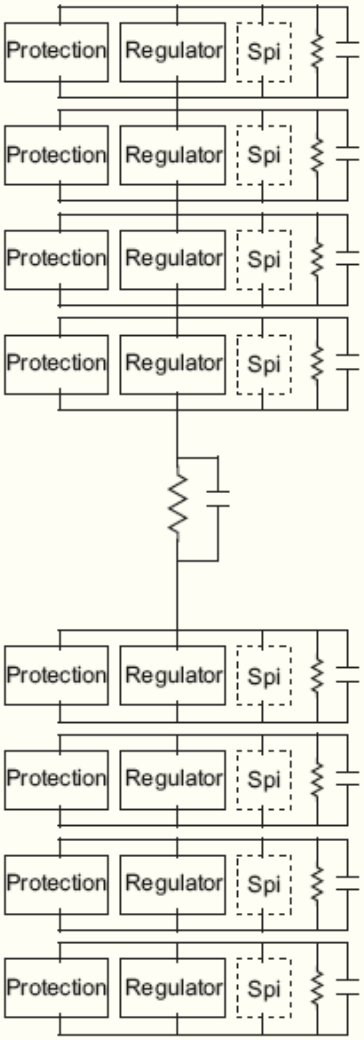
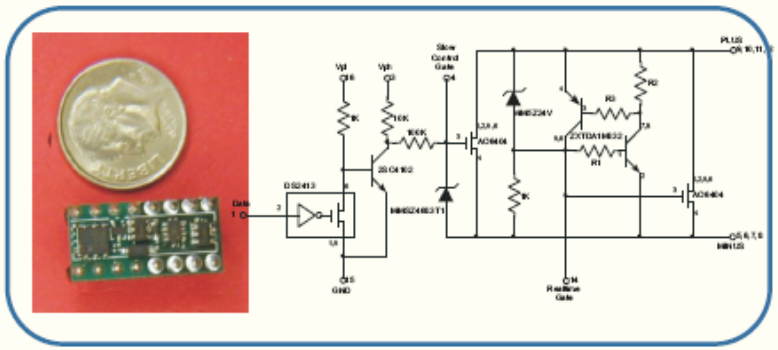
PPB system test studies

SP System Test Board

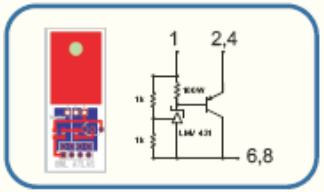




Protection Circuit- Protoype I



Regulator Board



SPi Board

System Test Board

- Mimics 8 hybrids + 8 virtual hybrids
- 16 x 2.5 V = 40 volt operation
- Test real-time circuits; allows 1-wire controlled "open circuits" in variety of "hybrid" locations
- Test multiple 1-wire bypass circuits
- Mimics clock dependent variable module current loads for noise tests
- SPi chip compatible
- Study power-up issues

Note: Thermal issues limit current to 2.5 Amps

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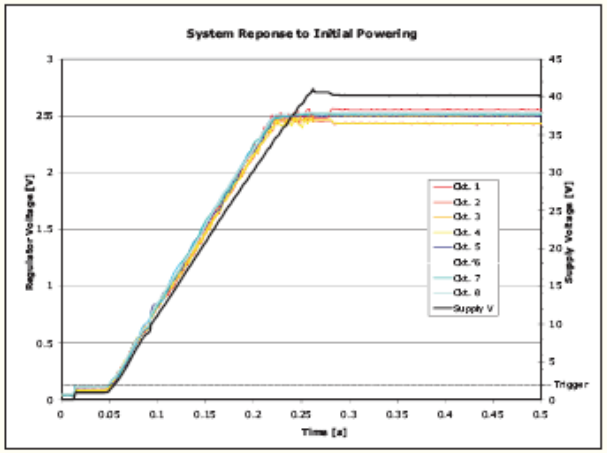
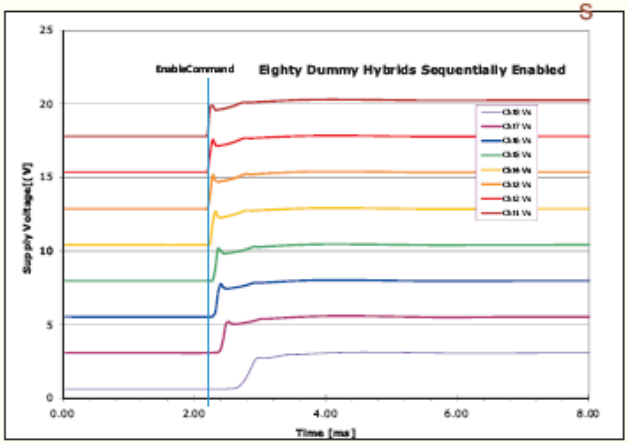
PPB system test results

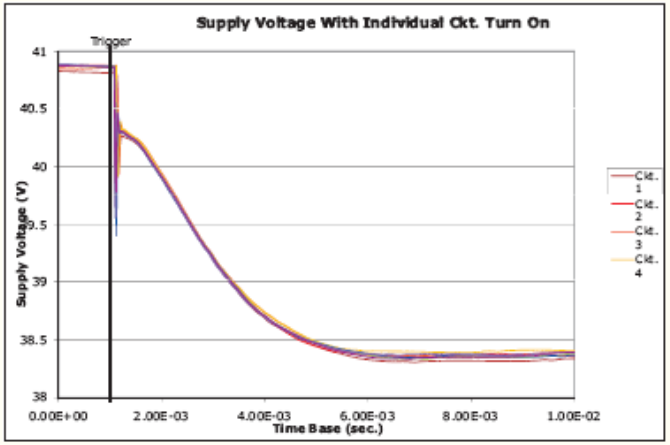
Simultaneous Power-Up



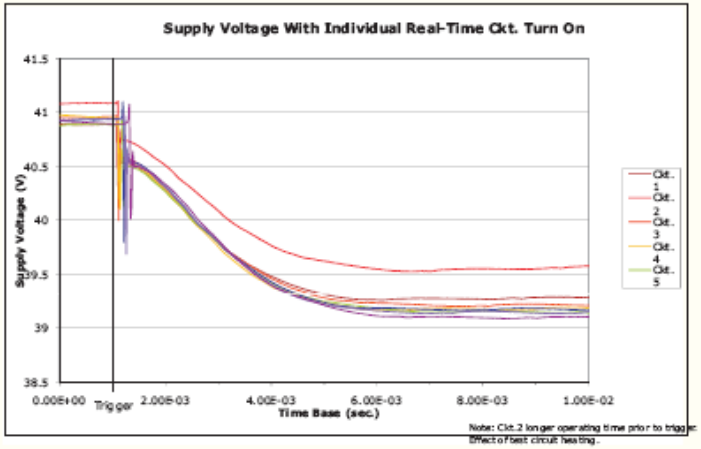
Sequential Power-Up Via 1-Wire Bypass Disable



Change in Supply Voltage When Hybrid is DCS Bypassed



Change in Supply Voltage When Real-Time Bypass is Enabled



- *System Tests all show protection circuit behaves as expected in a serial chain of dummy hybrids.*
- *More details in power working group session*

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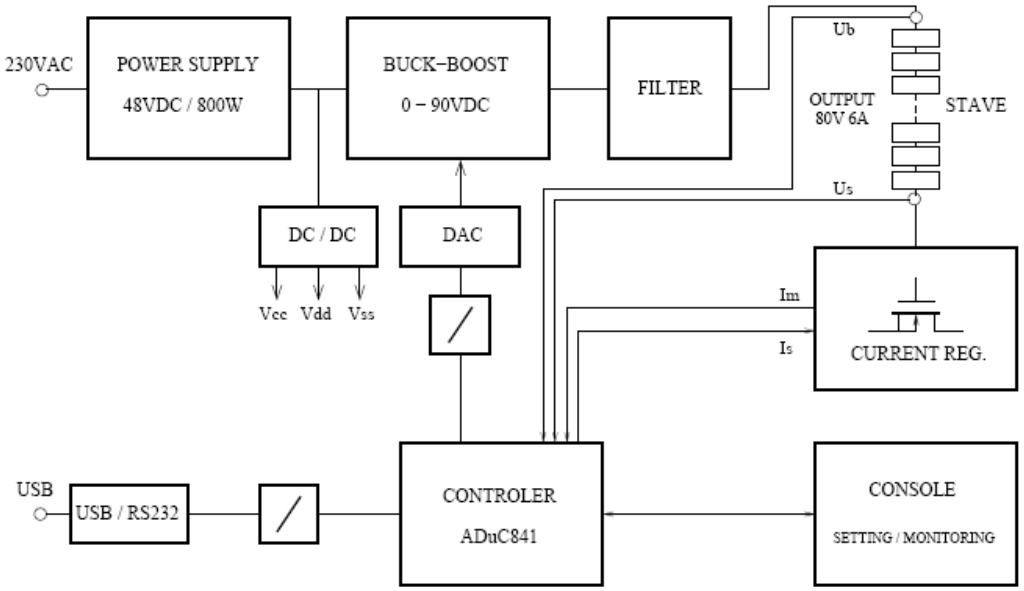
Programmable Constant Current source



- **programmable current source** has been prototyped **(**J.Stastny, ASCR)
- specifically designed for stave09 (ABCN-25), output up to 80V at 6A
- current setting resolution 2mA
- isolated USB interface
- overvoltage protection
- it should work well also for ABCN-13
- now under test with stavelets at RAL

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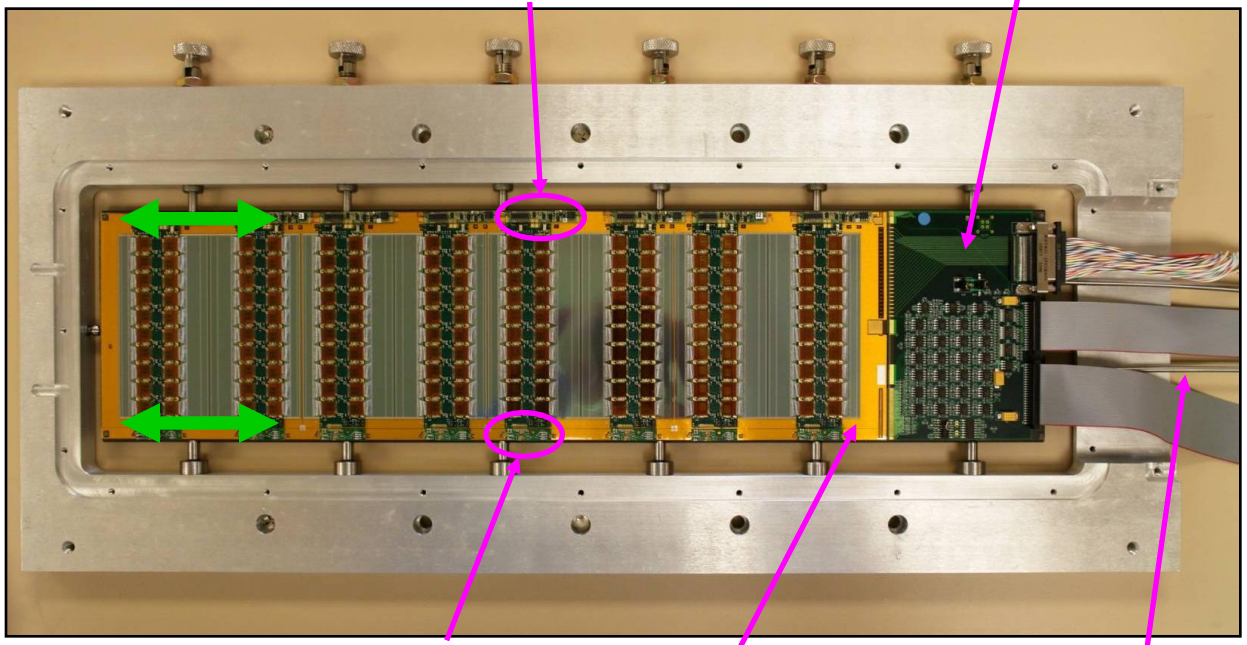
The Stavelet with ABCN-25 readout

power and
power control
communication
(SPI)

data and hybrid
communication
(BCC)



- Allows comparison of: Different power configurations, Different bus cable designs, Different grounding and shielding concepts
- Stavelets allow option choices for later stave construction
- One built, second under costruction at RAL
- PPB carries protection and power plugin

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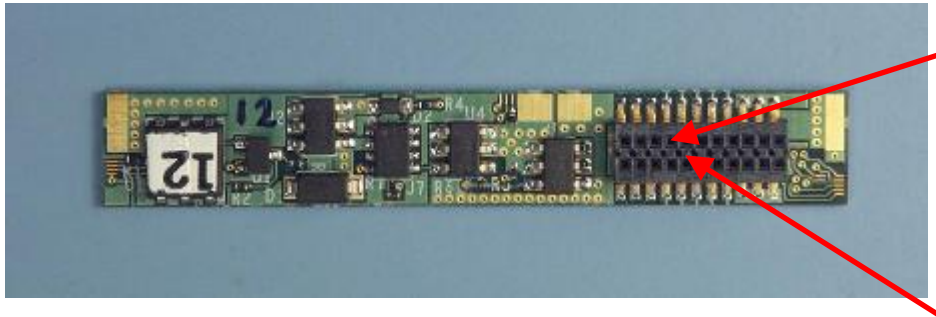
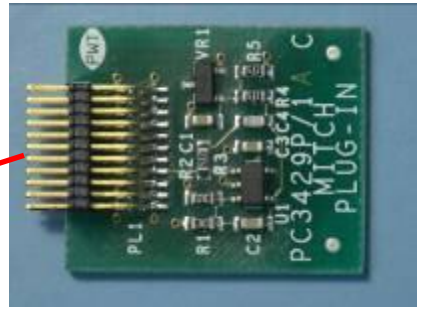
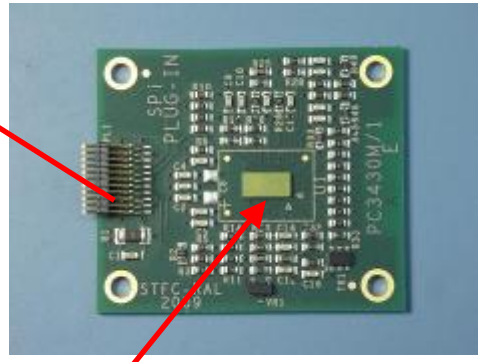
Power Protection board (PPB) and plugins

PPB





dual redundant
distributed
shunt plugin

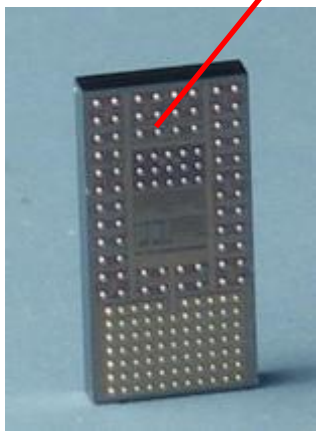


SPI plugin

PPB provided by BNL, implements protection scheme and power connectivity

Hybrid contains basic control circuit for distributed shunt – used for stavelet tests so far

Plug in boards will be used for testing other powering schemes – coming soon !



serial power
interface chip (SPI)
Fermilab

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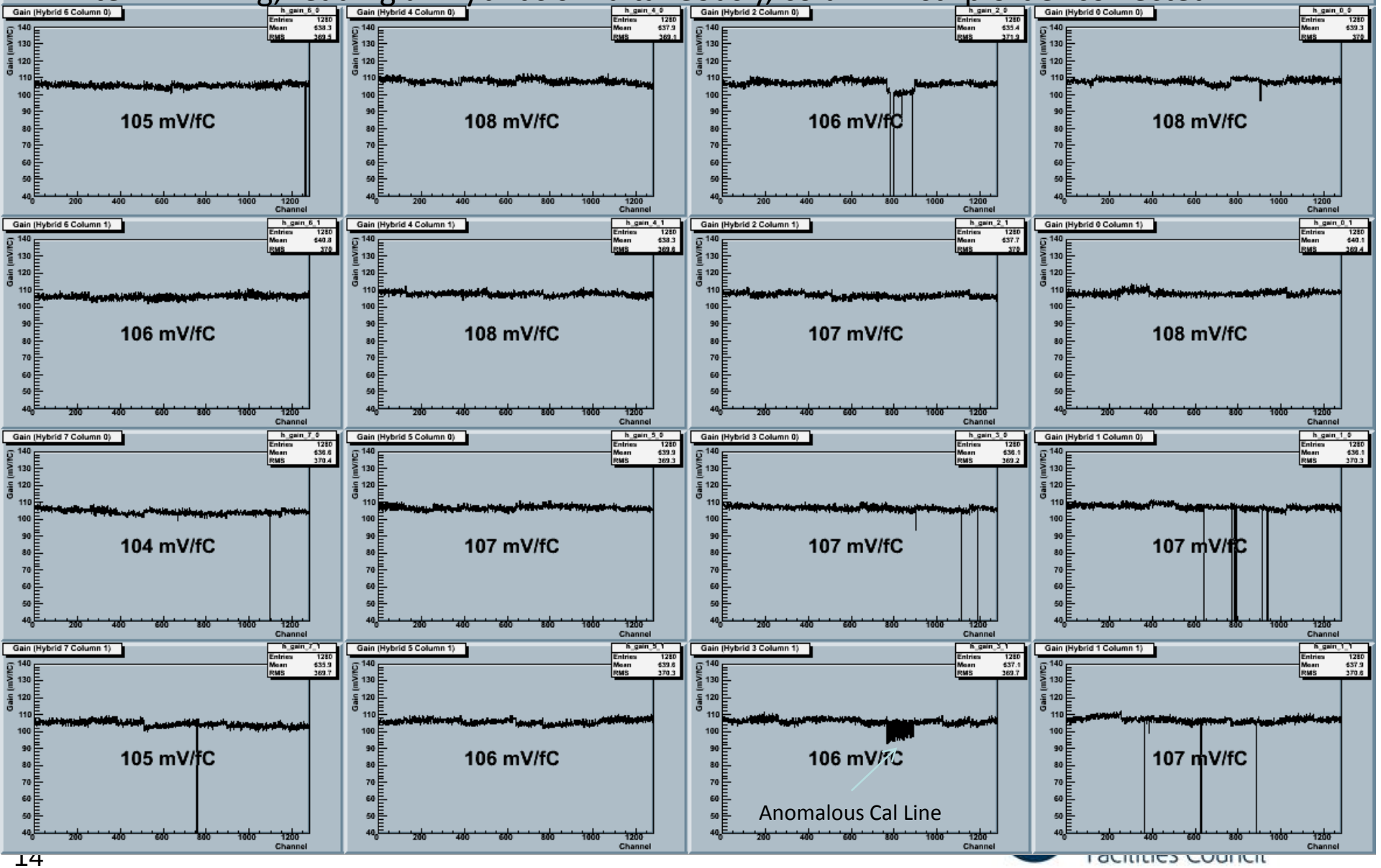
Stavelet GAIN @2fC, JS CS II@5A

Run 1108 Scan 3

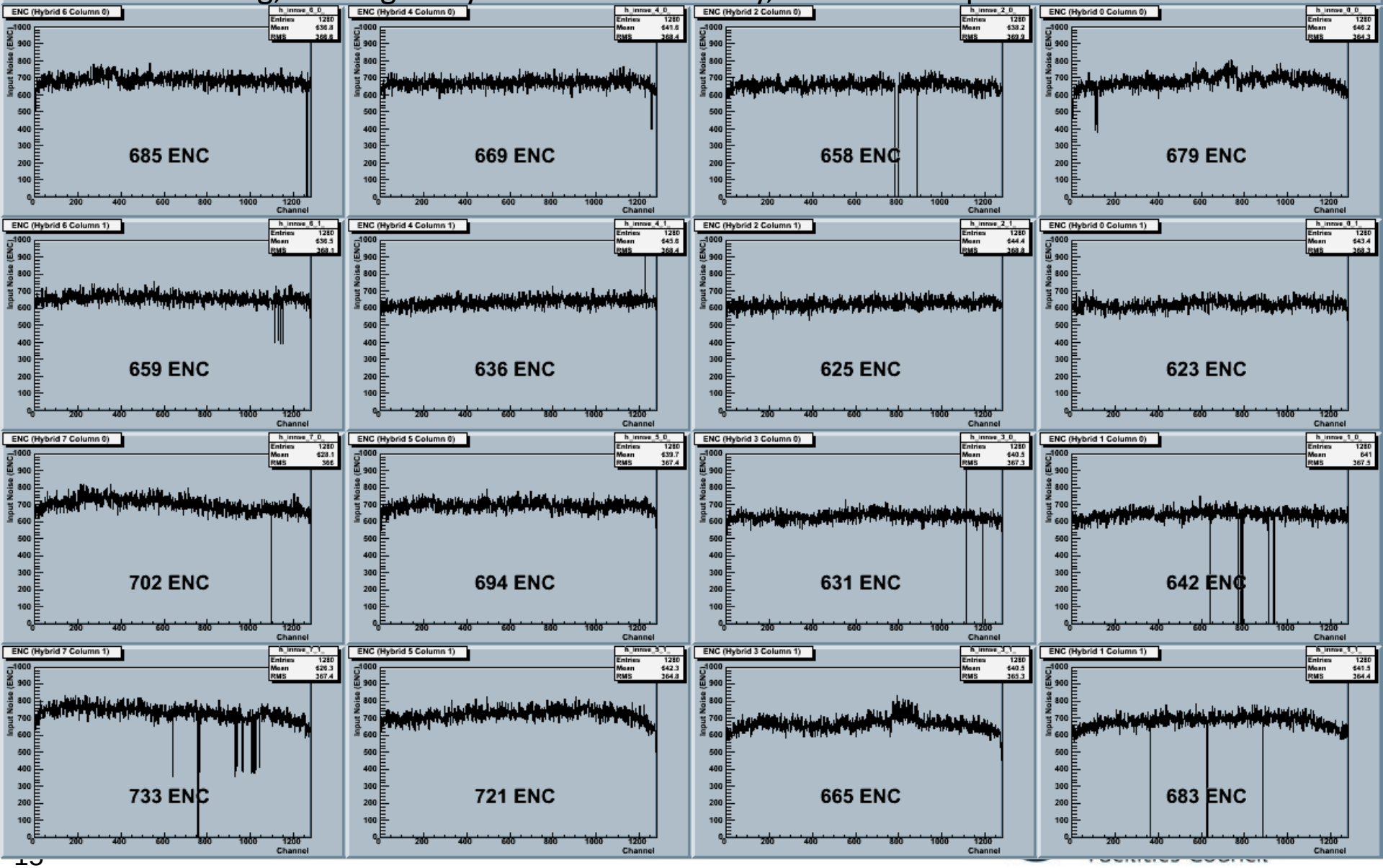
After Trimming, reading *all* hybrids simultaneously, column 1 strip order corrected.



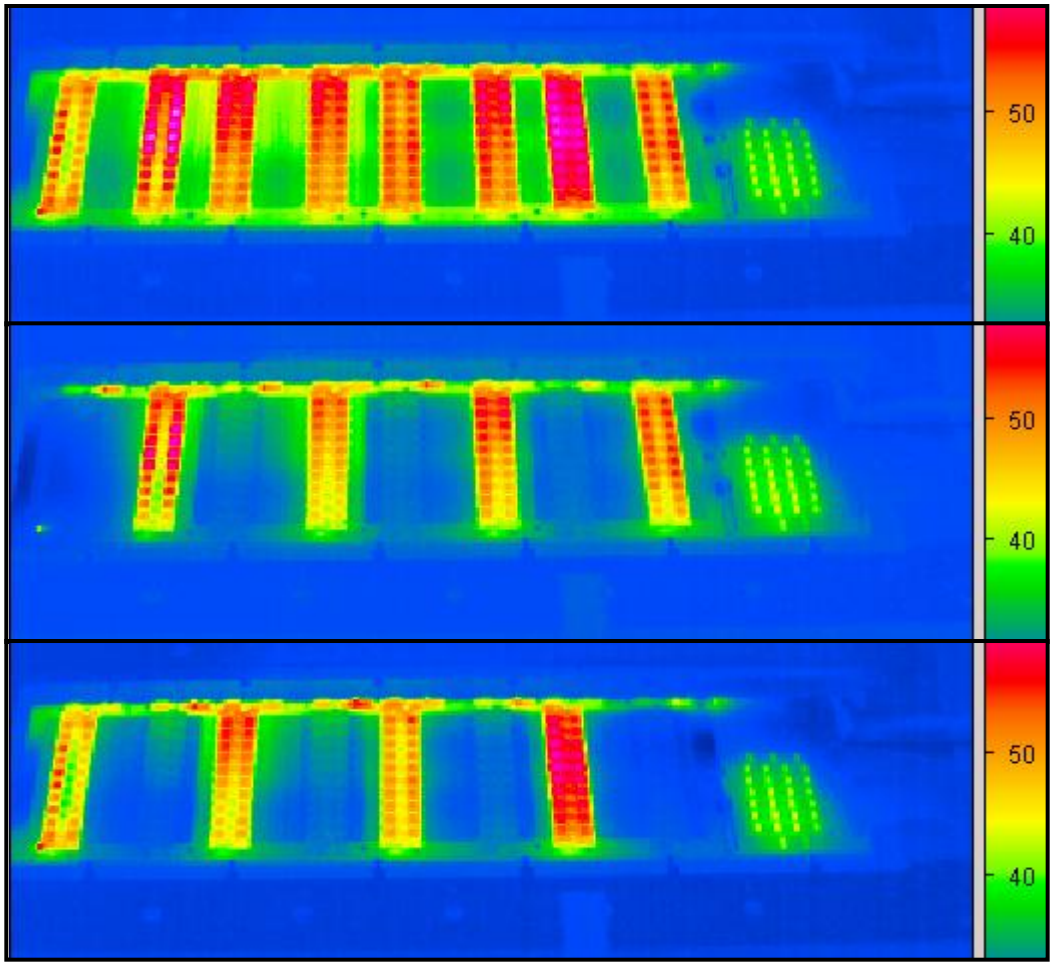
Stavelet ENC @2fC, JS CS II@5A

Run 1108 Scan 3

After Trimming, reading *all* hybrids simultaneously, column 1 strip order corrected.



Thermal images of stavelet in operation



All hybrids on

22.7V
5.09A

Slow control disables odd hybrids

12.7V
5.09A

Slow control disables even hybrids

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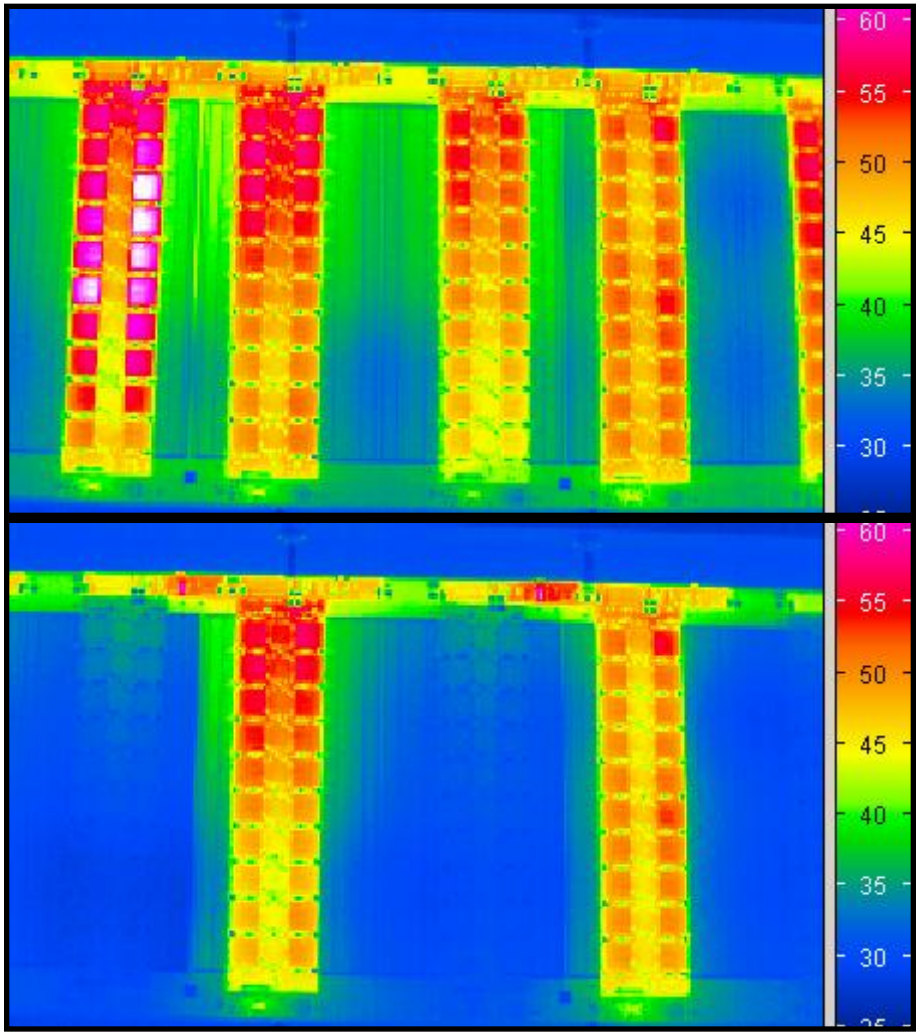
Thermal images of slow control bypass in operation



0.5 W

slow control bypass on: P = VI = 100mV * 5A = 0.5W

thermal images show slow control bypass working as expected

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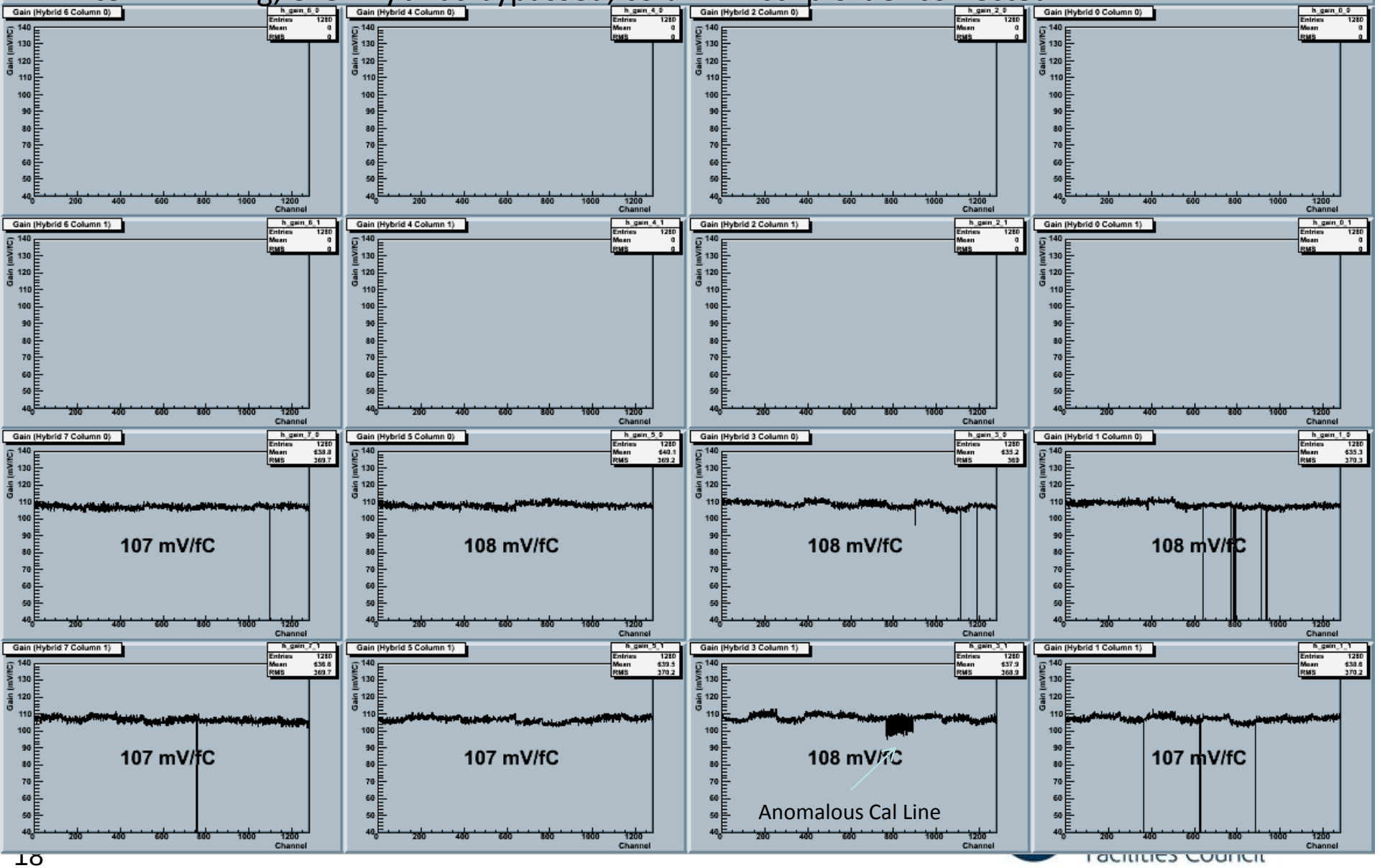
Stavelet GAIN @2fC, JS CS II@5A

Run 1113 Scan 3

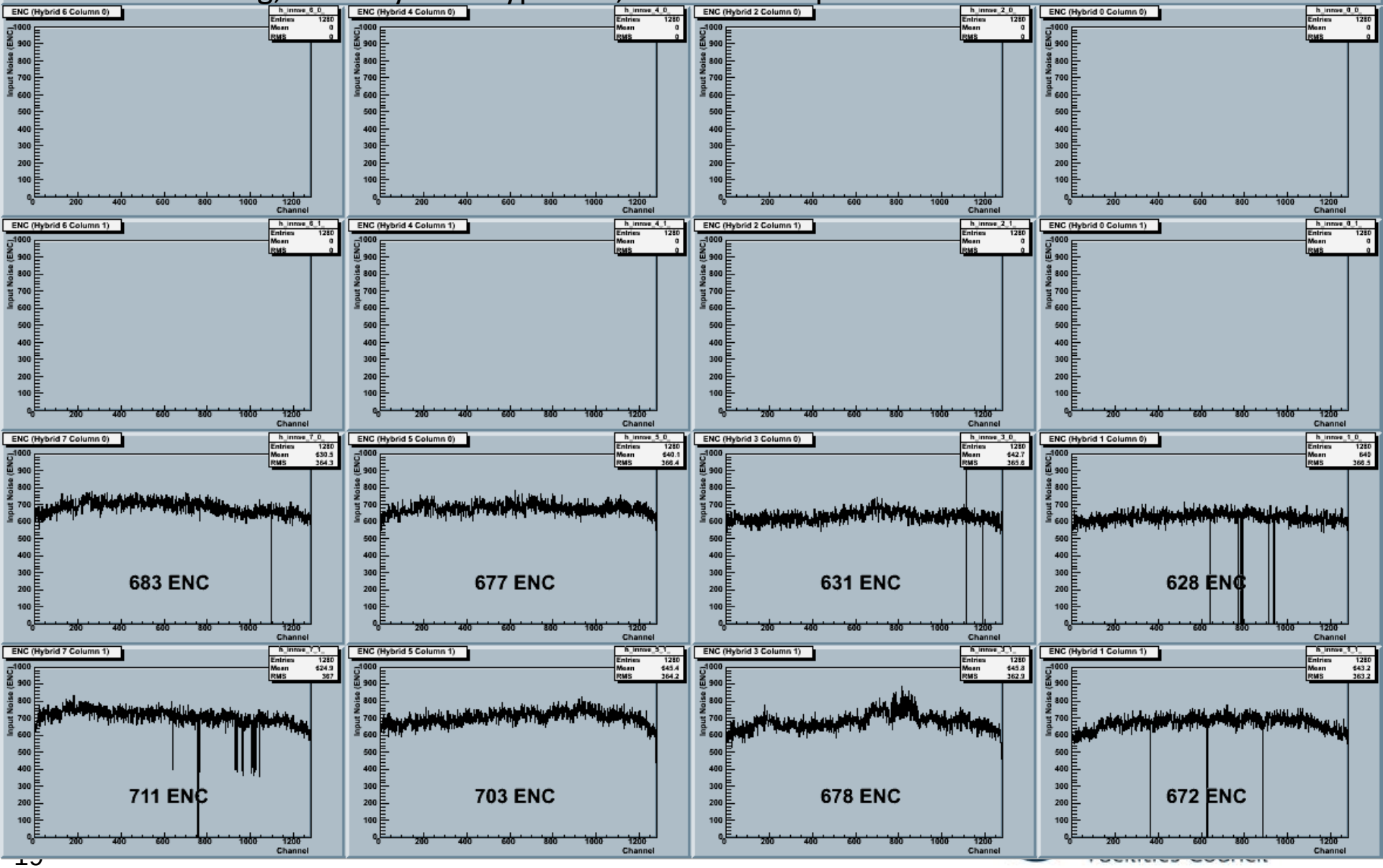
After Trimming, even hybrids bypassed, column 1 strip order corrected.



Stavelet ENC @2fC, JS CS II@5A

Run 1113 Scan 3

After Trimming, even hybrids bypassed, column 1 strip order corrected.



Summary and Next Steps

- Progress continues with Serial powering for the tracker Upgrade

- ABCn-25 chips contain custom SP components
- A protection system has been implemented using COTS components
- The protection system also implements slow control of powering
- A custom current source has been prototyped
- The first test stavelet has been built

- Stavelet working well so far, no excess noise. Modules can be turned on and off independently. Studies continue.
- Stavelets will allow refinement of architecture for a full SP stave prototype

- A modified stavelet is being designed (R.Wastie et al.) to allow DC-DC tests (with G.Blanchot, F.Faccio) and will be built asap

Spare slides

Power Requirements with Modern Process Technologies

					Power per 128 channel chip	per channel
In ATLAS SCT	**ABCD** **(0.8μm, biCMOS)**	Digital: Analogue:	4.0 volts 3.5 volts	35 mA per chip (actual) 74 mA per chip (actual)	=> 4.0 x 35 + 3.5 x 74 = 399 mW	**3.1 mW**
Present Prototype	**ABCN25** **(0.25μm CMOS)**	Digital: Analogue:	2.5 volts 2.2 volts	95 mA per chip (preliminary) 27 mA per chip (preliminary)	=> 2.5 x 95 + 2.2 x 27 = 300 mW	**2.3 mW**
Proposed	**ABCN13** **(0.13μm CMOS)**	Digital: Analogue:	0.9 volts 1.2 volts	**51 mA per chip (estimate) **16 mA per chip (estimate)	=> 0.9 x 51 + 1.2 x 16 = 65 mW	**0.5 mW**

ABCN25: Vdig > Vana Idig >> Iana

If we generate Vana from Vdig using LR:

- 27mA * 0.3V = 8.1mW per chip
- 3% of chip power

ABCN13: Vana > Vdig Idig >> Iana

If we generate Vdig from Vana using LR:

- 95mA * 0.3V = 28.5mW per chip
- **44% of chip power**
- Can we do better than this? *Of course…*

** Power Estimates for an ABCN in 130nm Technology, Mitch Newcomer, Atlas Tracking Upgrade workshop, NIKHEF, November 2008
http://indico.cern.ch/getFile.py/access?contribId=16&sessionId=8&resId=0&materialId=slides&confId=32084

Power Efficiency Comparison of Different Options

Realistic values for final system assumed below

Efficiency = power to readout chips/total power

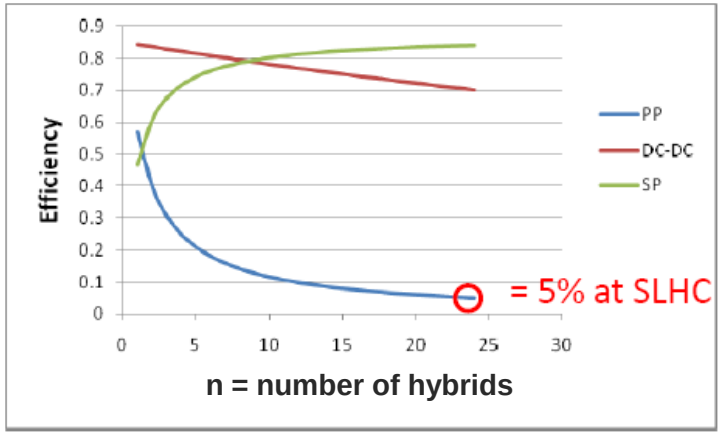
I = ABCN-13 hybrid current = 1.5A
V=ABCN-13 hybrid voltage = 1V
m=Vin/Vout for DC-DC = 10
n = number of modules on stave
$\varepsilon = P_{out}/P_{in}-1$ = 0.15
$\delta = I_{shunt}/I$ = 0.15
R = cable resistance = .5 Ω

$$\text{PP Eff} = \frac{nIV}{nIV+(nI)^2R}$$

$$\text{DC-DC Eff} = \frac{nIV}{nIV/(1-\varepsilon)+(nI/m(1-\varepsilon))^2R}$$

$$\text{SP Eff} = \frac{nIV}{nIV/(1+\delta)+(I/(1+\delta))^2R}$$

- Usual parallel powering not practical at SLHC
- SP improves with number of modules in chain (equivalently number on stave)
- DC-DC efficiency decreases with number on stave.
- Both DC-DC and SP look practical however for the standpoint of efficiency



these numbers for ABCN-13, i.e. next ASIC generation

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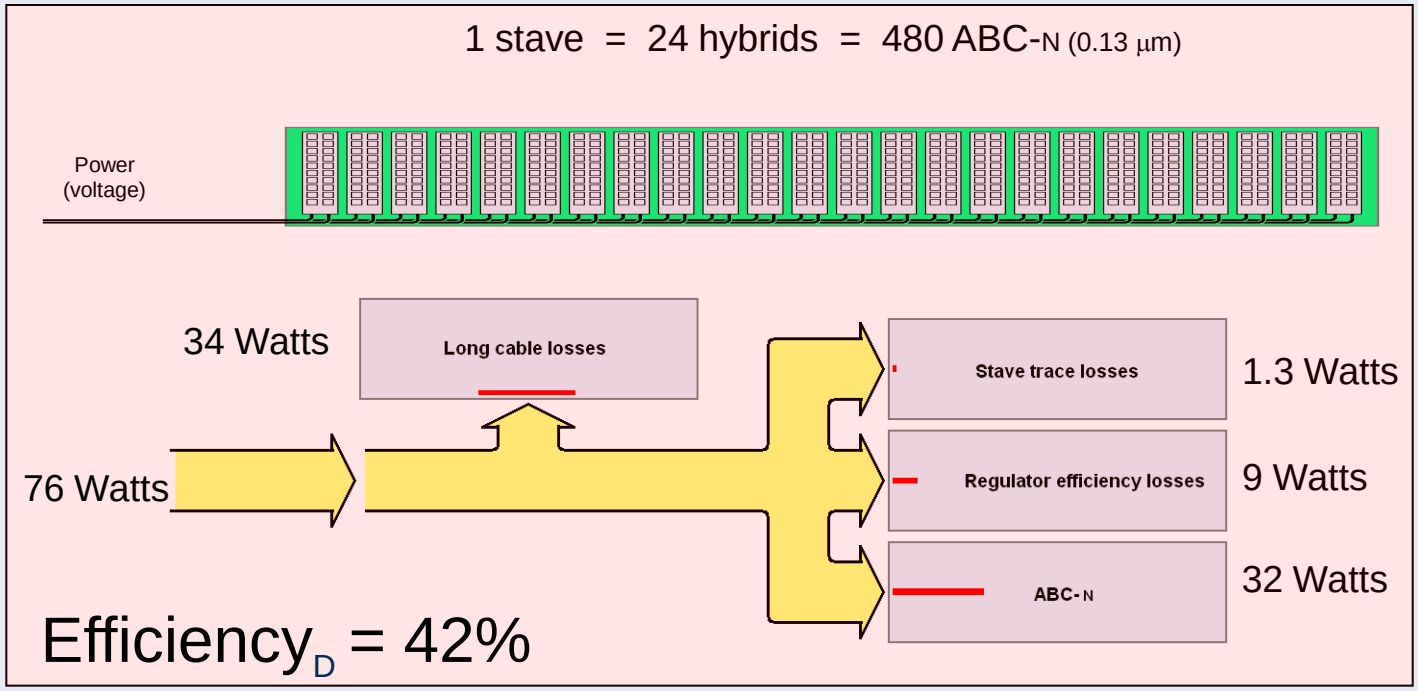
Detector power efficiency

Two-stage DC-DC powering (78% hybrid efficiency)



Cables assumed to be 2 ohms total for each power line pair
Regulator power = (1/eff - 1) x ABC power
Stave supply current = (32 + 9)watts / 10volts = 4.1amps

Numbers rounded

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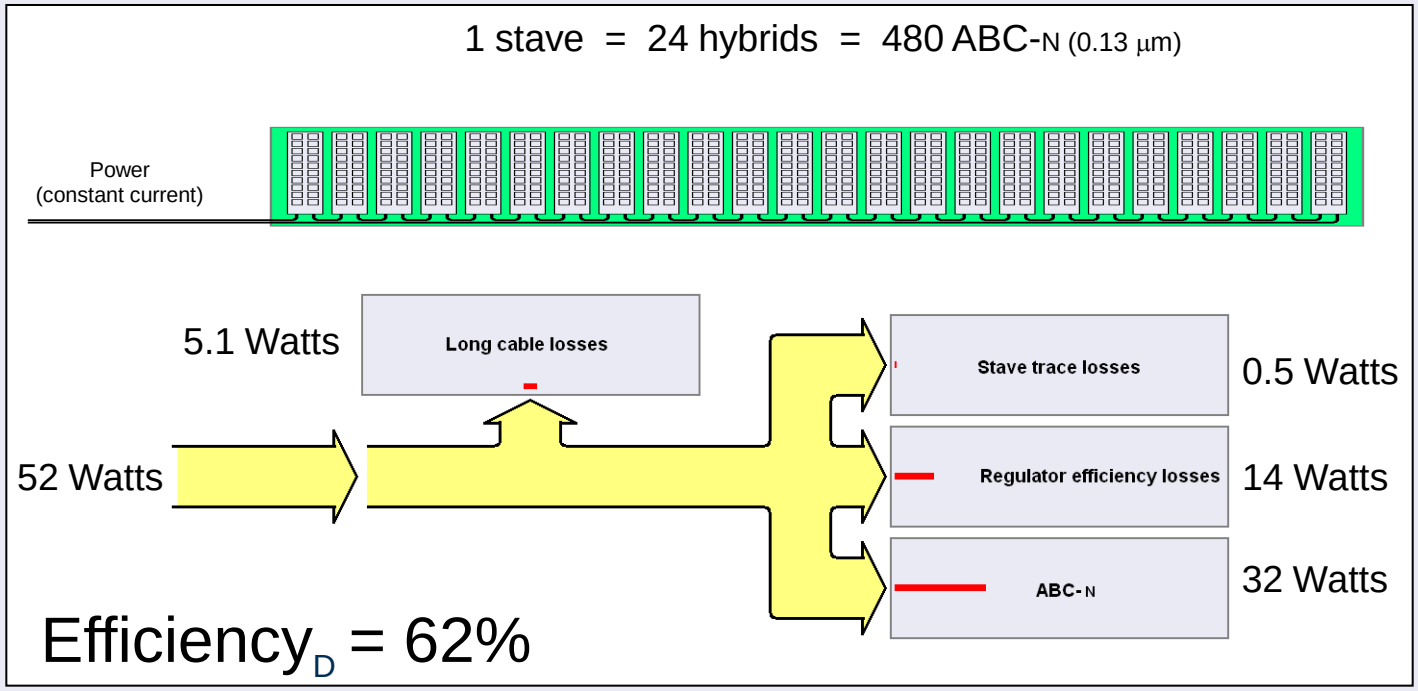
Detector power efficiency

Serial powering a stave, (no DC-DC version)



Cables assumed to be 2 ohms total for each power line pair
Regulator power = (1/eff$_H$ - 1) x ABC power
Stave supply current = (32 + 14)watts / (1.2volts x 24) = 1.6amps

Numbers rounded

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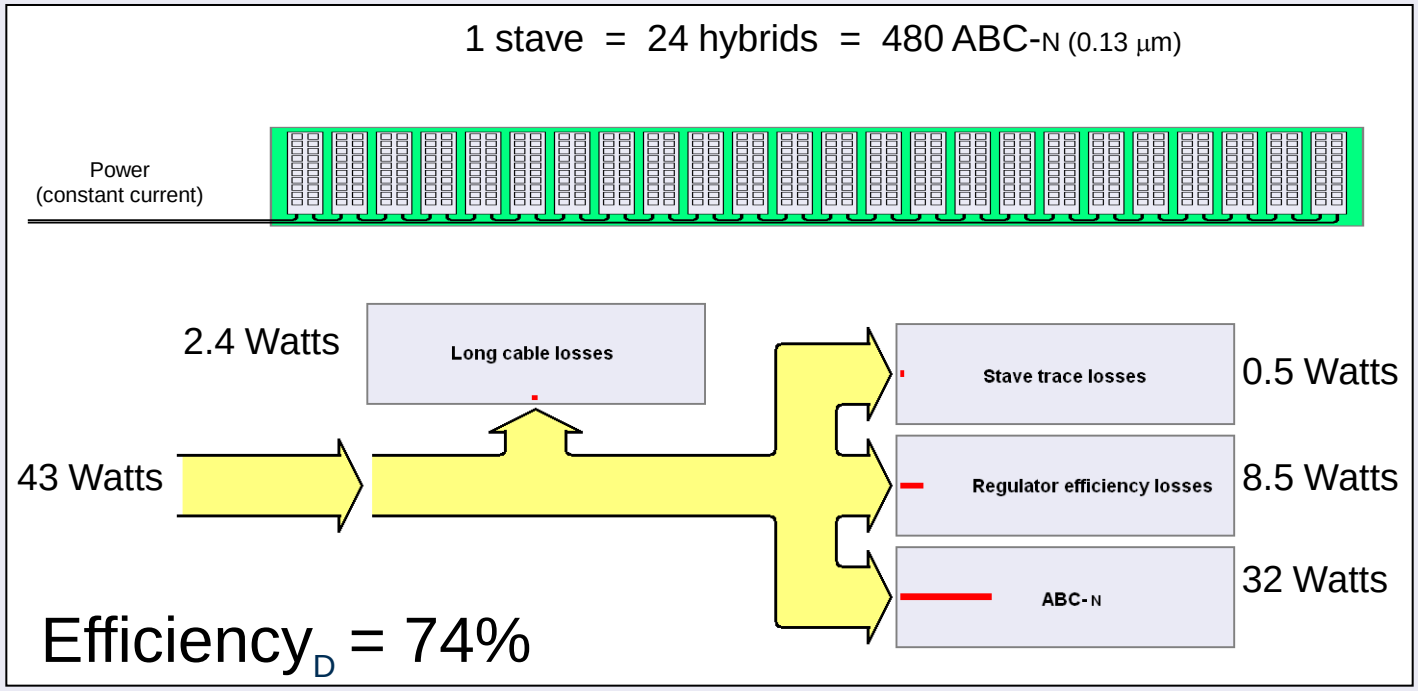
Detector power efficiency

Serial powering a stave, (higher voltage, with DC-DC version)



Cables assumed to be 2 ohms total for each power line pair
Regulator power = (1/eff$_H$ - 1) x ABC power
Stave supply current = (32 + 8.5)watts / (1.6volts x 24) = 1.1amps

Numbers rounded

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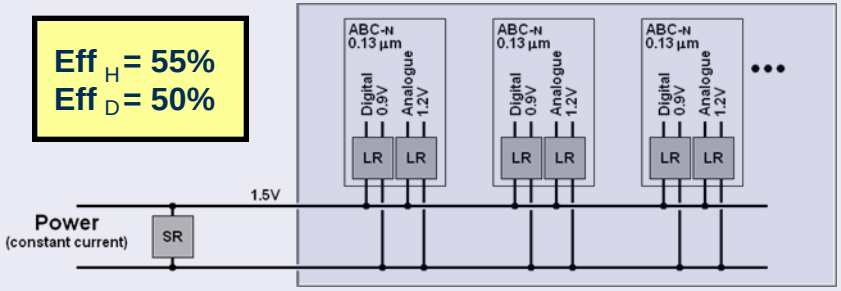
Two possible future SP implementations

Lowest Noise:

SP with on-chip Linear Regulators for both Analogue and Digital

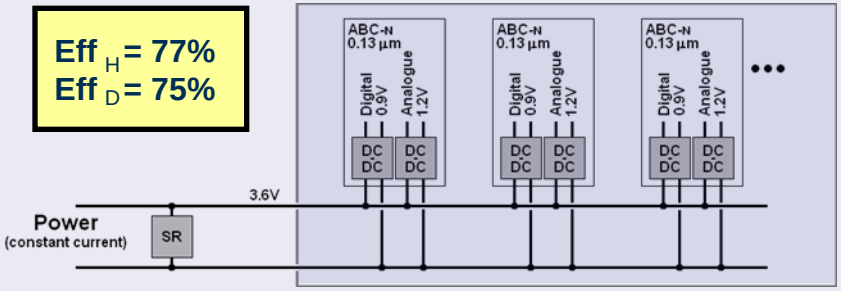
Eff $_H$ = 55%
Eff $_D$ = 50%



Highest Efficiency:

SP with on-chip DC-DC conversion using switched capacitors

Eff $_H$ = 77%
Eff $_D$ = 75%



$$\text{Efficiency}_H = \frac{\text{power consumed by ABCN}}{\text{power delivered to hybrid}}$$

$$\text{Efficiency}_D = \frac{\text{power consumed by ABCN}}{\text{power delivered by power supply}}$$

ABCN demand power is dependent on task. This will normally mean a shunt regulator will dissipate some power to maintain voltage under all conditions.

Some assumptions: Cable resistance 2 ohms for each line pair, SR = 85%, low current DC-DC = 90%, high current DC-DC = 85%
Bus cable traces 7.5mm wide, 18 micron Cu
chip power is that projected for 130nm ABCn

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The SPI chip – a serial power test bed

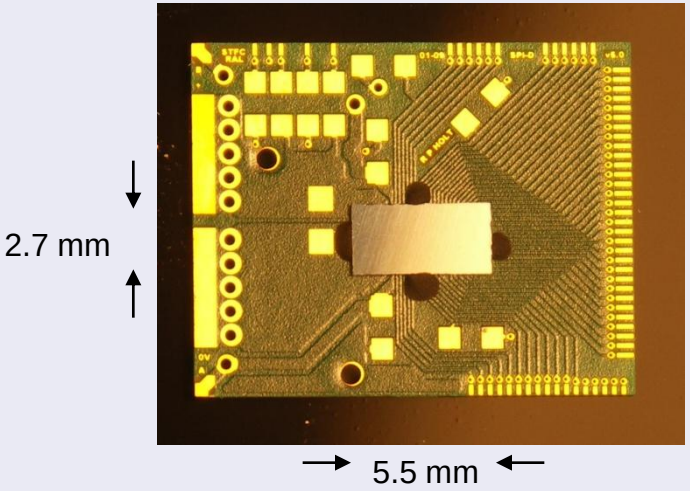
SPi (Serial Power Interface):

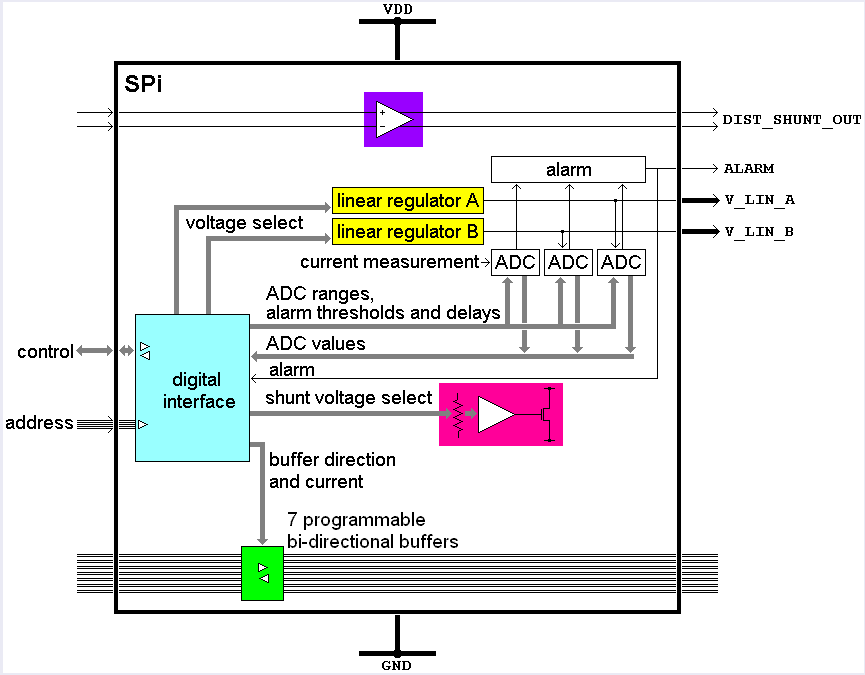
- Shunt regulator schemes
- Data communication
- Power management
- Monitoring/alarms

Designed by

Marcel Trimpl (FNL)

Mitch Newcomer (U Penn)





- flip chip, bump bonded
- 144 pads (68 I/O, 76 power)
- Sub-set used for each application

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Serial Powering system design

Current Source ver.2 specifications:

Input Voltage	90 - 264 VAC
Input Frequency	47 - 63 Hz
Input Power	800 W (max)
Output Current range	0 – 6 A
Output Current Setting Resolution	2 mA
Output Current Settling Time	< 2 ms
Voltage Compliance	0 – 80 V
Voltage Resolution	25 mV
Output Current Ripple (P_k-P_k)	10 mA (estimated max)
Control	Manual / Remote(USB)
Mechanical Dimensions (W x D x H)	305 x 280 x 133 mm

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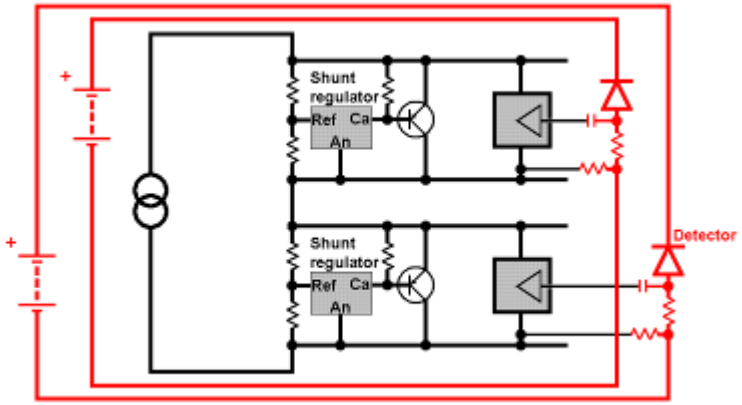
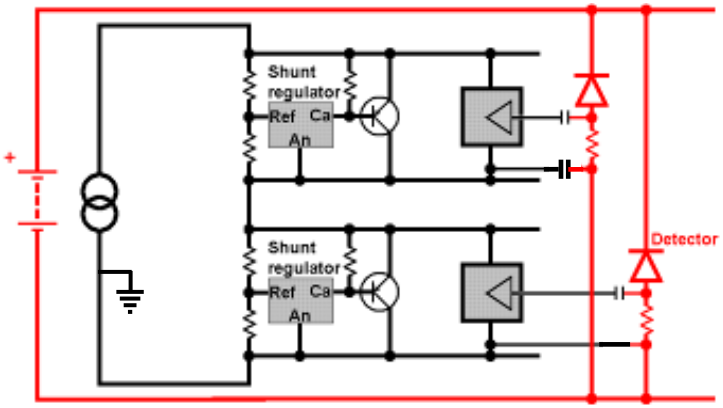
Serial Powering and HV



Standard HV powering: one HV per hybrid



Alternative HV powering: one HV supply per 2 hybrids

- Serial Powering is compatible with the use of a single HV supply for several modules
- Each sensor is dynamically connected to current source ground through output impedances of the chain of shunt regulators
- Low shunt output impedance is crucial to achieve good ‘grounding’ and reduce noise

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AC coupled data transmission - prototype bus tape

Whether we use SP or not, need to minimize number of signal traces in stave => multi-drop

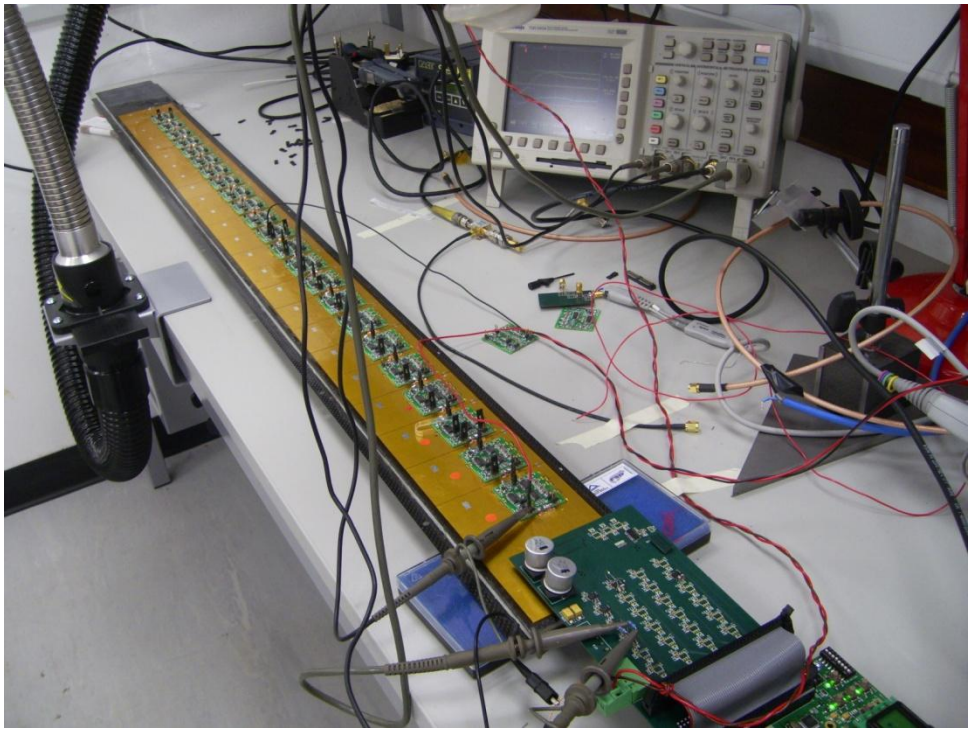
Test stave at Oxford

Cu/kapton + Al screen layer

Send “TTC” data from FPGA → 24 dummy hybrids with receiver/drivers

Loopback data on dummy hybrids ➔FPGA ➔ BERT.

Measure BERT for balanced and unbalanced data, parallel and serial powering



Balanced code works fine. M-LVDS + Serial powering + balanced code ok, ie no errors found in 3 locations tested (3 ,12 and 24).

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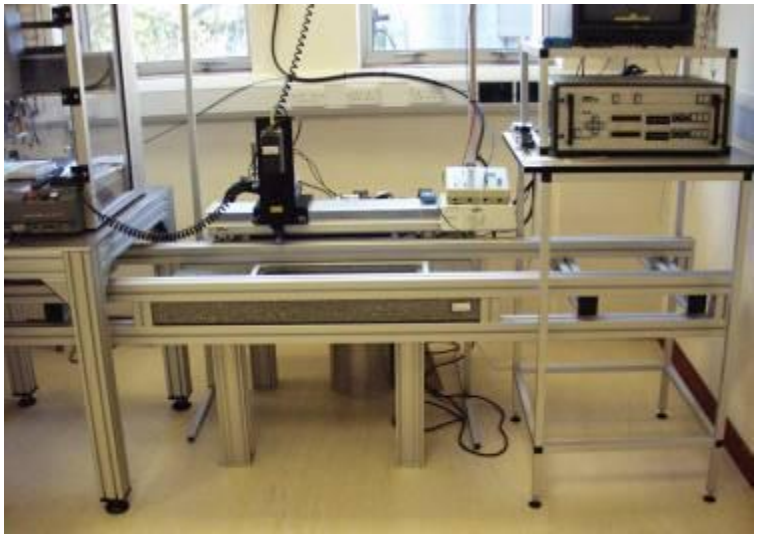
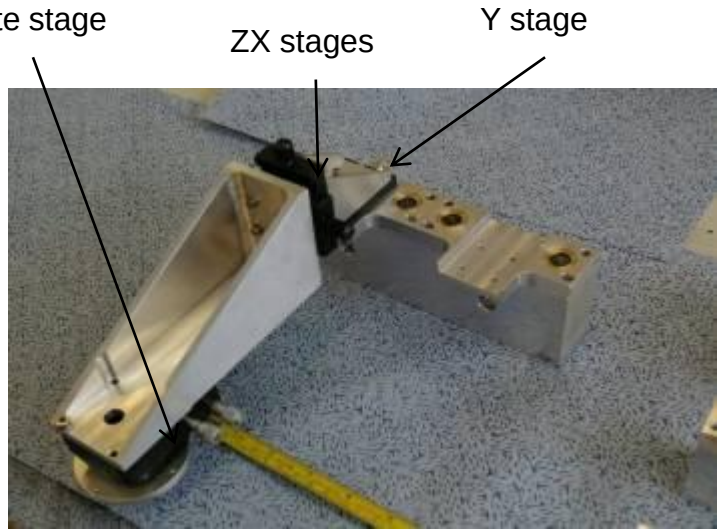
Stavelet construction at RAL

Module placement area



Module placement arm



Glue pattern trials
(left - on test board , right – on test bus cable)

Stavelet test box

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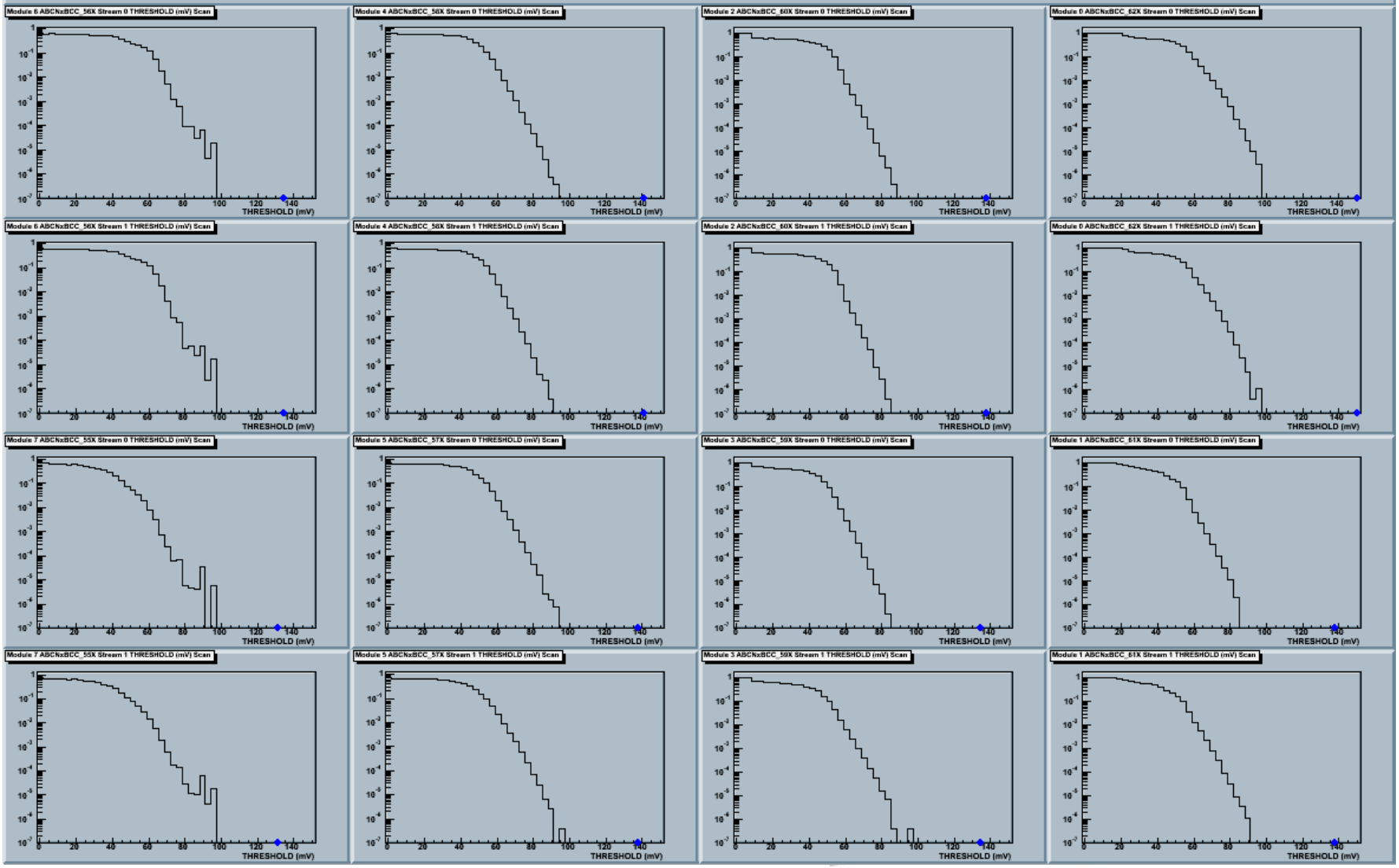
Run 1108 Scan 6 (log)



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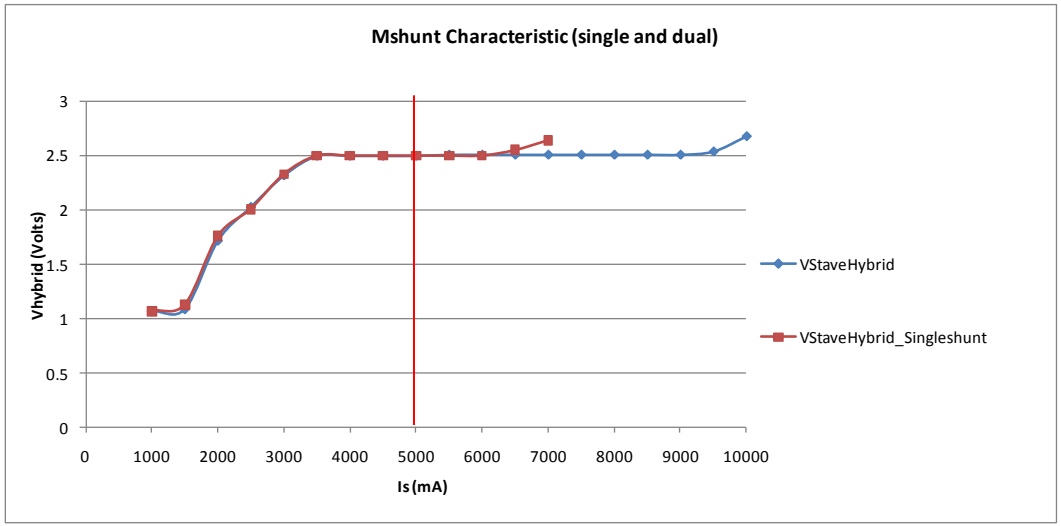
Hybrid powering

Hybrids are designed for two powering schemes:

1. Parallel power, which could be provided by DCDC converters

2. Shunt regulation, using the distributed shunt regulators integrated within the ABCN-25s
   - Required for serial powering – Mshunt is the default scheme



Mshunt characteristic for single and dual shunts enabled per ABCN-25 on a 20 ASIC hybrid
(expect max. Hybrid shunted current to be ≤5A)

Single Shunt transistor enabled per ABCN-25 (20 x shunt transistors)
Shunt regulates Vhybrid to 2.5V at I_s>3.5A and diverges at I_s<6.5A (*cf* I_{hybrid} +I_{smax} (3.6 + (20 x 0.14))) = 6.4A

Dual Shunt transistors enabled per ABCN-25 (40 x shunt transistors)
Shunt regulates Vhybrid to 2.5V at I_s>3.5A and diverges at I<9.5A (*cf* I_{hybrid} +I_{smax} (3.6 + (40 x 0.14))) = 9.2A

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