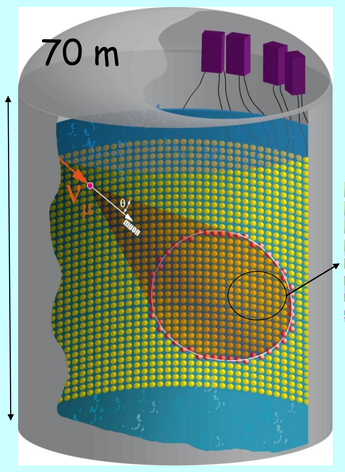
Topical Workshop on Electronics for Particle Physics 2010 — Aachen, Germany, 20-24 September 2010

A R&D on a triggerless acquisition for next generation neutrino experiments

http://pmm2.in2p3.fr

E. Wanlin on behalf of the PMm² collaboration



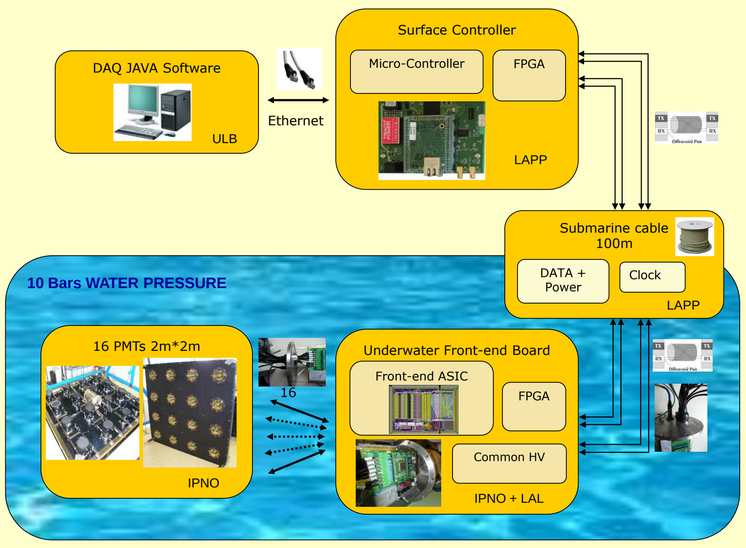
Megaton scale water Cerenkov such as MEMPHYS at Fréjus, France (10 to 20 times Super Kamiokande) might be made of several tanks with the order of 80,000 photomultiplier tubes (PMTs) each.

The next generation of megaton scale water tanks implies very large surfaces of photodetection and a large volume of data. PMm² is a funded R&D project to implement and propose a demonstrator. The main features are:

- Replace large 20" PMTs by 12"
- Modular design of 16 PMTs arrays
- Underwater front-end electronics
- Surface controller
- Triggerless data acquisition
- Demonstrator with 16 8" PMTs

Global Architecture and Constraints

- Modular design of 16 PMTs arrays, 2 m x 2 m
- Low cost
- Single high voltage power supply for 16 PMTs
- Gain compensation on front-end electronics
- Triggerless
- 5 kHz noise pulses rate of PMTs
- 10-bar pressure/water resistance
- PMTs data transferred continuously to the surface controller
- Coincidence and data analysis off line

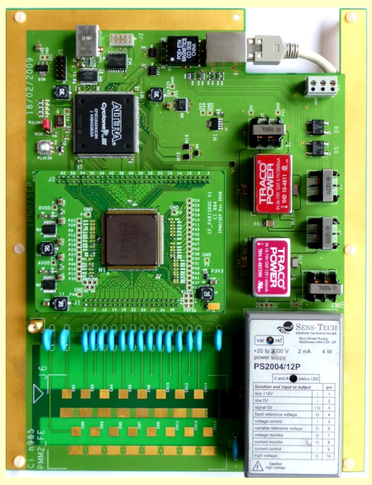


Global synoptic of PMm²

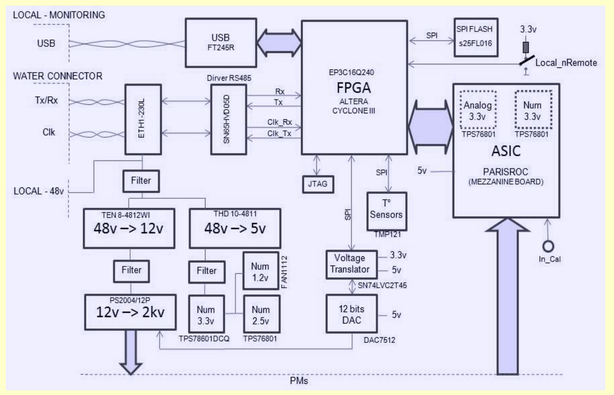
Underwater Front-End

- Analog front-end ASIC PARISROC (see below)
- Altera Cyclone3 FPGA for slow-control and readout of the ASIC and data transmission from/towards the surface controller (mean 5 Mbps)
- Single tunable (up to 2 kV) High Voltage via a 12-bit DAC
- Surface monitoring of temperature
- USB interface for standalone debugging
- DC/DC converters for 48 V / 12 V, 48 V / 5 V and linear regulators
- PCB (8 layers, class 5) design meets rules of isolation, filtering, cooling and EMC
- Watertight box, connectors and PMTs' bases potting tested up to 13 bars

Submarine board into watertight box



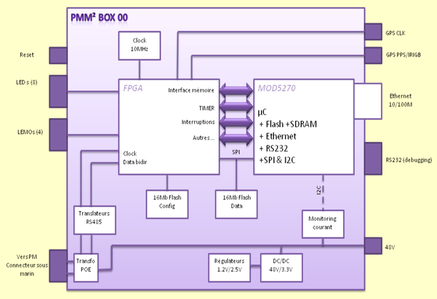
Submarine board



Synoptic of the submarine board

Surface Controller, 100m Cable

- Micro-Controller for connection to Ethernet network
- FPGA for synchronization and dialogue with submarine board
- 100m cable, cat.5 class D, with 2 differential pairs:
  - 10 MHz GPS clock for synchronization
  - dataflow + Power Over Ethernet 48 V / 30 W
- Dedicated serial Manchester protocol (RS485 levels) 5 Mbps
- Underwater harness: industrial electrical and pressure tests

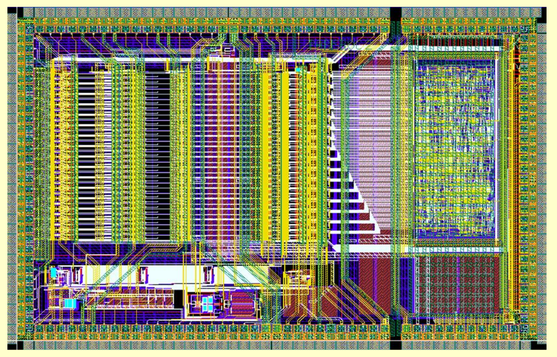


Synoptic of the surface controller

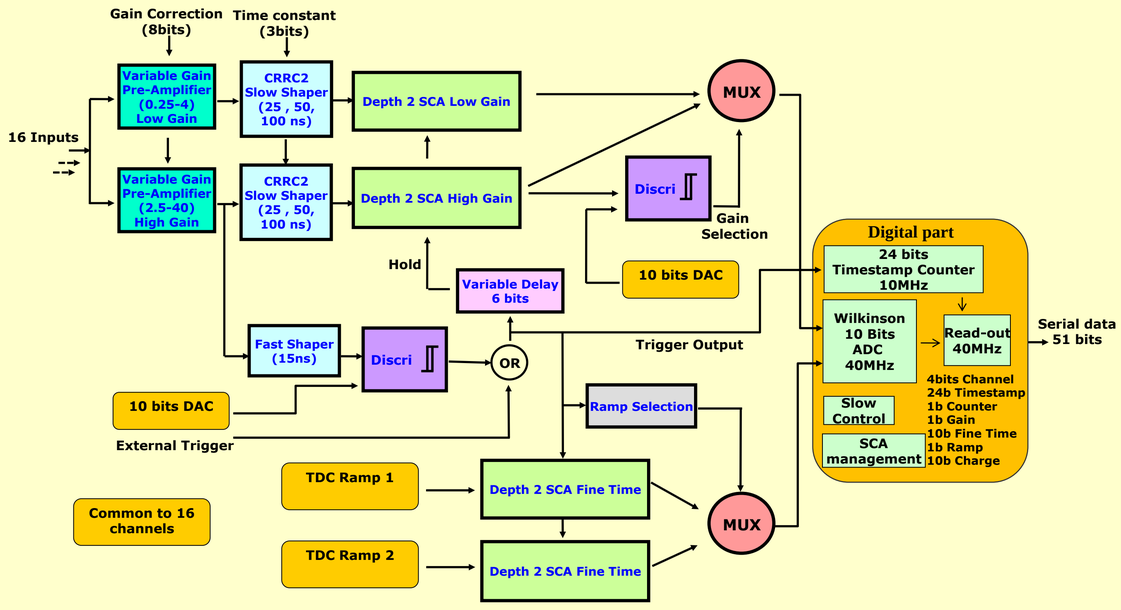
Surface board and underwater cables

Front-End ASIC (PARISROC)

- AMS SiGe 0.35 µm
- 16 independent channels
- Independent gain adjustment by channel
- Charge and time digitization
- Charge: 0 to 300x10⁶ electrons
- efficiency from 10⁶ electrons input charge
- Time resolution 425 ps RMS
- 24-bit timestamp counter @ 10 MHz
- Virtual 12-bit ADC @ 40 MHz
  (10-bit Wilkinson ADC + 2 gains with automatic selection)
- Serial readout @ 40 MHz
- Max conversion + readout time = 45 µs



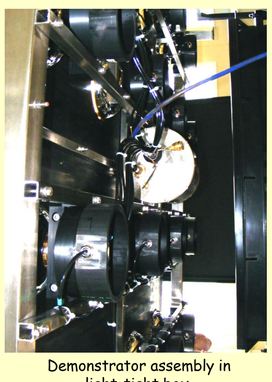
PARISROC Chip – 0.35 µm SiGe - 5 mm x 3.4 mm.



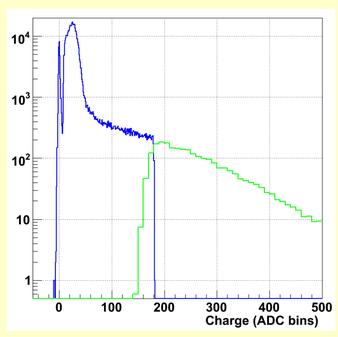
Synoptic of the PARISROC ASIC

16 8" PMTs Demonstrator: First Results

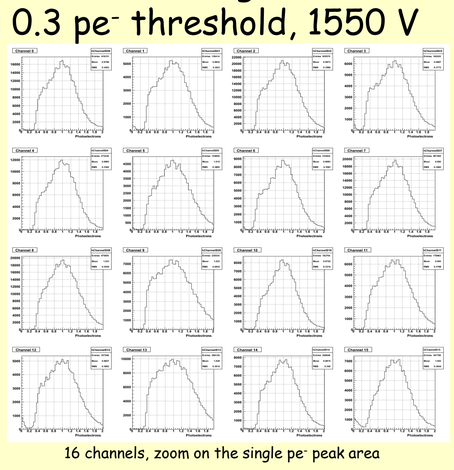
- Charge measurement of PMTs and gain compensation
- Ability of PARISROC to sustain the PMTs counting rate
- Single photoelectron response with 0.3 pe⁻ threshold, 1550 V



Demonstrator assembly in light-tight box



1 channel, noise histogram with pedestals subtracted



16 channels, zoom on the single pe⁻ peak area

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