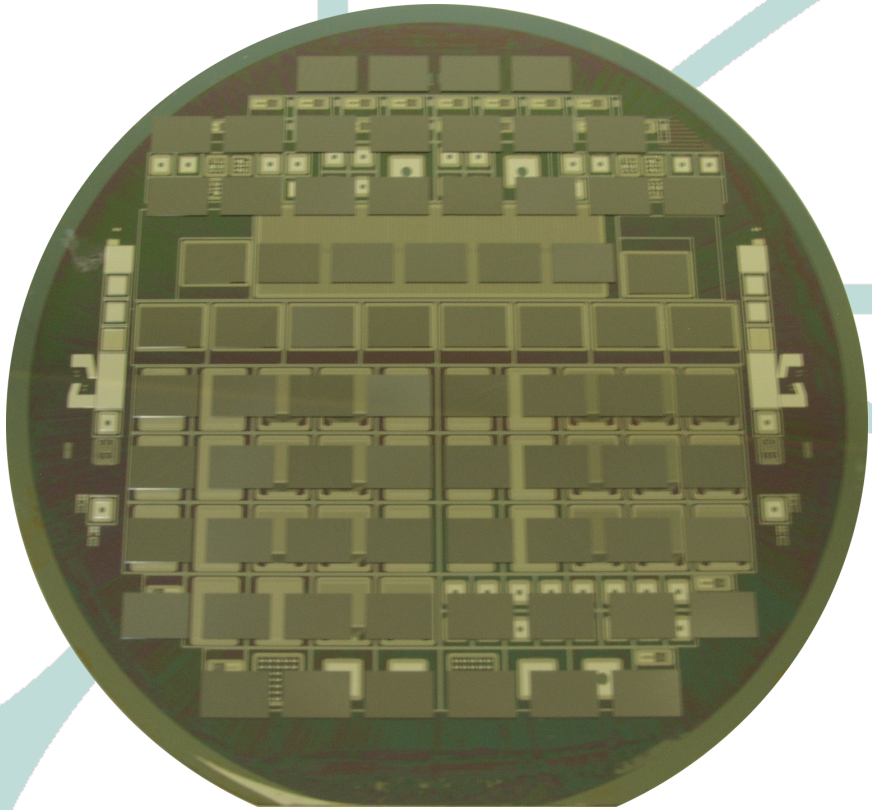
ICV-SLID interconnection technology for the ATLAS pixel upgrade at SLHC



L. Andricek, M. Beimforde, A. Macchiolo,
H.-G. Moser, R. Nisius, R.A. Richter, P. Weigell

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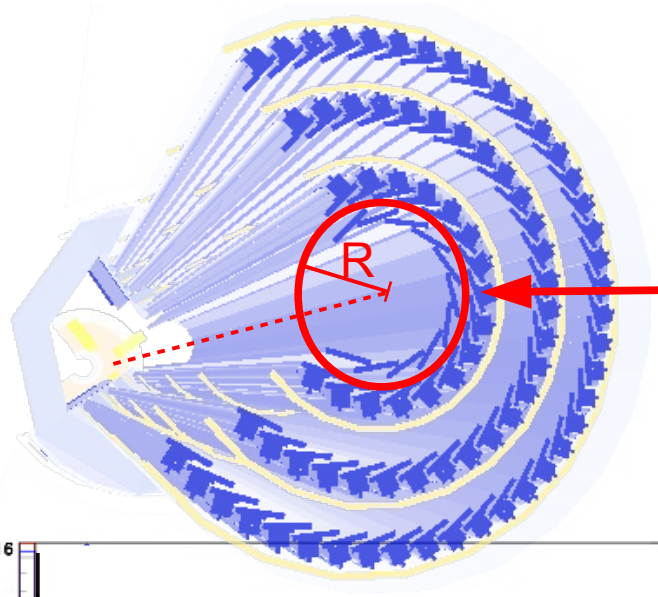
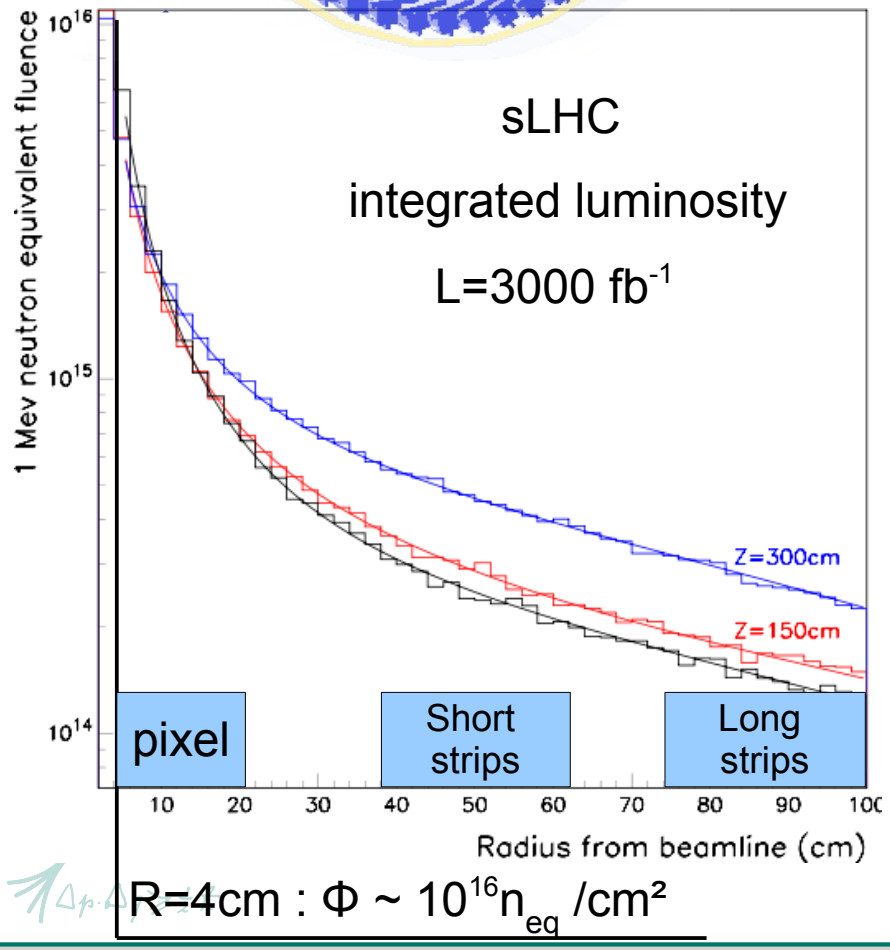
Overview

- Pixel detector needs for luminosity upgrades
- The MPP module concept
- Solid-Liquid InterDiffusion (SLID)
- Inter-Chip Vias (ICV)

Fraunhofer EMFT

ATLAS Pixel detector Upgrades





Phase 1 upgrade:

- Surpass LHC design luminosity by ~ 2016
- Insert new innermost pixel layer (b-Layer) **IBL** into the present one. R~3.3cm

Phase 2 upgrade (Super LHC):

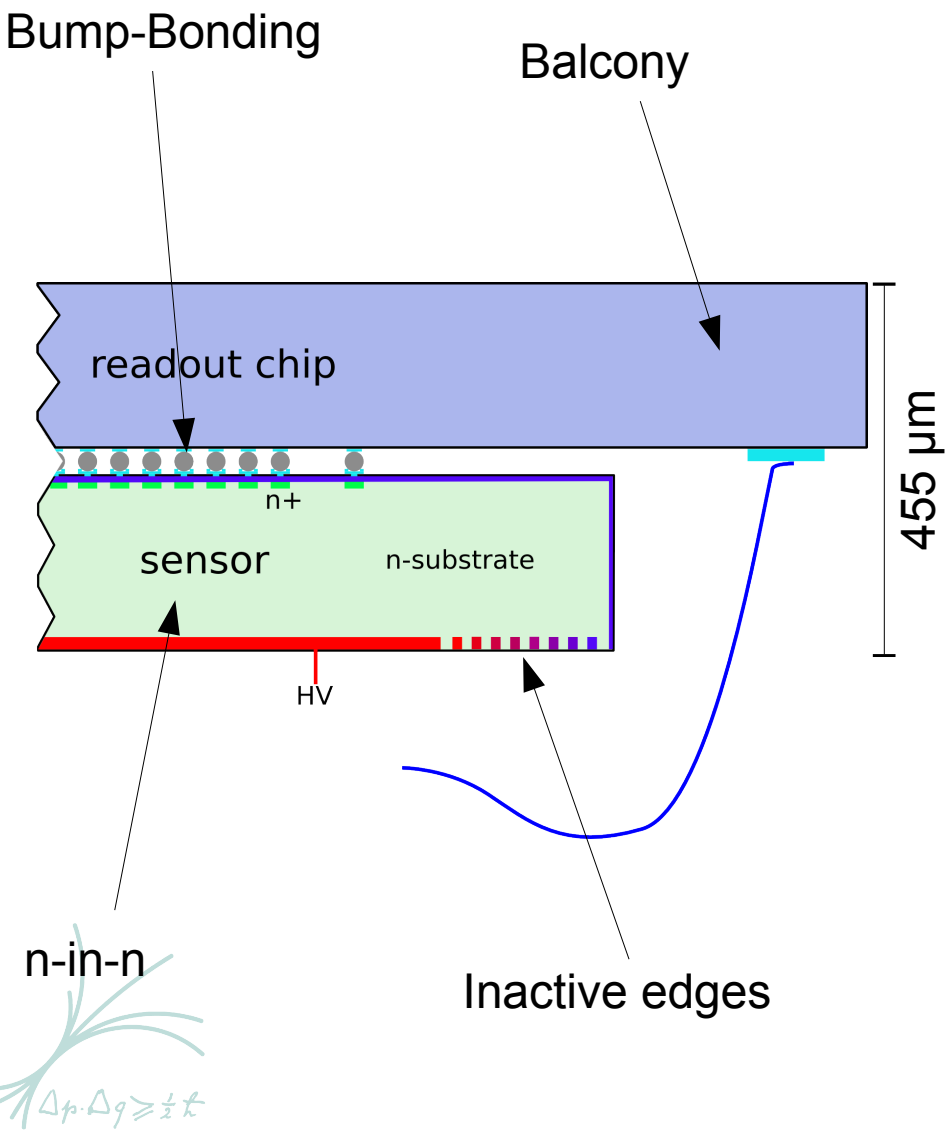
- Plan: (5 -10) x 10^{34}/cm^{2}s → (5 -10)-fold increase
- Completely new pixel detector is needed
- Pixel modules from 3.7cm < R < 20.9cm (current: 5.1cm < R < 12.2cm)
  - Very compact modules needed!
  - Cheap modules wanted!
  - Less multiple scattering (material) desired!

sLHC radiation environment:

- Integrated fluence: Φ~10^{16} n$_{eq}$ cm^{-2} (scaled to damage of 1 MeV neutrons) after 3000fb^{-1}
- Radiation damage esp. for inner pix. layers
  - Radiation hard modules needed!

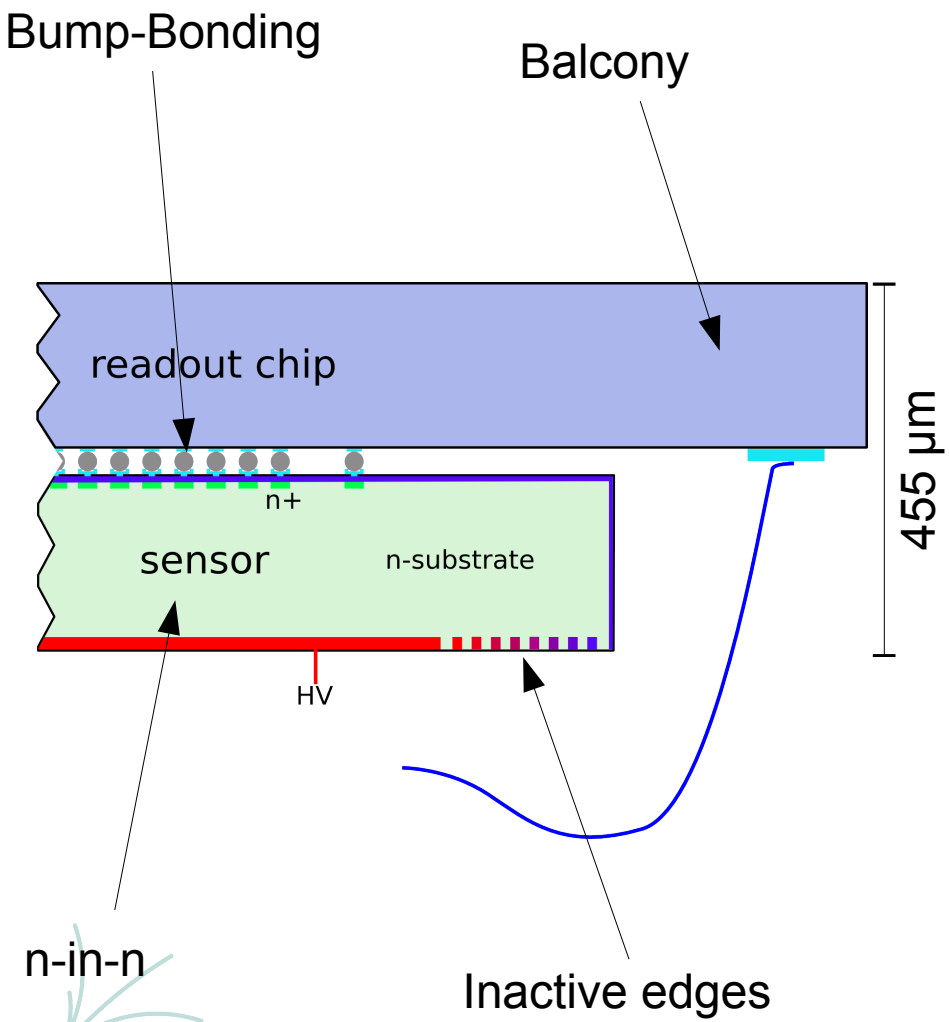
The MPP module concept

ATLAS standard

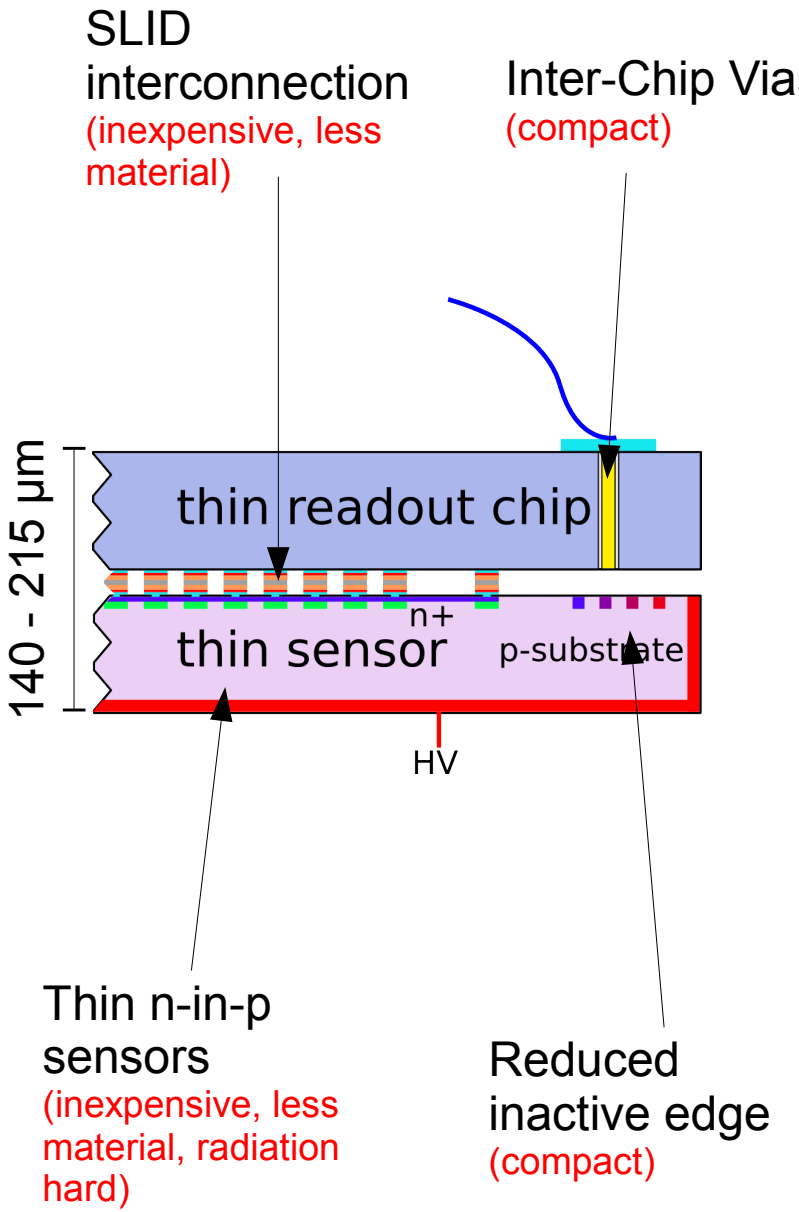


The MPP module concept

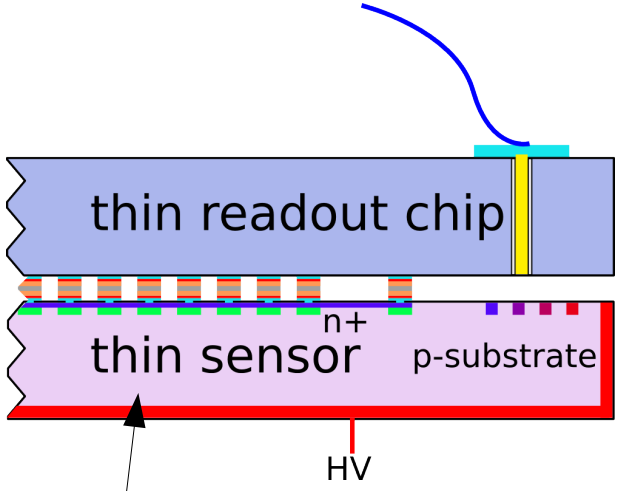
ATLAS standard



Novel MPP concept



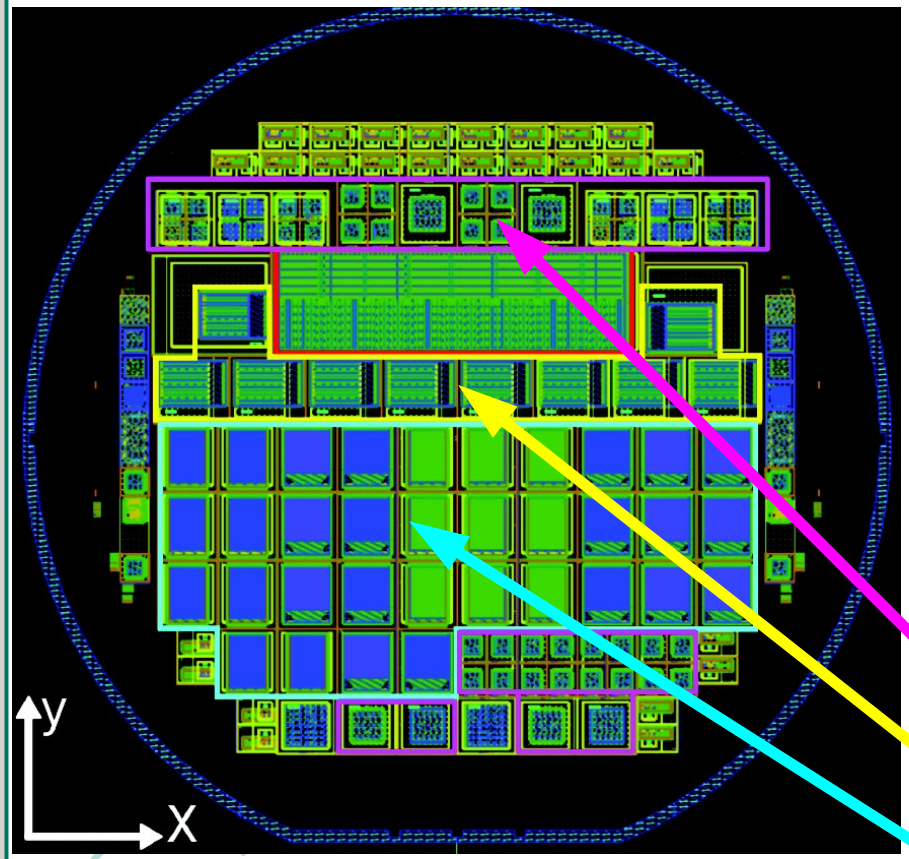
The MPP module concept



Thin n-in-p sensors
(inexpensive, reduced material, radiation hard)

Thin sensors

HLL + Industry:



Potential advantages of thin sensors:

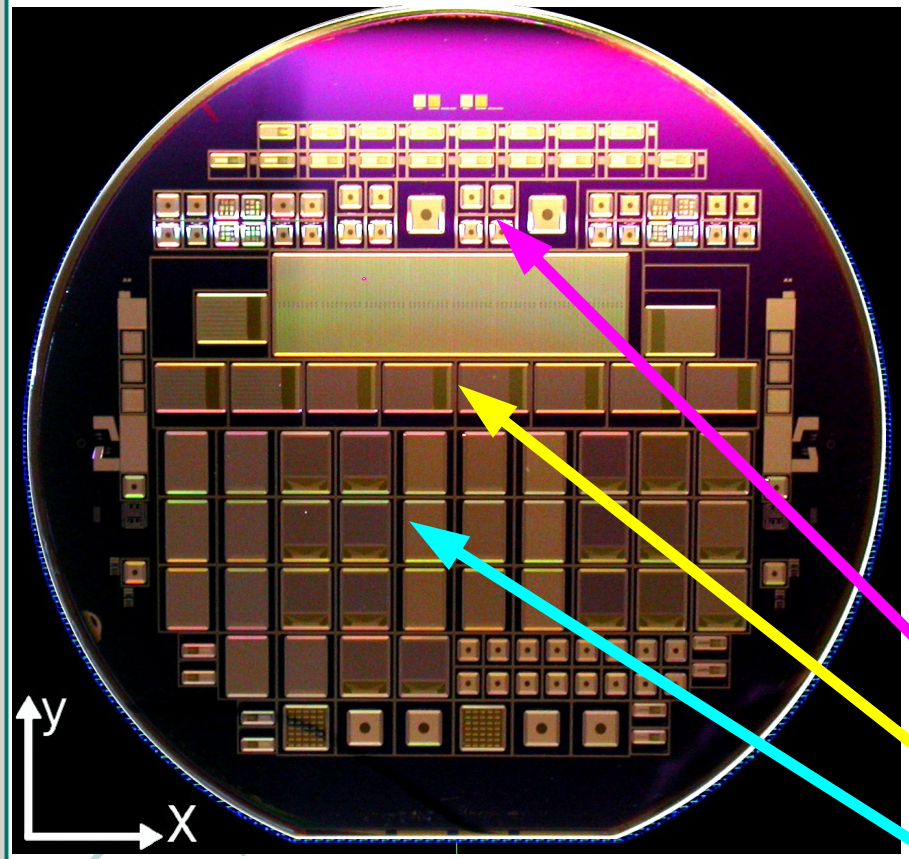
- Lower leakage currents: I ~ V
- Lower full depletion voltage: $U_{fd} \sim d^2$
- Higher electric field for same voltages:
  - De-trapping / avalanche multiplication
- Higher signals expected

First thin sensor production:

- 8 n-in-p wafers
- Active thicknesses: 75 µm and 150 µm
- Diodes: Si properties
- Pixel sensors: prototype modules
- Strip sensors: charge measurements

Thin sensors

HLL + Industry:



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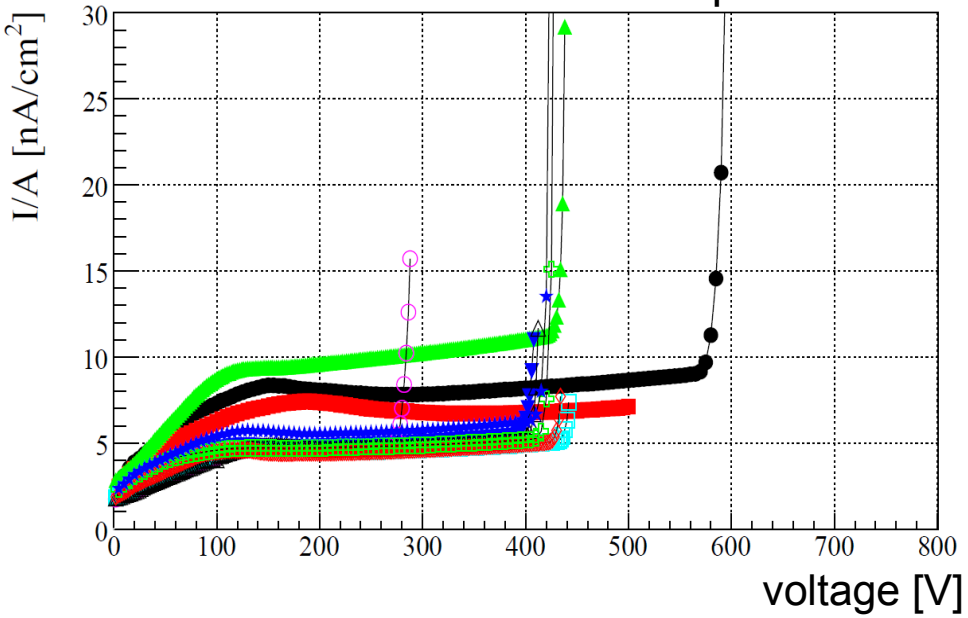
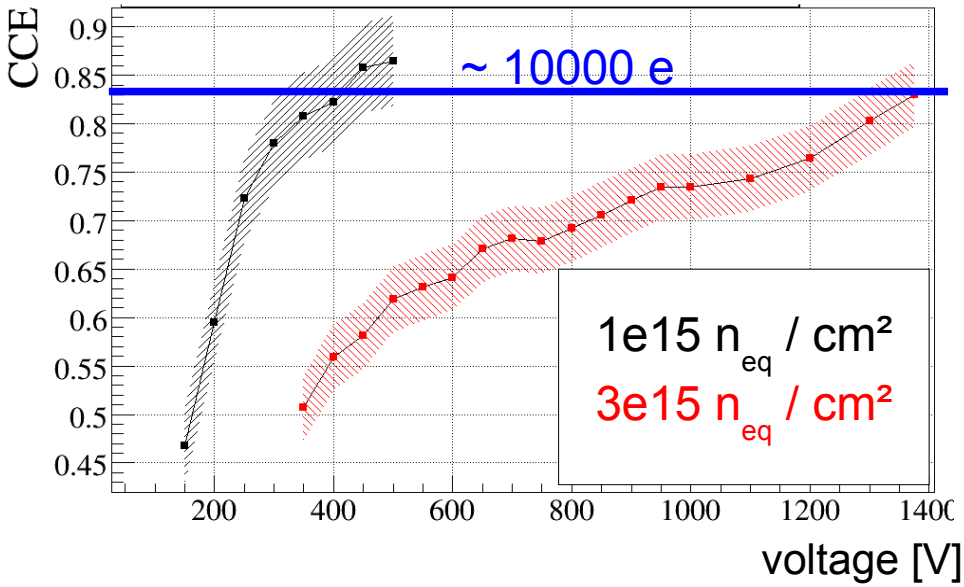
The MPP module concept

Pixel sensors: 75 & 150 µm



Strip sensors: 150 µm



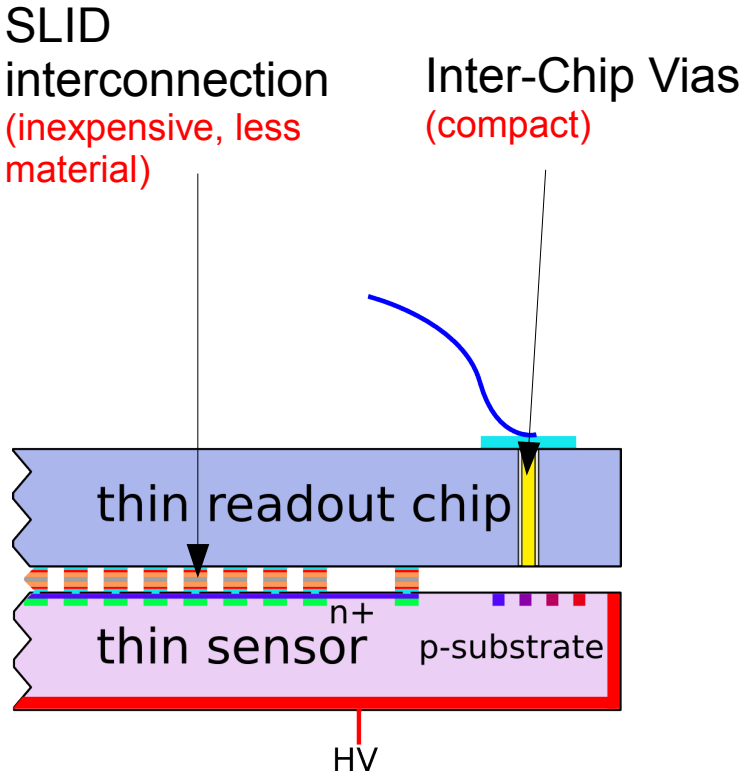
Sensor characterization:

- Low leakage currents
- High break-down voltages
  - $U_{bd} >> U_{fd}$
- High device yield (pixel sensors: > 98%)
- High charge collection efficiency after irradiation

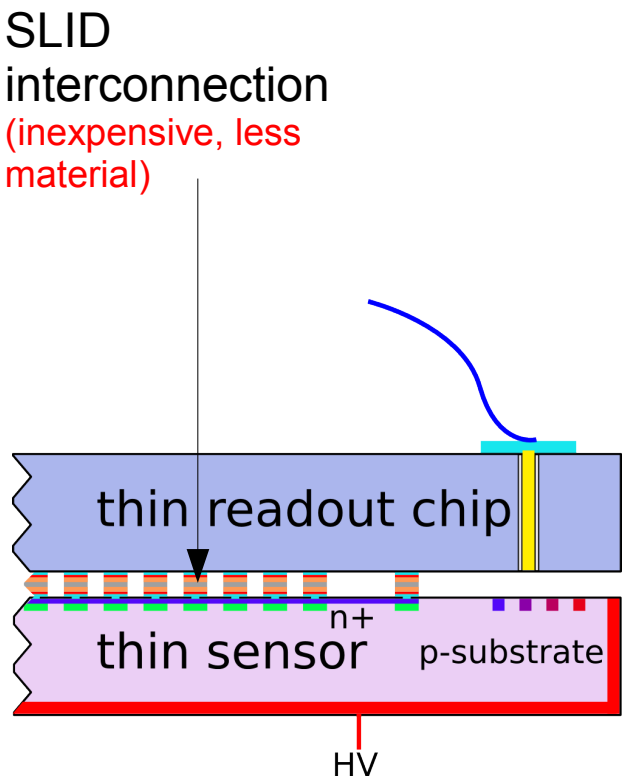
IBL sensor production:

- A second thin sensor production for the IBL is ongoing
- Includes mainly sensors compatible with the new ATLAS readout chip: FE-I4
- Results expected early 2011

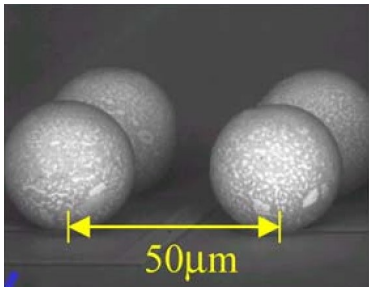
The MPP module concept



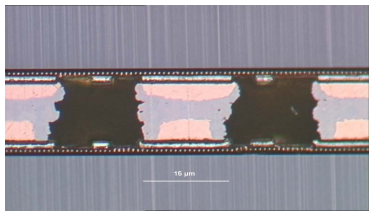
The MPP module concept



Solid-Liquid InterDiffusion



Fraunhofer EMFT



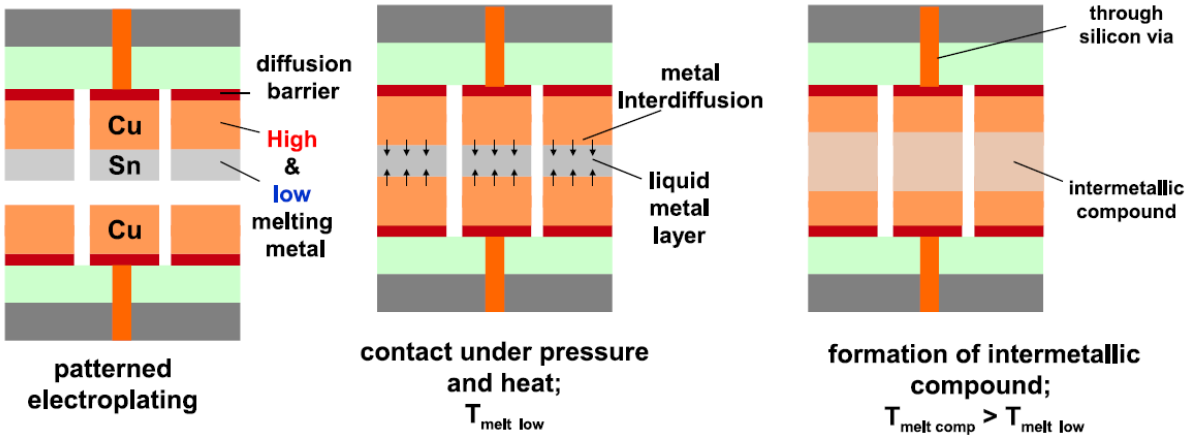
	Bump-bonding process	SLID process
1st step	Metallization and solder apply	Metallization and solder apply
2nd step	Reflow	
3rd step	Pick & place (flux)	Pick & place (no flux)
4th step	Soldering	Soldering

SLID overview:

- New interconnection technique between sensors and readout chips
- Possible alternative to bump-bonding
- Potentially cheaper
- Allows for finer and variable shape connection pads
- Needs high precision assemblies
- Many-layer stacking possible

Solid-Liquid InterDiffusion

Fraunhofer EMFT

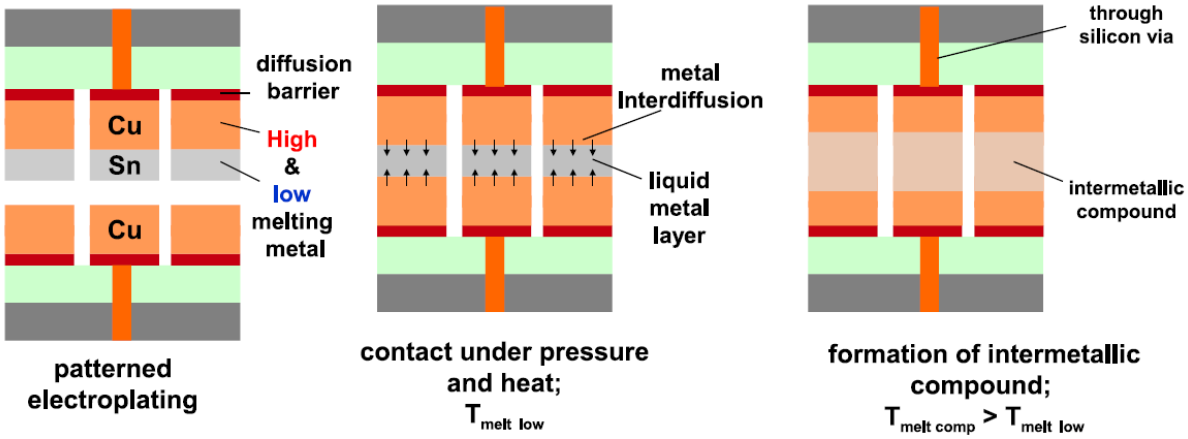


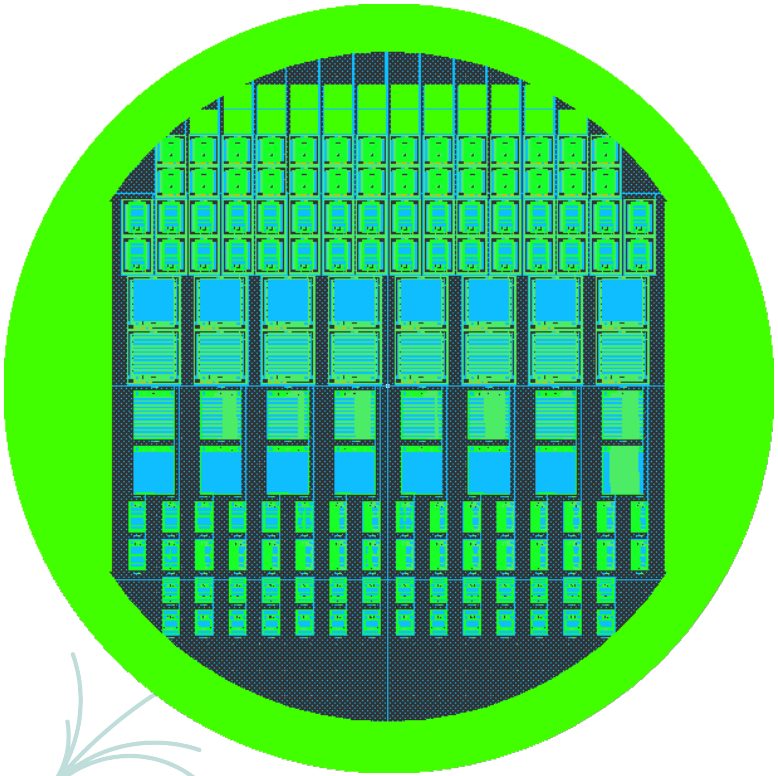
The SLID metallization:

- 5µm of Cu on sensor and chip side
- 3µm of Sn on sensor side
- Metal interdiffusion at ~ 300°C to form Cu_3Sn with a melting point of ~ 600°C

Solid-Liquid InterDiffusion

Fraunhofer EMFT





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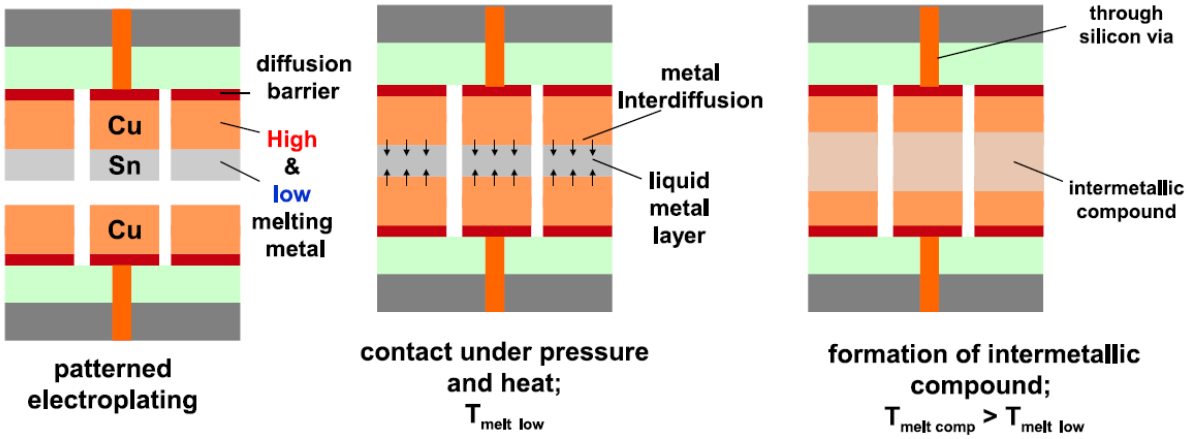
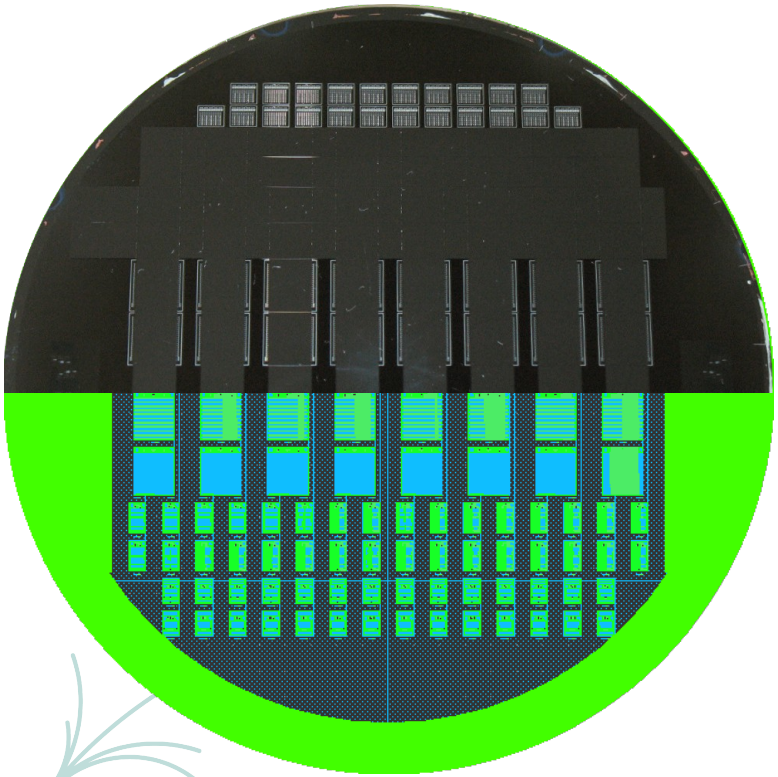
First SLID interconnections:

- 6-inch SLID wafer production
- Daisy chains with different geometries
  - Many compatible with the FE-I3 footprint
- Structures for measurement of misalignment
- 1. Wafer-to-wafer interconnection
- 2. Chip-to-wafer interconnection

Solid-Liquid InterDiffusion

Fraunhofer EMFT





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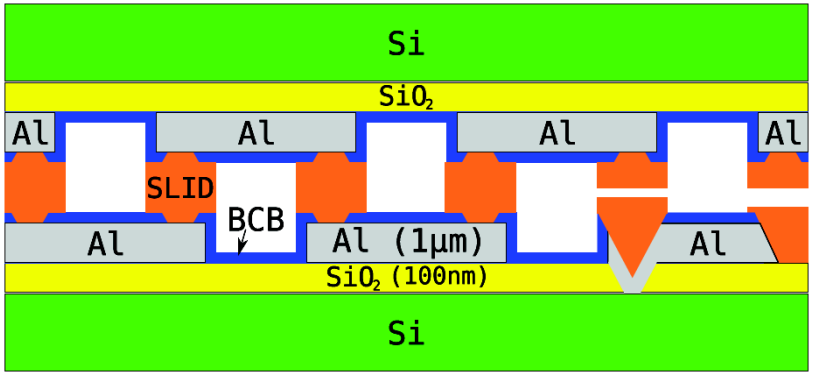
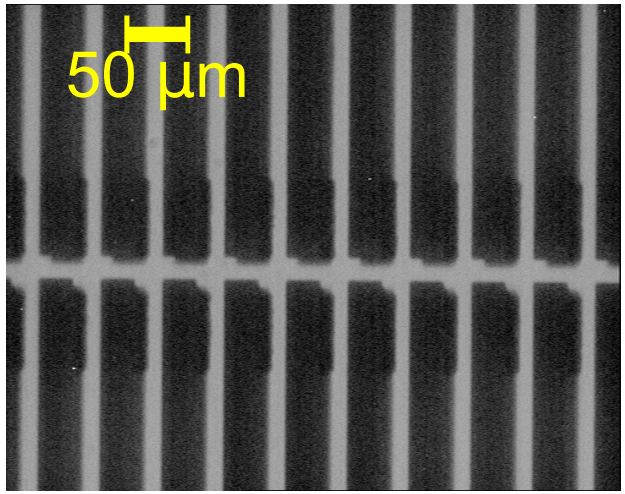
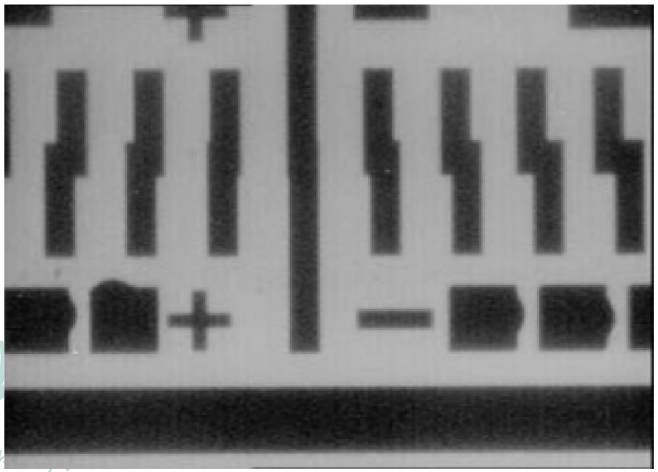
Wafer-to-wafer





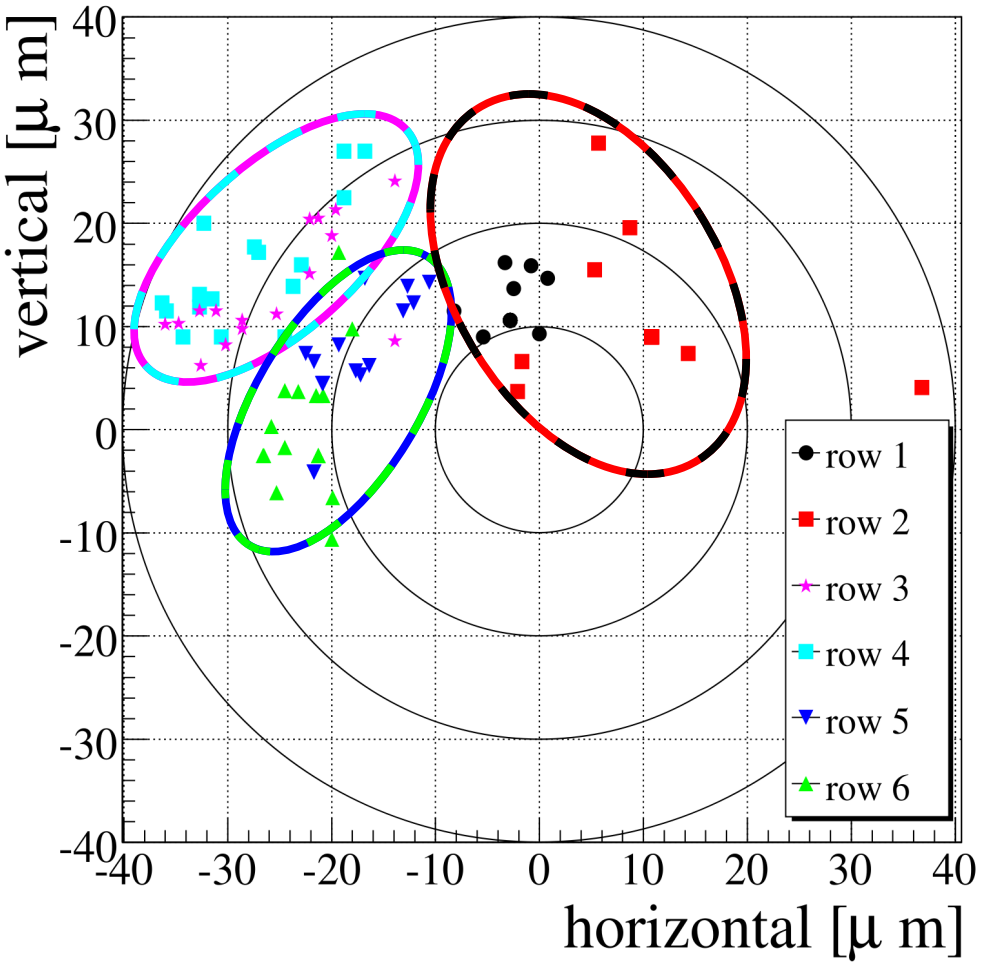


Dasiy chain test structures:

- Test structures to investigate the reliability of the SLID interconnection
- Different pad sizes and distances between SLID pads
- Deliberate introduction of aplanarities to test the sensitivity of the SLID interconnection to surface imperfection
- Placement accuracy of the wafers between 5 µm and 10 µm observed
- High connection efficiency measured:

Pad-size (μm^2)	Pad-distance	aplanarity	inefficiency
30 x 30	60 µm	-	$<1.2 \times 10^{-4}$
80 x 80	100 µm	-	$<7.8 \times 10^{-4}$
27 x 60	50 µm, 400 µm	-	$(5 \pm 1) \times 10^{-4}$
30 x 30	60 µm	100 nm	$(10 \pm 4) \times 10^{-4}$
30 x 30	60 µm	1 µm	$(4 \pm 3) \times 10^{-4}$

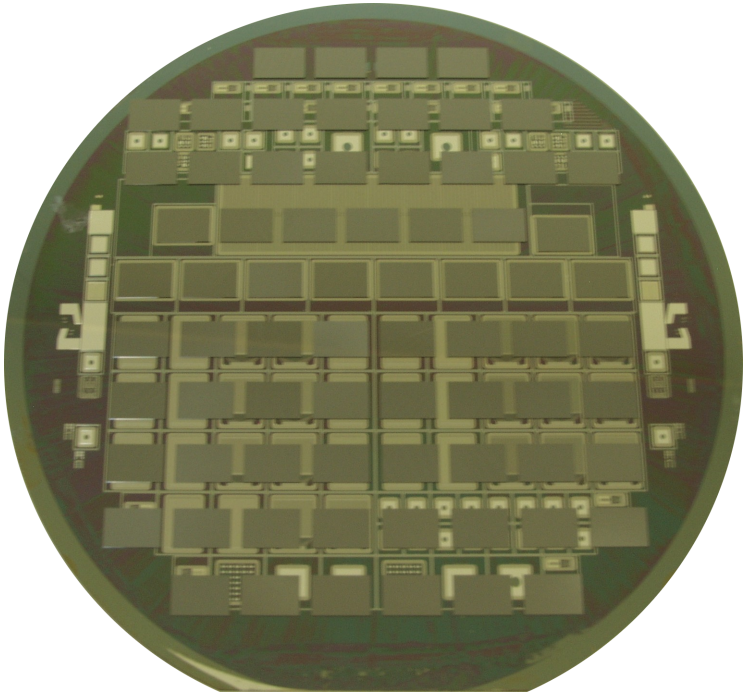
Chip-to-wafer



Pick and place precision:

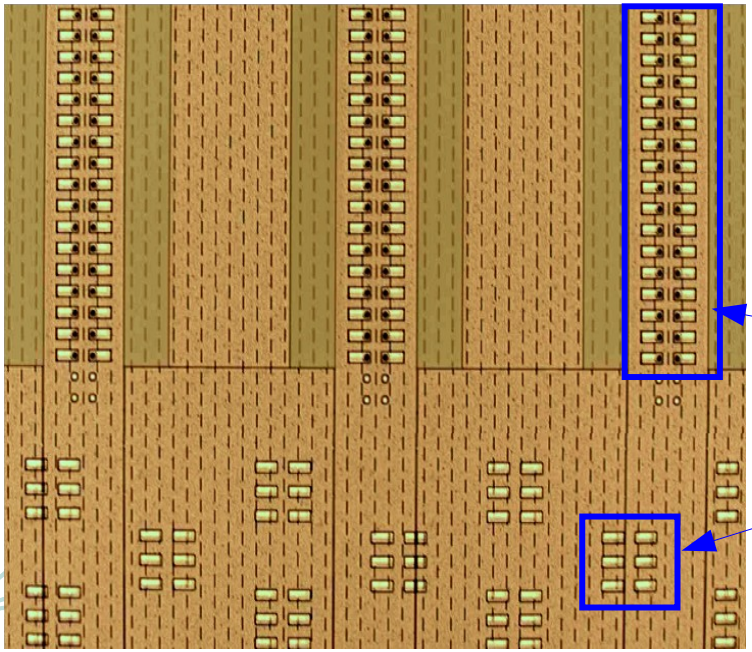
- One of the two wafers was singularized and chips were placed on a handle wafer
- Several of the chip-to-wafer interconnections were not functioning:
  - Tool swaps during the pick-and-place process
  - Different thicknesses of the single chips used (different wafers)
- Both of these problems will likely not be present for the actual FE chips that will be connected to the thin sensors

SLID: FE-I3



FE-I3 to <u>dummy</u> sensor connection:

- ATLAS pixel FE-I3 chips singularized
- Placed on handle wafer
- Connected to a dummy sensor wafer
- For each chip a corresponding UBM was prepared on the sensor side
- Study of alignment marks with IR microscope
- Visual inspection of cross-sections



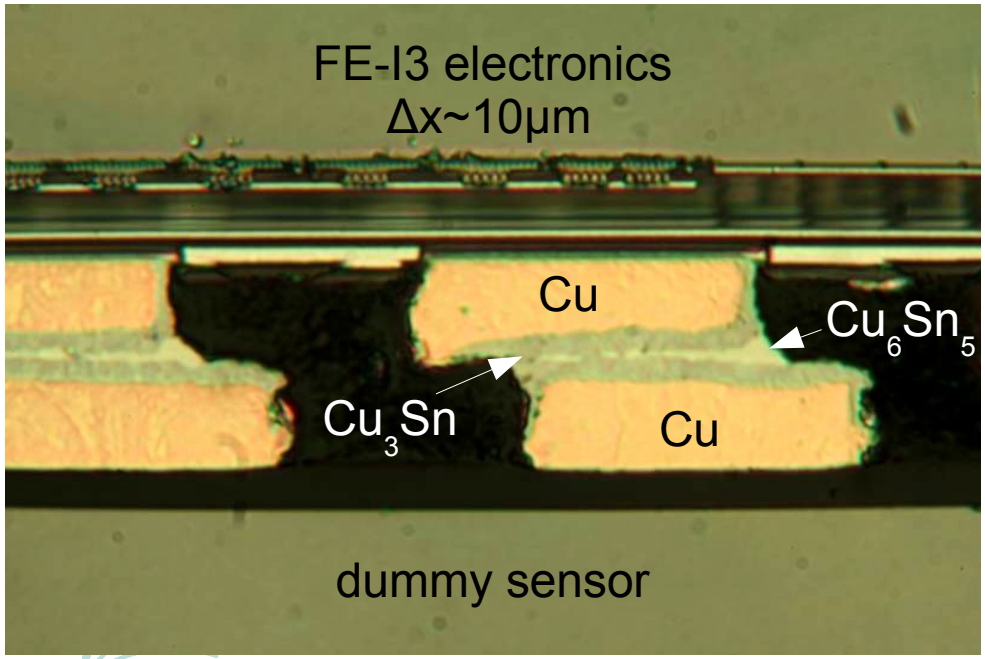
SLID pad geometry:

- Pad size: 27 x 60 µm²
- Minimum distances: 23µm, 29µm
- SLID pads in the FE-I3 over the original openings in the passivation
- SLID pads in the chip balcony to increase mechanical stability

SLID: FE-I3

Misalignment in the dummy central pixel row:

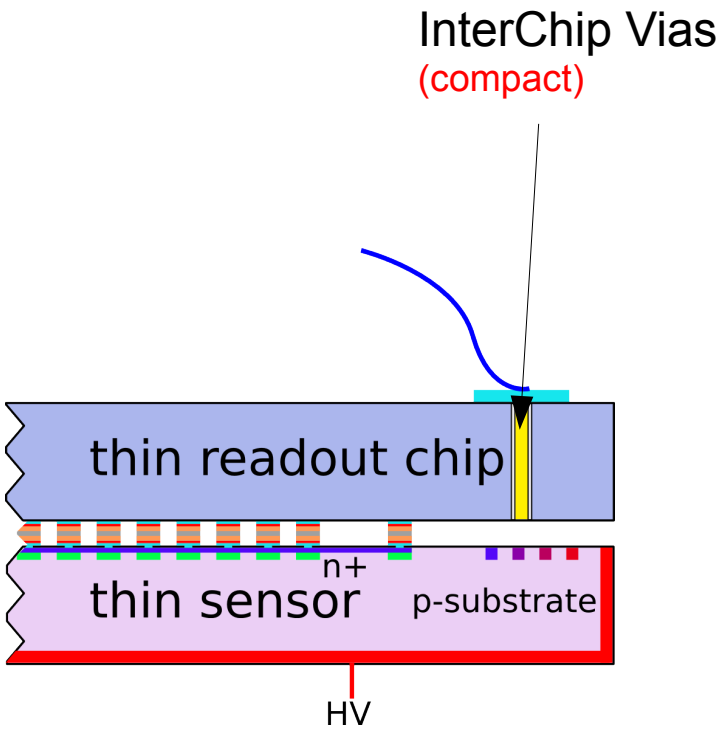
Chip	1	2	3	4	5	6	7	8	Pad size	distance
Δx [μm]	-6.2	17.2	15.3	23.8	16.5	6.8	18.4	13.4	27.0	23.0
Δy [μm]	-14.4	-26.0	-19.7	-15.3	-14.7	-12.8	-10.0	-1.2	60.0	29.0



Optical cross-section inspection:

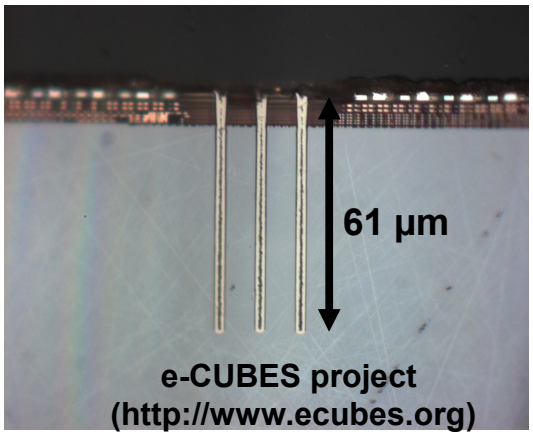
- Visible formation of Cu-Sn alloy
- Due to some misalignment interdiffusion not homogeneous in all interconnections:
  - Cu_3Sn and Cu_6Sn_5 visible
- Very acceptable misalignment for detector operation
- Tests for mechanical stability to be conducted
- Interconnections of hot chips to hot sensors is currently ongoing

The MPP module concept

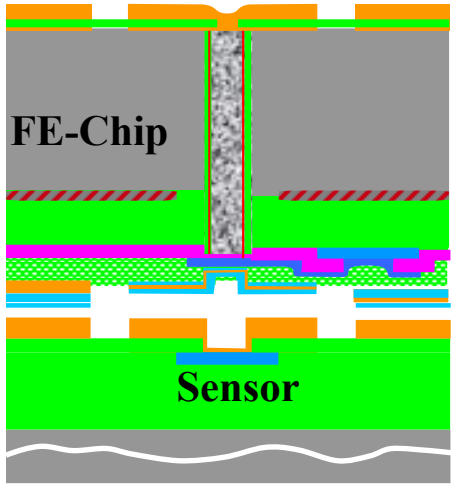


Inter-Chip Vias

Fraunhofer EMFT

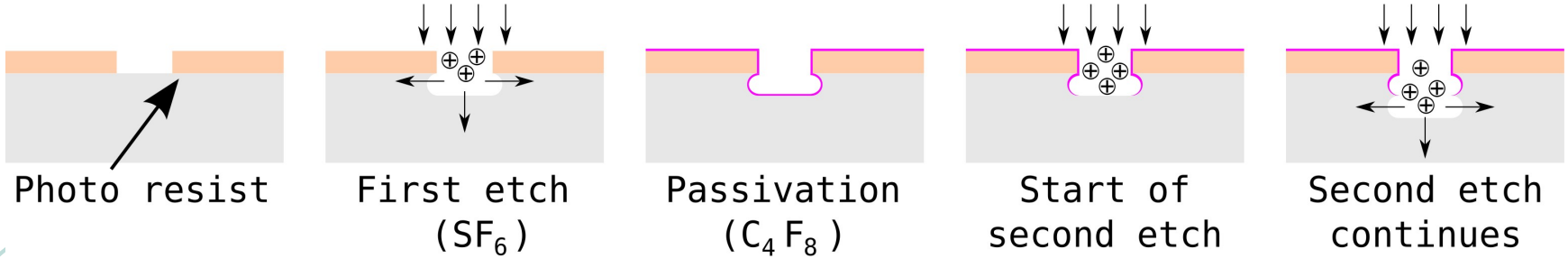


Courtesy: P. Ramm, J. Weber
(Fraunhofer EMFT)



Inter-Chip Vias (ICV):

- Allows for vertical signal transport through Si structures
  - Compact pixel modules
- Bosch-process etching and tungsten filling.
- Aspect ratio: 20:1 (3x10x60 µm³)
- Chips thinned to 50 µm
- "Via last approach"
- Active research on 3D multi-tier readout chips is performed (Marseille, Bonn, LBNL with Chartered + Tezzaron)



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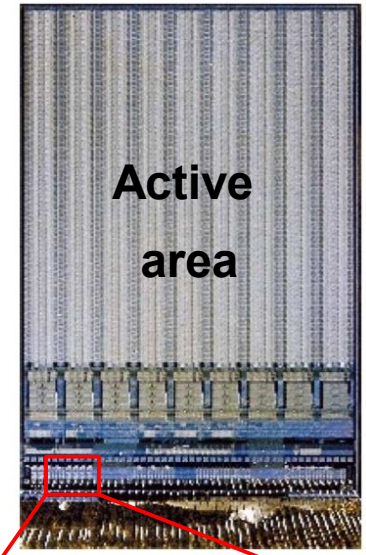
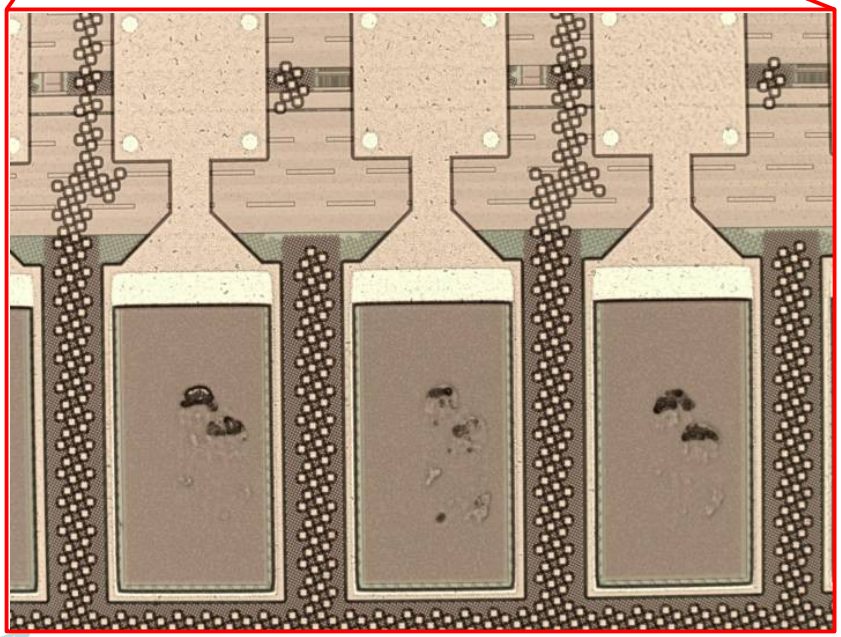
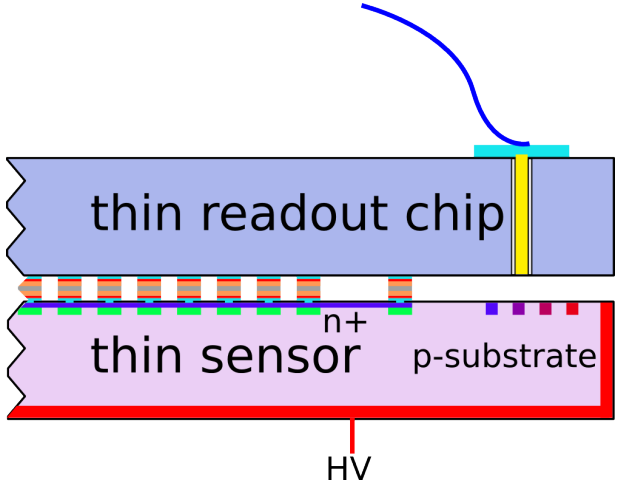


47 I/O pads



Inter-Chip Vias on the FE-I3:

- Vias are being etched in the within the digital I/O pads of the FE-I3
- No affection of the FE circuit (only place possible)
- This allows for easy readout with present standard readout hardware



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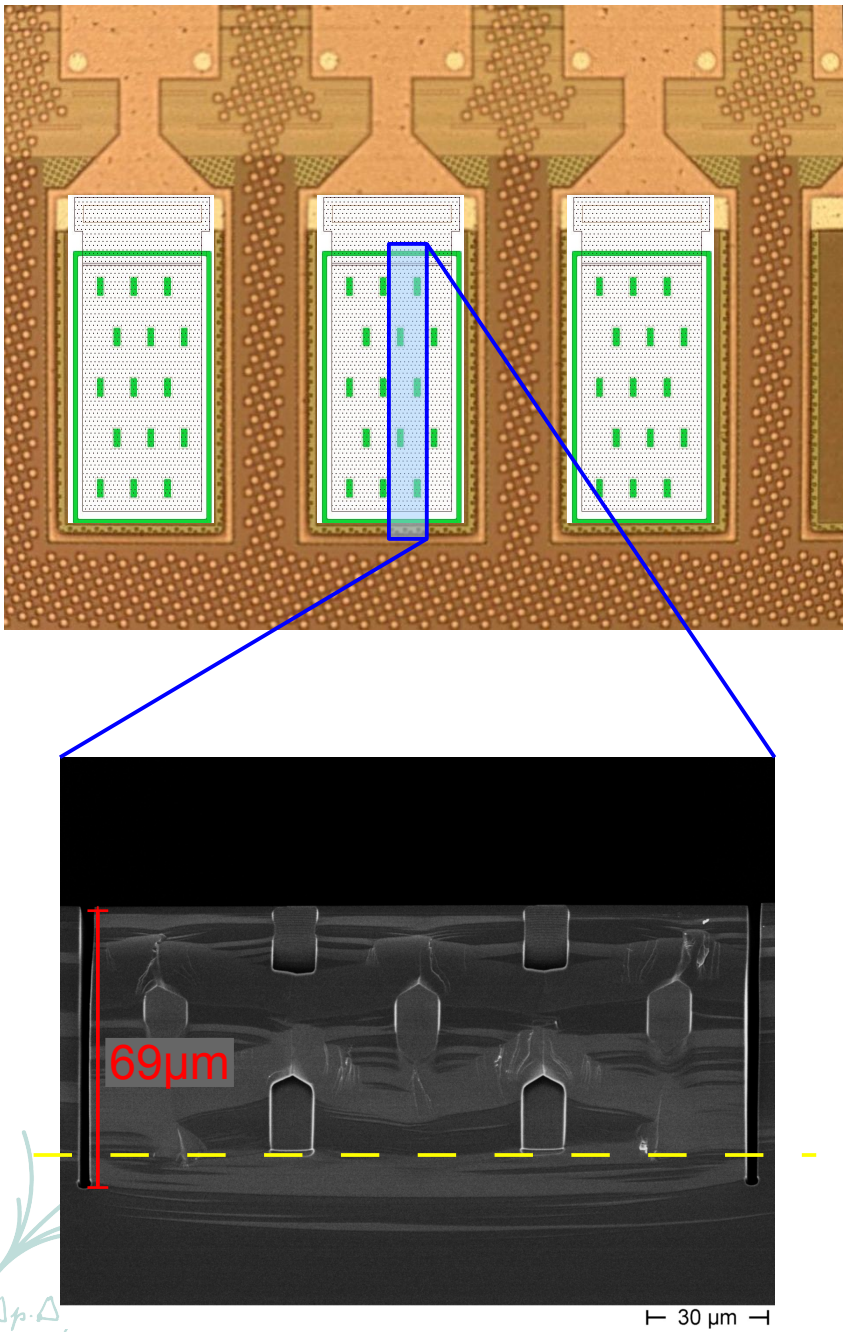

First etched vias:

- Performed in the un-thinned FE-I3 chips of one designated test wafer
- Etched to a depth of ~ 69 µm
- Rough cut/break along the long dimension of a test structure shows the structure of the vias and the trench around
- Next steps:
  - Perform via etching and filling on the hot FE-I3 wafers
  - Connect the readout chips with SLID to the hot sensor wafers
  - Connect the single chip demonstrator module to the ATLAS USB-Pix readout system.

Summary and outlook:

- The MPP is developing a novel pixel module with:

Thin n-in-p sensors:

- Thin sensors of 75µm and 150µm active thickness showed a high charge collection efficiency and high device yield
- A new sensor production for the IBL qualification is being currently produced

3D integration with SLID + ICV (EMFT):

- Wafer-to-wafer SLID: high connection efficiencies
- FE-I3 chips were successfully connected to dummy sensors
- Connection of hot chips is currently carried out
- Inter-Chip Vias were etched in the FE-I3 chips
- Single chip modules with SLID will be ready late 2010 or early 2011
- Single chip modules with SLID and ICV should be testable in mid 2011

Thank you for your attention!