A 20 GS/s sampling ASIC in 130nm CMOS technology.

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TWEPP 2010, Aachen , Germany

Outline

- Context
- Fast timing and Waveform analysis
- Sampling Electronics
- 130nm CMOS Waveform Sampler Tests
- Next chip
- Conclusion - Perspective

Context

Fast photo-detectors :

Timing resolution:

Time of flights with accuracies in the 10-100ps range, sensitive to single photo-electron.

- Photomultipliers,
- Pin diodes
- Avalanche Photo-Diodes
- Solid state photomultipliers,
- Micro-channel plate

Position resolution:

- Pixilated structure:

- Multi-anode PMTs
- Solid state devices

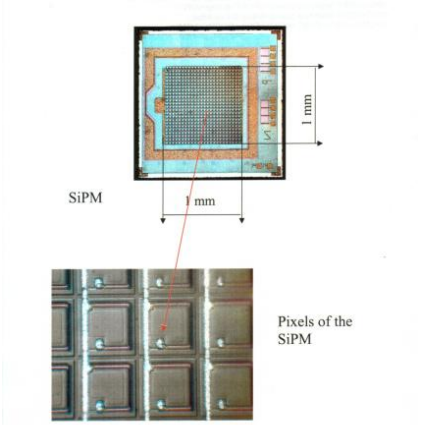
- Transmission lines readout

- Micro-channel Plates

Timing-Imaging Devices

Multi-anodes PMTs
Dynodes

Silicon-PMTs [10]
Quenched Geiger in Silicon

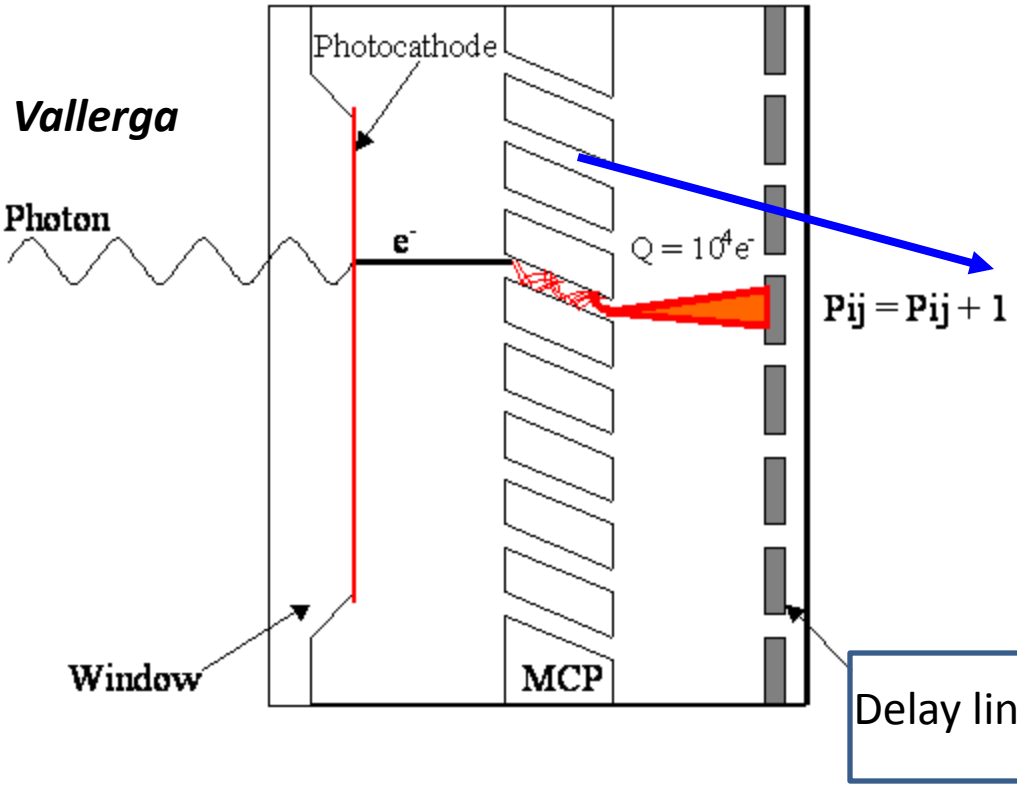


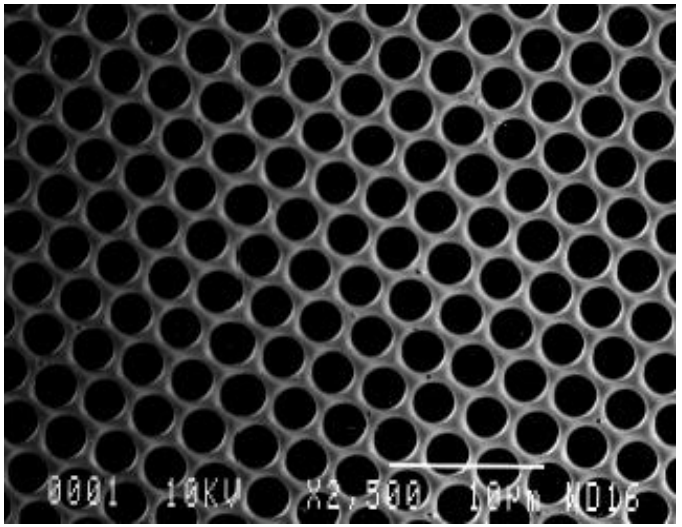
Micro-Channel Plates [1]
Micro-Pores

Quantum Eff.	30%	90%	30%
Collection Eff.	90%	70%	70%
Rise-time	0.5-1ns	250ps	50-500ps
Timing resolution (1PE)	150ps	100ps	20-30ps
Pixel size	2x2mm^2	50x50μm^2	1.5x1.5mm^2
Dark counts	1-10Hz	1-10MHz/pixel	1Hz-1kHz/cm^2
Dead time	5ns	100-500ns	1μs
Magnetic field	no	yes	15kG
Radiation hardness		1kRad=noisex10	good (a-Si, Al_2O_3)

Timing Imaging Devices
Micro-Channel Plate Detectors

J. Vallerga





Timing Resolution: Single Photo-Electron Time Transit Spread:

$$\sigma_t^2 = \sigma_{1\,stgap}^2 + \sigma_{pore}^2 + \sigma_{2\,ndgap}^2$$

Large Area Pico-second Photo-Detectors

Objective:

Develop 20x20cm2 Micro-Channel Plate
- ~1mm space resolution
- a few ps timing resolution.

Effort distributed in 5 groups:
- Hermetic packaging
- Photocathode
- MCP
- Electronics
- Integration.

Teams :

3 Nat. Labs, 5 Universities, 3 companies.

Time scale:

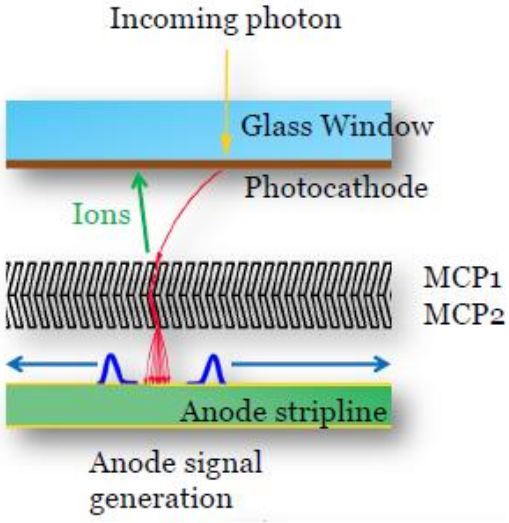
3-5 years.

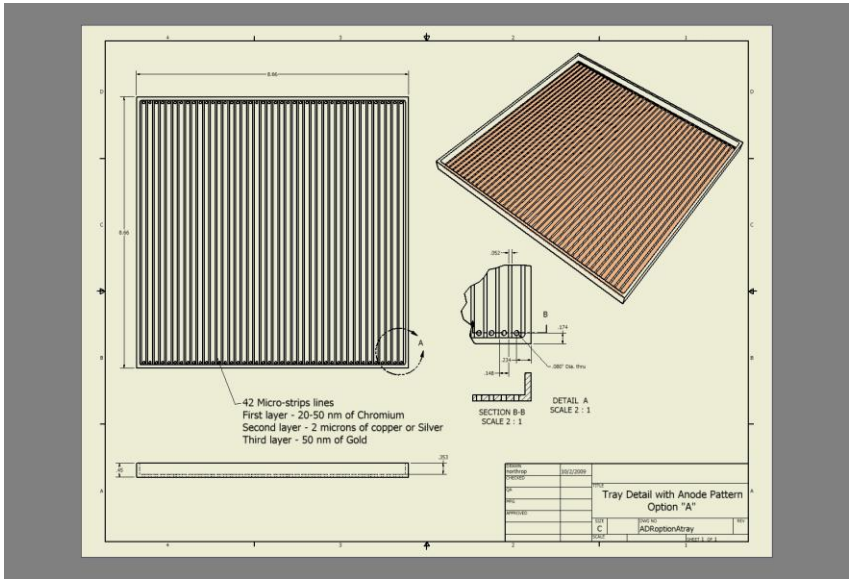
Funding:

Dept. Of Energy

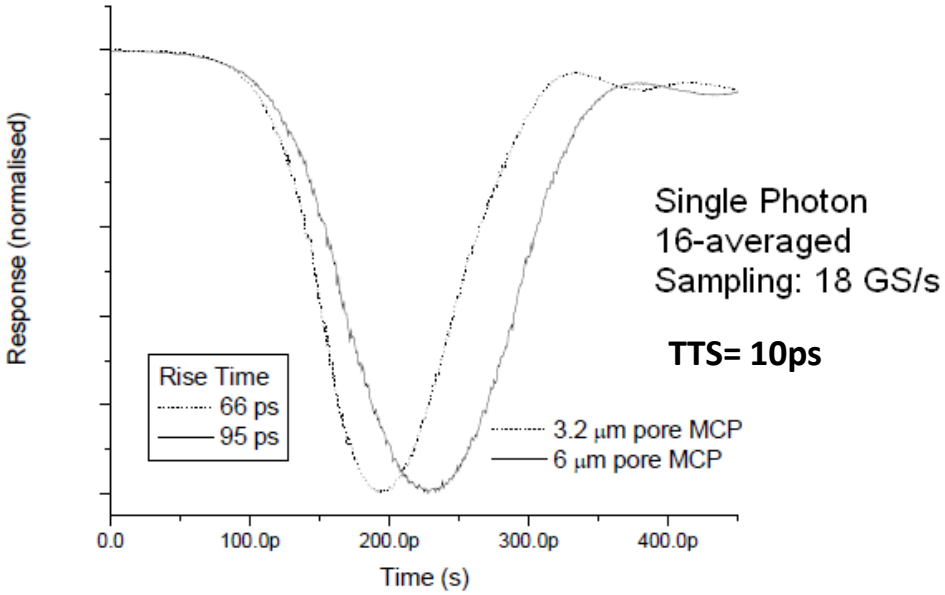
Web page and docs:

http://psec.uchicago.edu

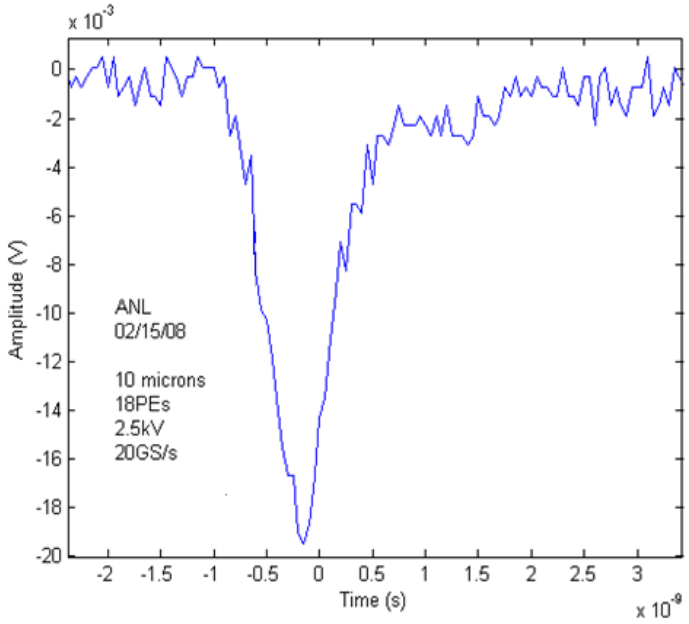




Fast Micro-Channel Plate signals



Time response curves for two models of PMT110 with different MCP pore diameters.



2" x 2" ***imaging*** MCP (BURLE/PHOTONIS)

From Photek

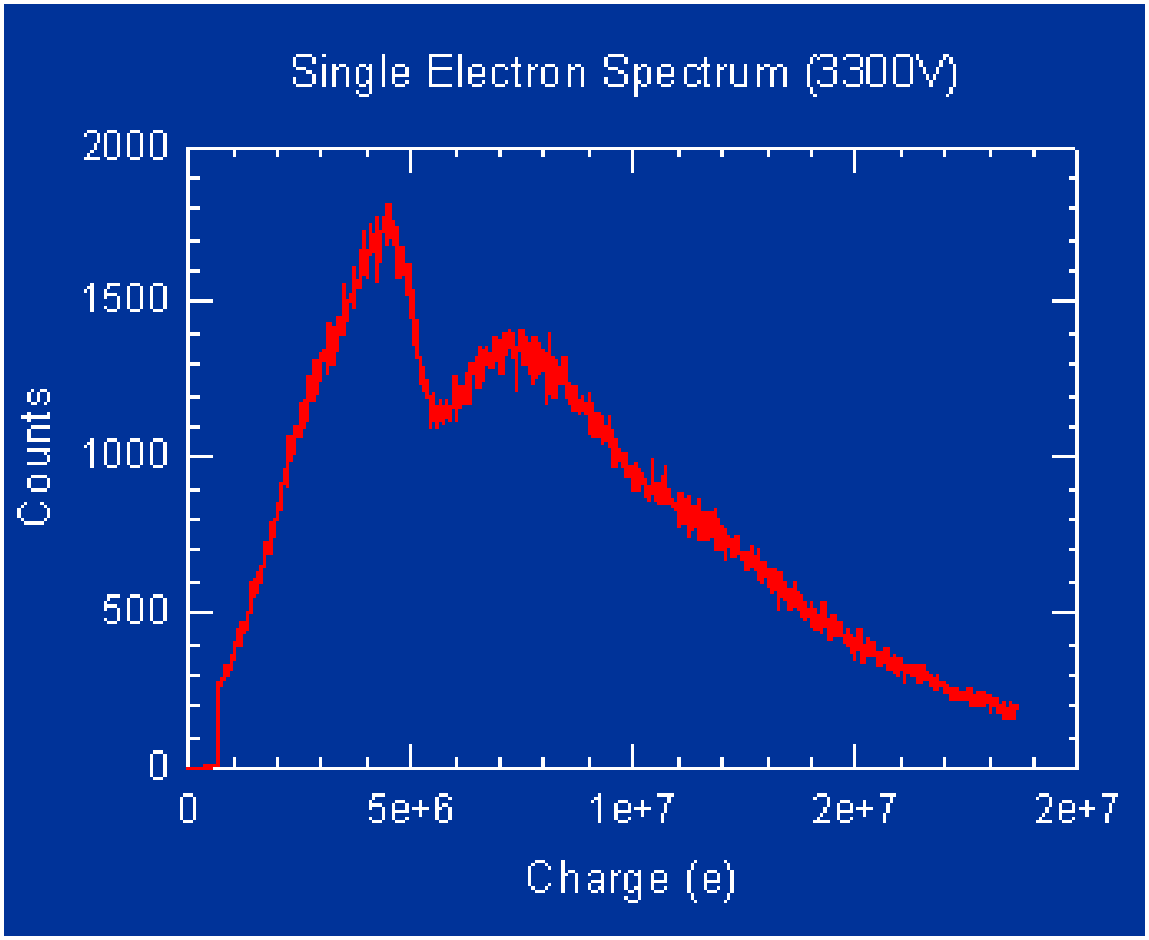
Data taken at Argonne National Lab

11 mm diameter Micro-Channel Plate signal
Signal bandwidth: 10 GHz
Timing resolution:
Single Photoelectron Time Transit Spread: 10ps

2" x 2" Micro-Channel Plate
2 GHz

30ps

MCP Single Photo-Electron response



From Burle-Photonis (Paul Hink)

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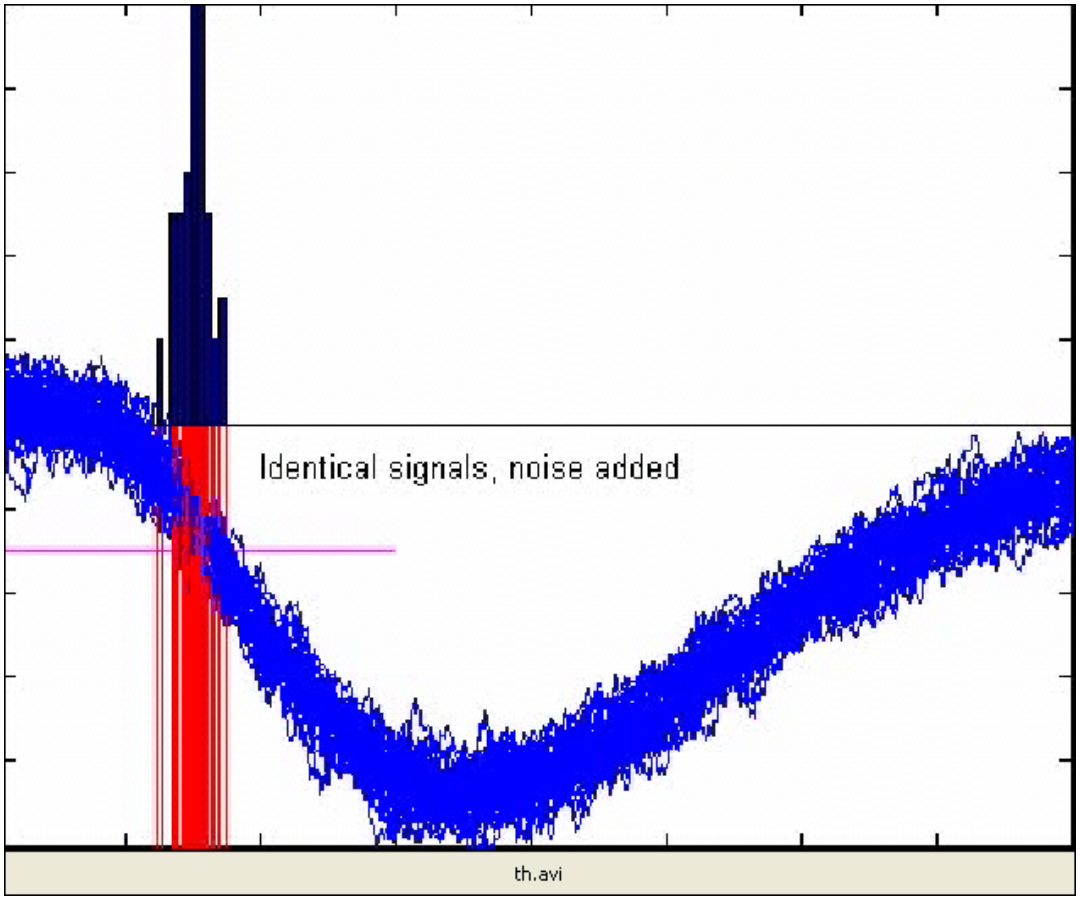
Timing resolution

Single Threshold



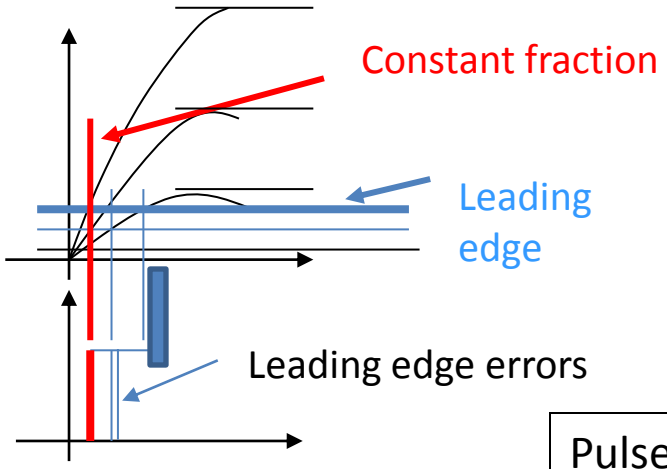
$$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$$

Time spread proportional to 1/rise-time and noise

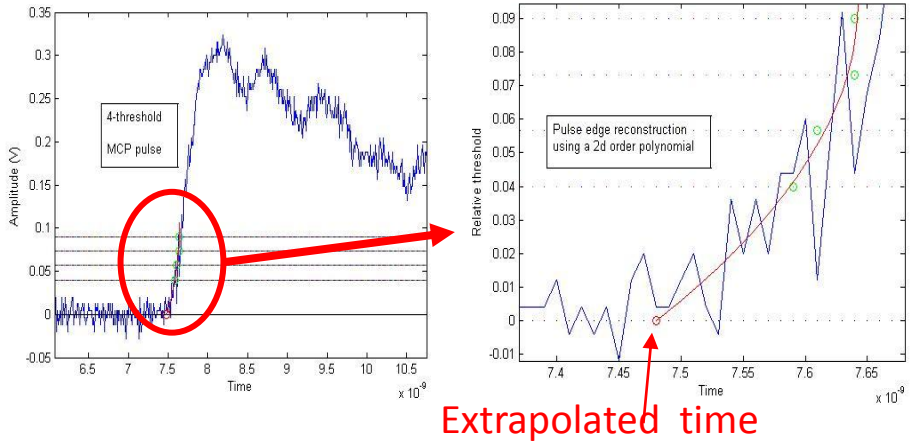
Timing techniques

ANALOG

Constant-fraction

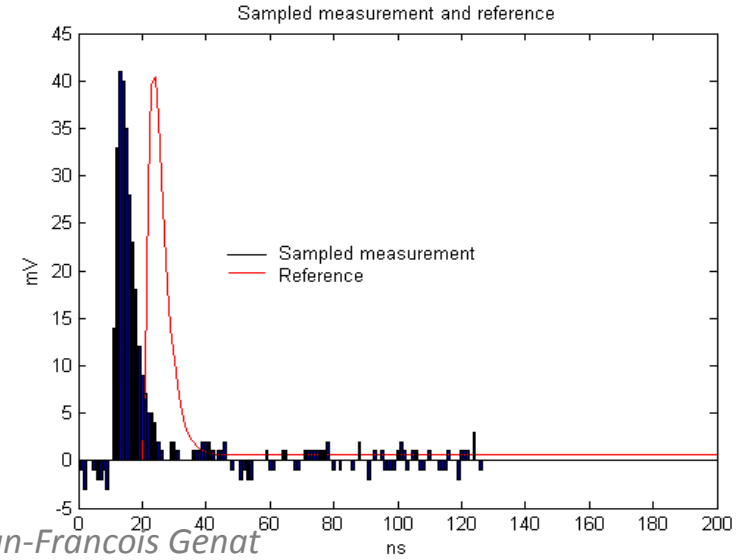


Multi-threshold



Pulse sampling and Waveform analysis

DIGITAL



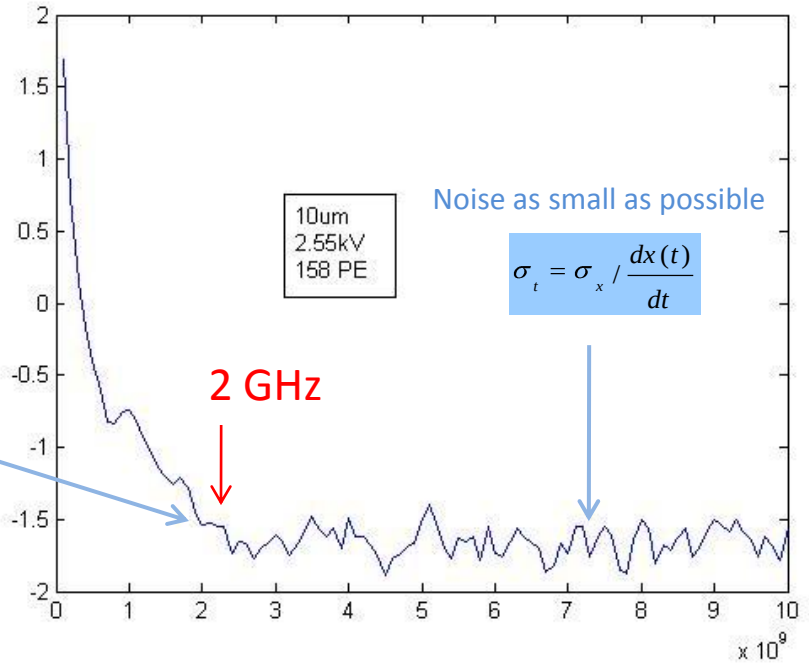
Sample, digitize,
Fit to the (known) waveform
Get time and amplitude

Picosecond Digital Electronics for Micro-Channel Plate Detectors

Store the full detector information as a digital oscilloscope:

- Detector + electronics noise >> quantization noise (LSB/√12)
- Sampling frequency > 2 x full Analog Bandwidth (Shannon-Nyquist)

Fourier spectrum of a 2"x 2" MCP signal



$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$

Slope as steep as possible

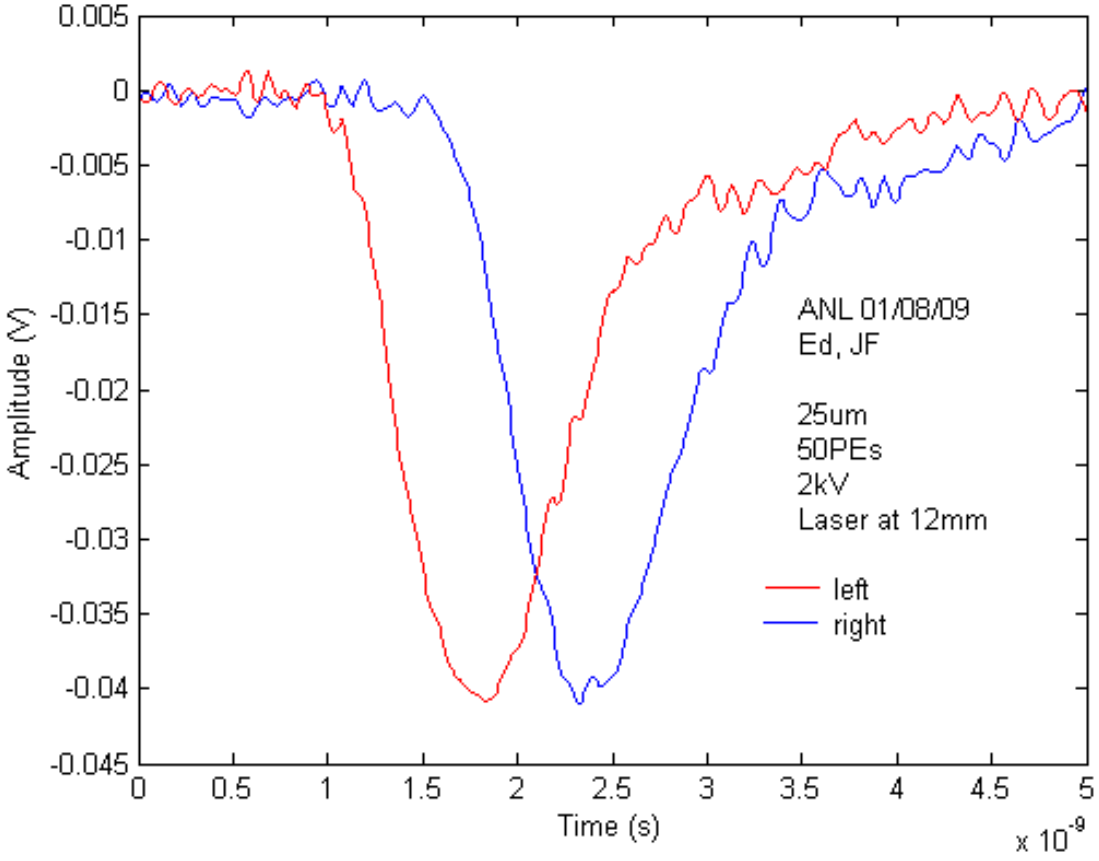
Noise as small as possible

$\sigma_t = \sigma_x / \frac{dx(t)}{dt}$

ADC: Digitize on the fly, if the two above conditions can be fulfilled.
SCAs: If not, use Analog Memories, if input rate and ADC conversion time allows.

Position resolution. Transmission Line Readout

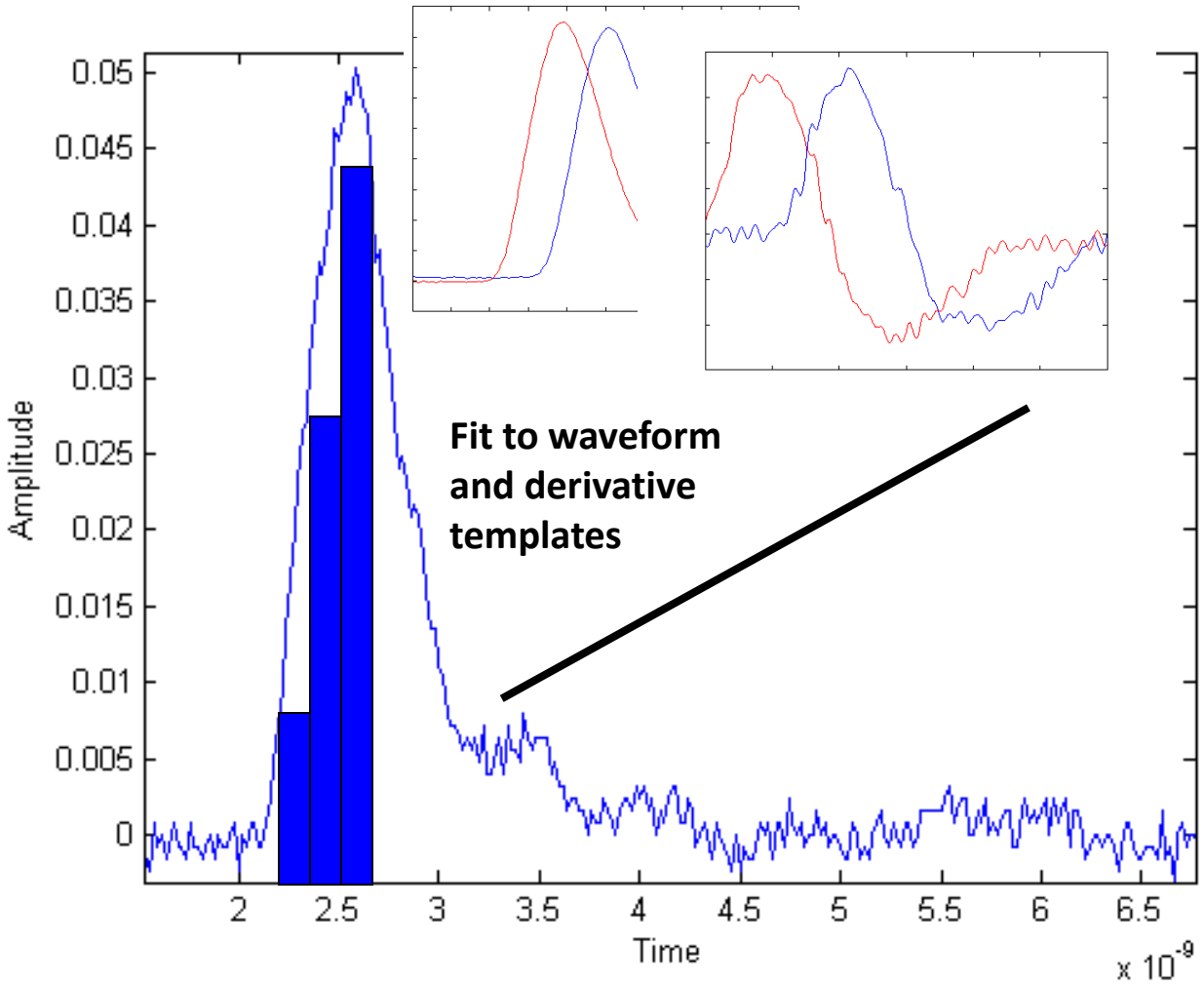
50 PEs

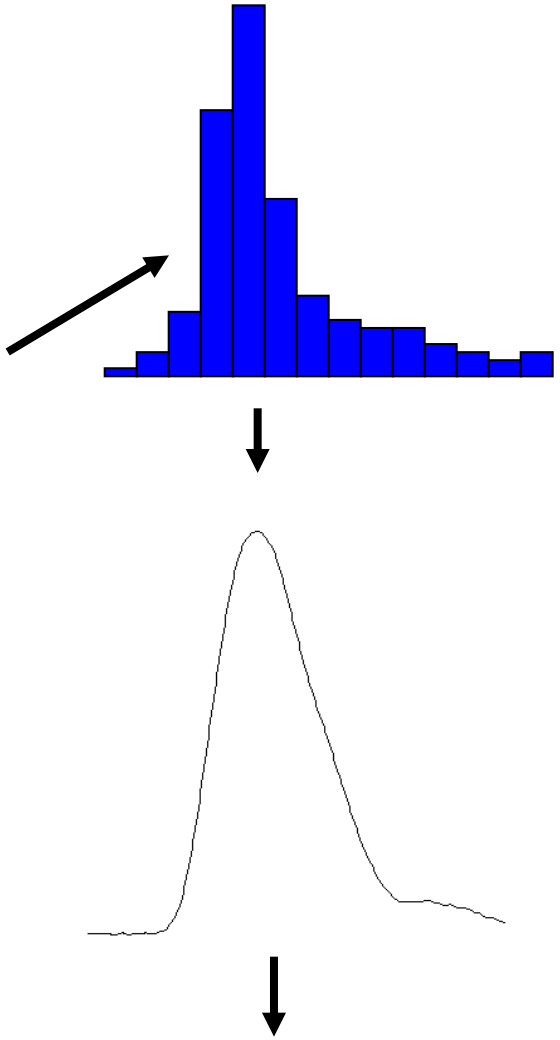


Oscilloscope
TDS6154C
Tektronix

25 μm pore MCP signal at the output of a ceramic transmission line
Laser 408nm, 50Ω, no amplification

Digital Waveform Analysis



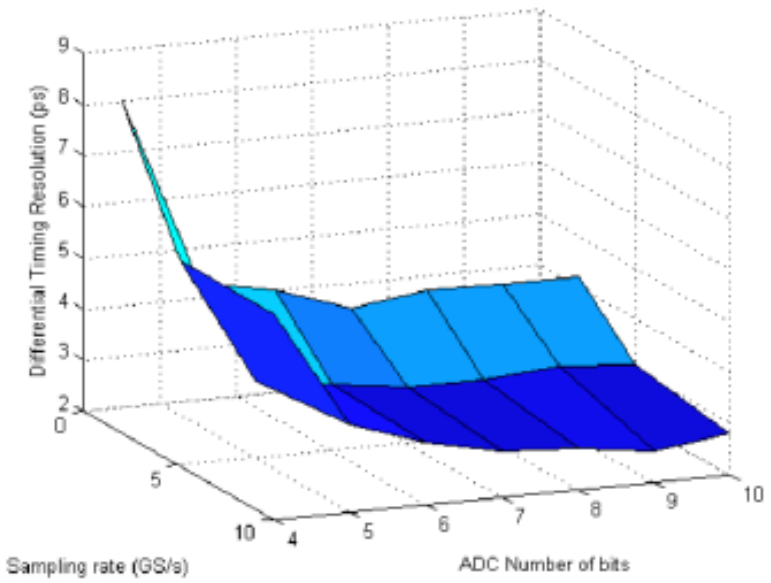


Psec Timing
and Charge

Timing resolution with Fast Waveform Sampling

At 1GHz analog bandwidth:

bits	2GS/s	5GS/s	10GS/s
8	4.2ps	3.1ps	2.8ps
7	4.0ps	3.1ps	2.9ps
6	4.5ps	3.3ps	3.2ps
5	4.8ps	3.5ps	3.7ps
4	8.5ps	6.1ps	5.9ps



Waveform sampled MCP data taken with a TDS6145C oscilloscope

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Fast Waveform Sampling Electronics

- Integration for large scale detectors ~ $10^{4\text{-}6}$ channels.
- Control sampling rate, sampling depth, sampling window.
- Self trigger for data sparsification, or/and common stop.
- Low power.
- High reliability
- Very low cost for high quantities.

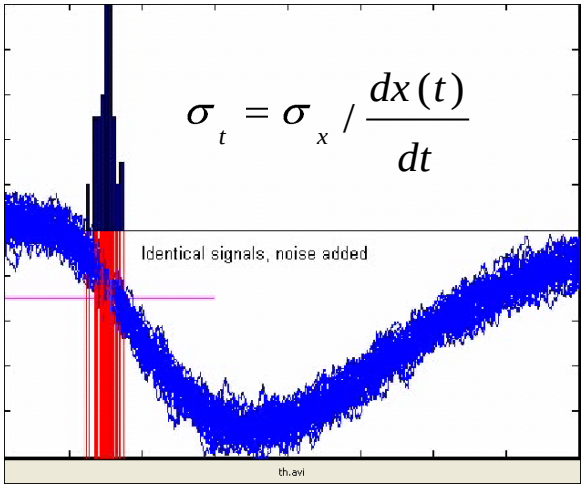
ASIC

Fast Digital Electronics for Micro-Channel Plate Detectors

A/D state of the art:

8-bit 1GS/s
10-bit 300 MS/s
16-bit 160 MS/s

Need at least 5 GS/s sampling rate, 10-12bit
There is no !



Fast analog storage + slower digitization, if input rate and dead-time allows.

Apply the best timing algorithm suited to the detector waveform

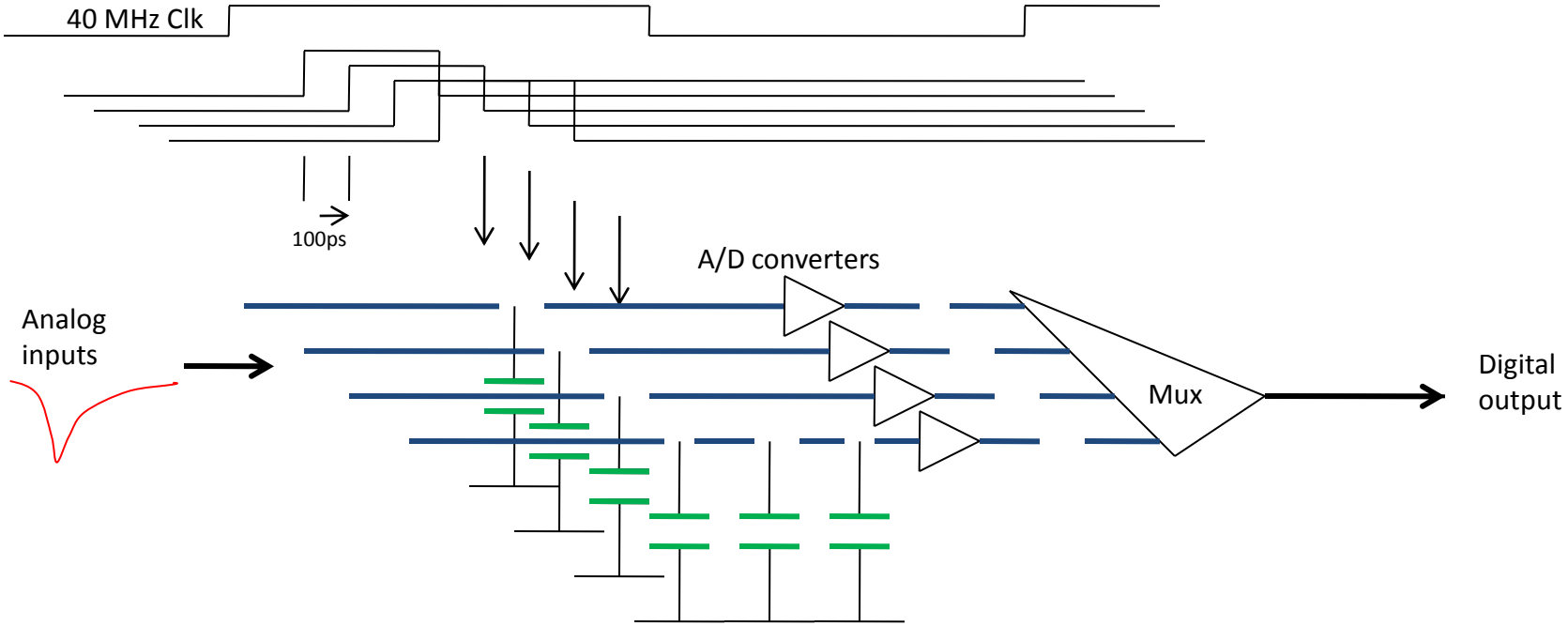
Sampling Chips Survey

	Hawaii	Varner		Saclay/Orsay	Delagnes/	Breton		PSI	S.Ritt	This proposal
	Blab1	Lab1-2	Lab 3	Hamac	Matacq	Sam	Planned	DRS3	DRS4	
Sampling	100 MHz-6 GHz		20 MHz-3.7GHz	40 MHz	0.7-2.5 GHz	0.7-2.5 GHz	10 GHz	10 MHz-5 GHz	5 GHz	10-20 GHz
Bandwidth (3db)	300 MHz		900 MHz	50 MHz	200-300 MHz	300 MHz	650 MHz	450 MHz	950MHz	> 1.5 GHz
Channels	1	8	9	8	1	2		12 6 2 1	8 4 2 1	4 16
Triggered mode	Yes		Common stop		Yes			Common stop	Common stop	Channel trigger
Resolution	10 bit			13.3 bit	13.4 bit	11.6 bit		11.6 bit	11.5 bit	8-10-bit
Samples	128 rows of 512	256	256	144	2520	256	2048	1024-12288	1024-8192	256
Clock			33 MHz	40 MHz	100 MHz				fsamp/2048	20-40 MHz
Max latency	560 us	2.2ms	50us							
Input Buffers	Yes			Yes	Yes	Yes	No	No	No	No
Differential inputs	No	No	No	Yes	Yes	Yes		Yes	Yes	Yes
Input impedance	50 Ohms	50 Ohms	50 Ohms Ext	10 MOhm/3pF	50 Ohms				11pF	50 Ohms
Readout clock	500 MHz			5 MHz	5 MHz	16 MHz		33 MHz	33MHz	500 MHz
Locked delays	Ext DAC	Ext DAC	Ext DAC			Yes		Ext PLL	Int PLL	Int PLL
On-chip ADC	12-b +500MHz TDC			No		No		No	No	Yes
R/W simultaneous	Yes			Yes		No		No	Yes	No
Power/ch	15mW/1.6W			36 mW	250-500 mW	150 mW		2-8mW	7.2mW at 2GS/s	
Dynamic range	1mV/1V			0.26mV/2.75V	175 uV-2V	0.65mV-2 V		0.35mV/1.1V	.35mV/1V	1V
Xtalk	Inter-rows 0.1%		10%			0.30%		< 0.5%		
Sampling jitter			4.5ps			25ps			6ps	?
Power supplies	-tbd/+2.5	-tbd/2.5V	-tbd/2.5V	-1.7/3.3V				2.5V	2.5V	1.2V
Process	TSMC .25	TSMC .25	TSMC .25	HP/DMILL .8	AMS .8	AMS .35	AMS .18	UMC .25	UMC .25	IBM .13
Chip area	5.25 mm2	10 mm2	2.5mm2	19.8mm2	30mm2			25mm2		1mm2/ch
Temp coeff	0.2%/◦C		0.2%/◦C					5e-5/◦C	25ppm/◦C	
Cost/channel	500$/40 10$/2k								10-15$	

Sampling ASIC Sequence of operations

-1 Write: The timing generator runs continuously, outputs clock phases 100ps spaced. Each phase closes a write switch during one sampling window.

-2 Trigger: Opens all the write switches. Analog input history stored in the capacitors.



-2 A/D conversion: after a trigger starts all A/D conversions in parallel Data available after 2 μs 2GHz counters)

-3 Read occurs after conversion (data can still be taken as in Phase 1)

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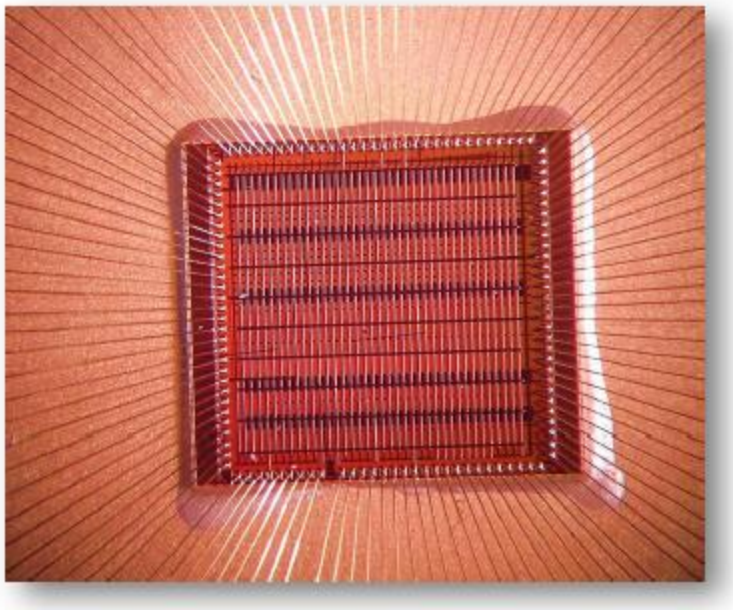
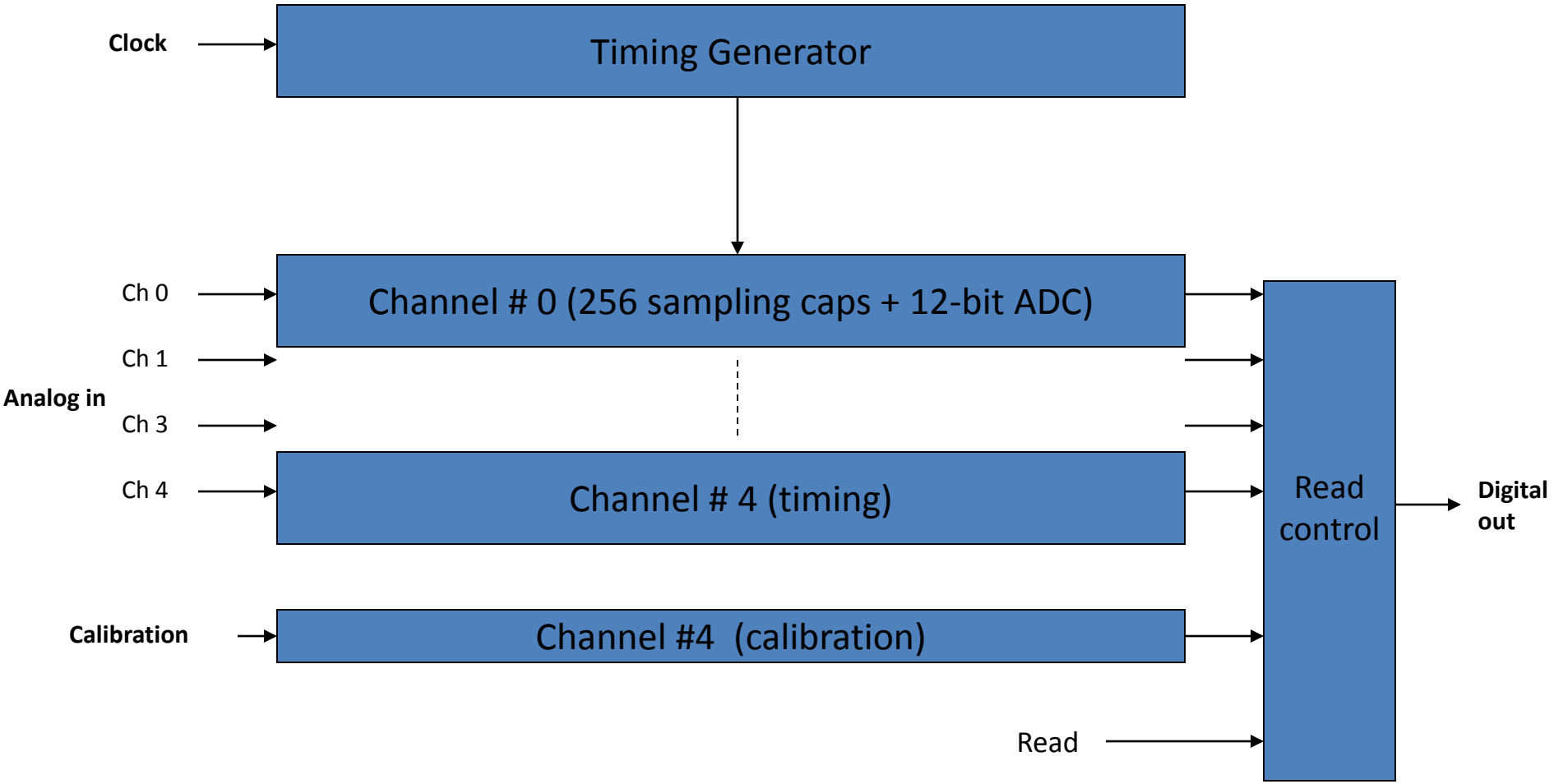
Waveform Sampler ASIC specs



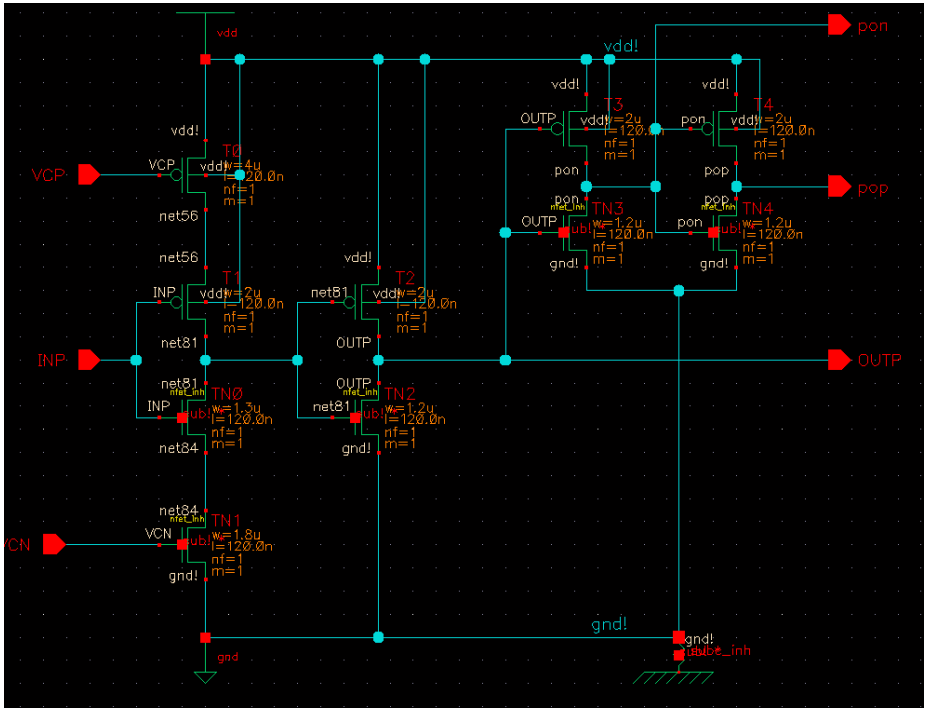
Channels 4 + 1 test
Sampling rate 10-15 GS/s
Analog Bandwidth 1-2GHz
Self and External trigger
Dynamic range 800mV
Sampling window 400ps-800ps (or 8 delay cells)
DLL Timing generator Internal phase comparator and charge pump, external LP filter
DC Input impedance ½ 50Ω internal, ½ external
Conversion clock Adjustable 500MHz 1GHz internal ring oscillator.
Maximum conversion time 8us.
Read clock 40 MHz. Readout time (4-channel) 4 x 256 x 25ns=25.6 µs
Power 40mW/channel
Power supply 1.2V
Process IBM 8RF-DM (130nm CMOS)

Block diagram



Timing Generator
Voltage Controlled Delay Cell

- 256 voltage controlled delay cells, 50-200ps each
- 20-80 MHz clock propagated

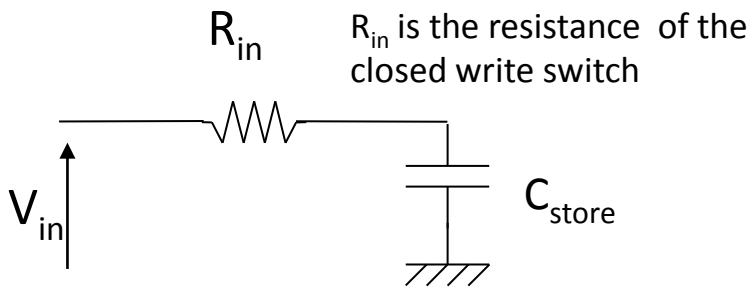


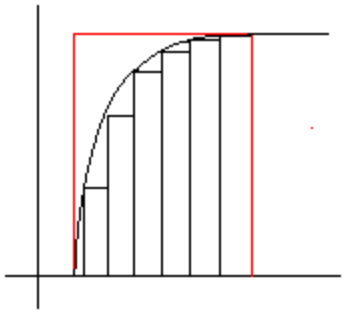
Voltage Controlled Delay Cell

Test structure:
Ring Oscillator: Two delay cells + inverter

Analog Bandwidth and Sampling Window

On chip:





Sampling window

- Analog bandwidth:

In practice, R_{in} and C_{store} are minimum, but limited by the stray capacitor of the switch, and the leakage current of the switch in the open state.

- **Sampling window**

Number of switches closed at a time x sampling period

The Analog Bandwidth does not depend upon the Sampling Window width

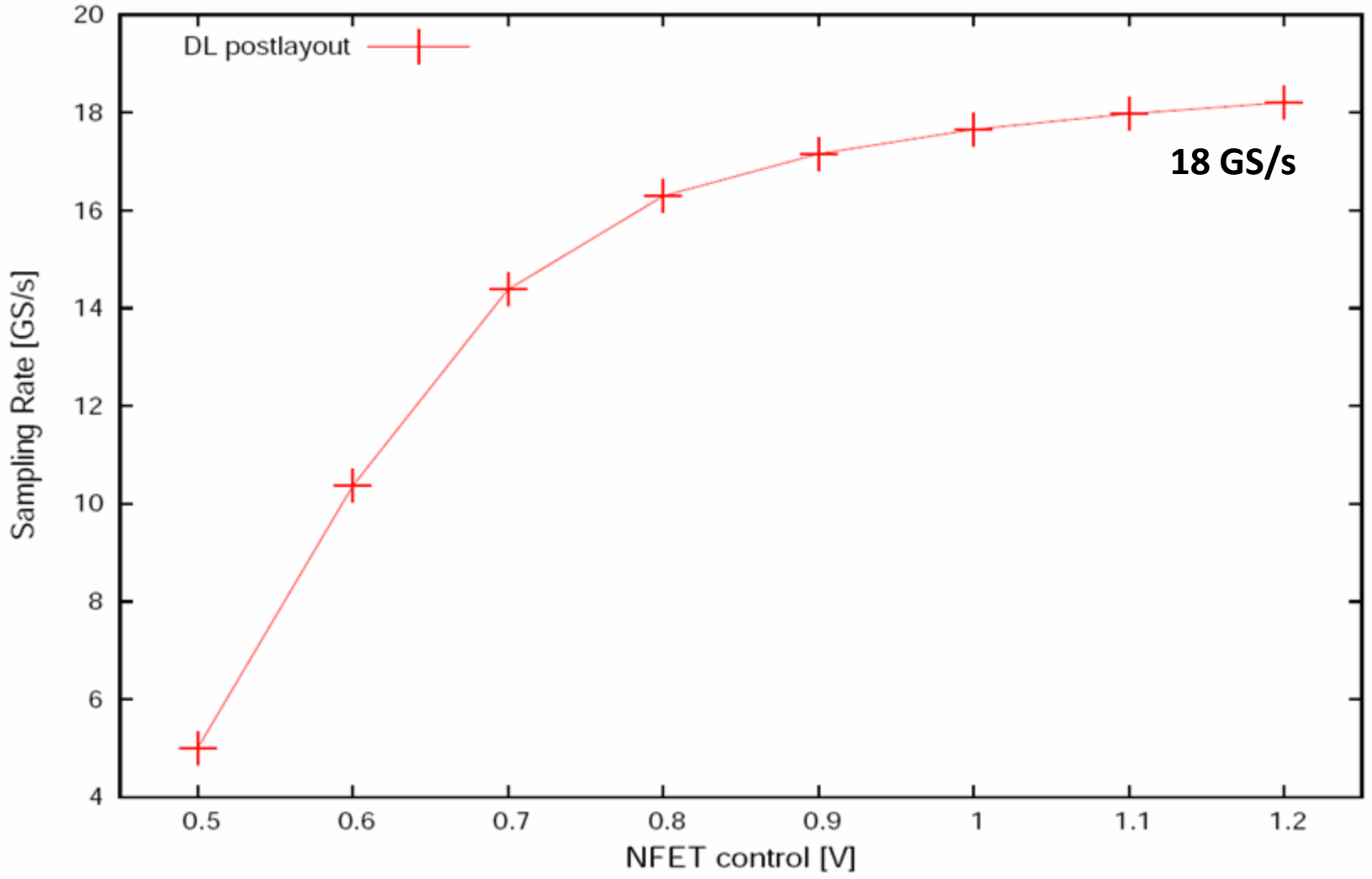
Off chip:

Inductance of the wire bonds and pad capacitance:

Bump-bonding investigated vs wire bonding

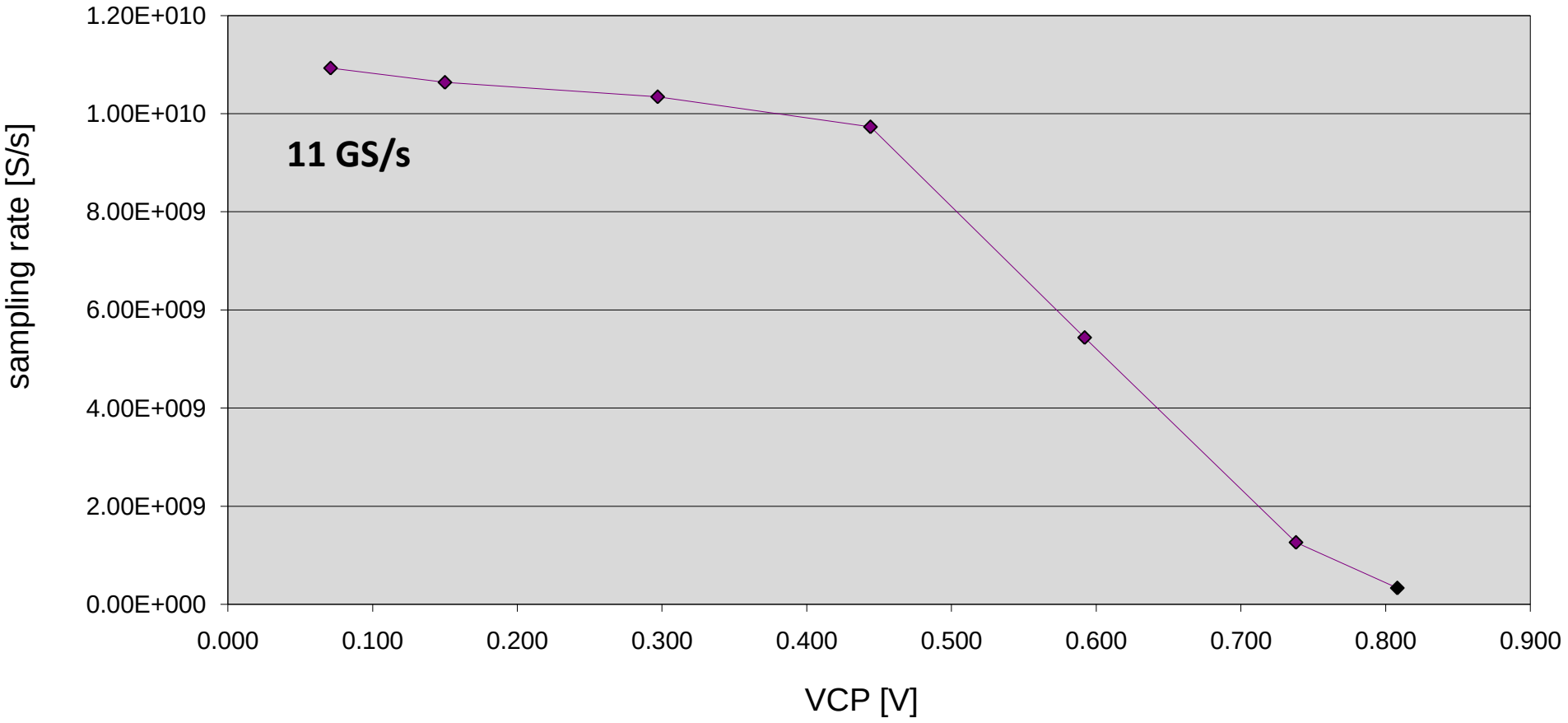
Sampler ASIC test card

Timing Generator simulation



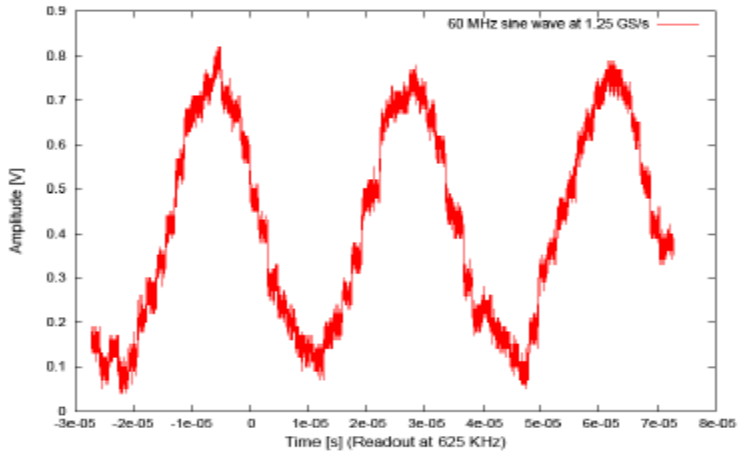
Timing Generator Tests

Sample rate

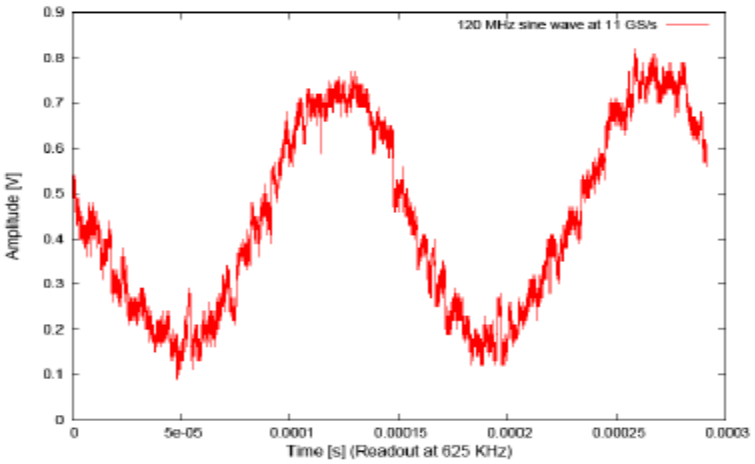


Sampling Rate tests

Sampled waveforms using Analog-out



1.25 GS/s



11 GS/s

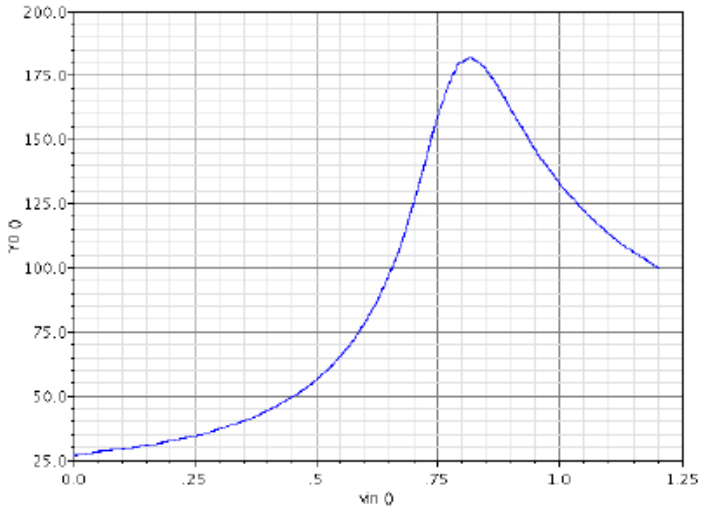
ADC not functional (still investigated)
Sampled waveforms using the analog output at 1.25 GS/s 11 GS/s .

Noise partly due to the test set-up. Under investigations.

Analog bandwidth simulated

Sampling capacitor + input buffer is ~100fF

Sampling switch “on” resistance



The Ron resistance is Voltage dependent. There fore the rise time will be amplitude dependent inside the cell. Ron ~ 100Ω

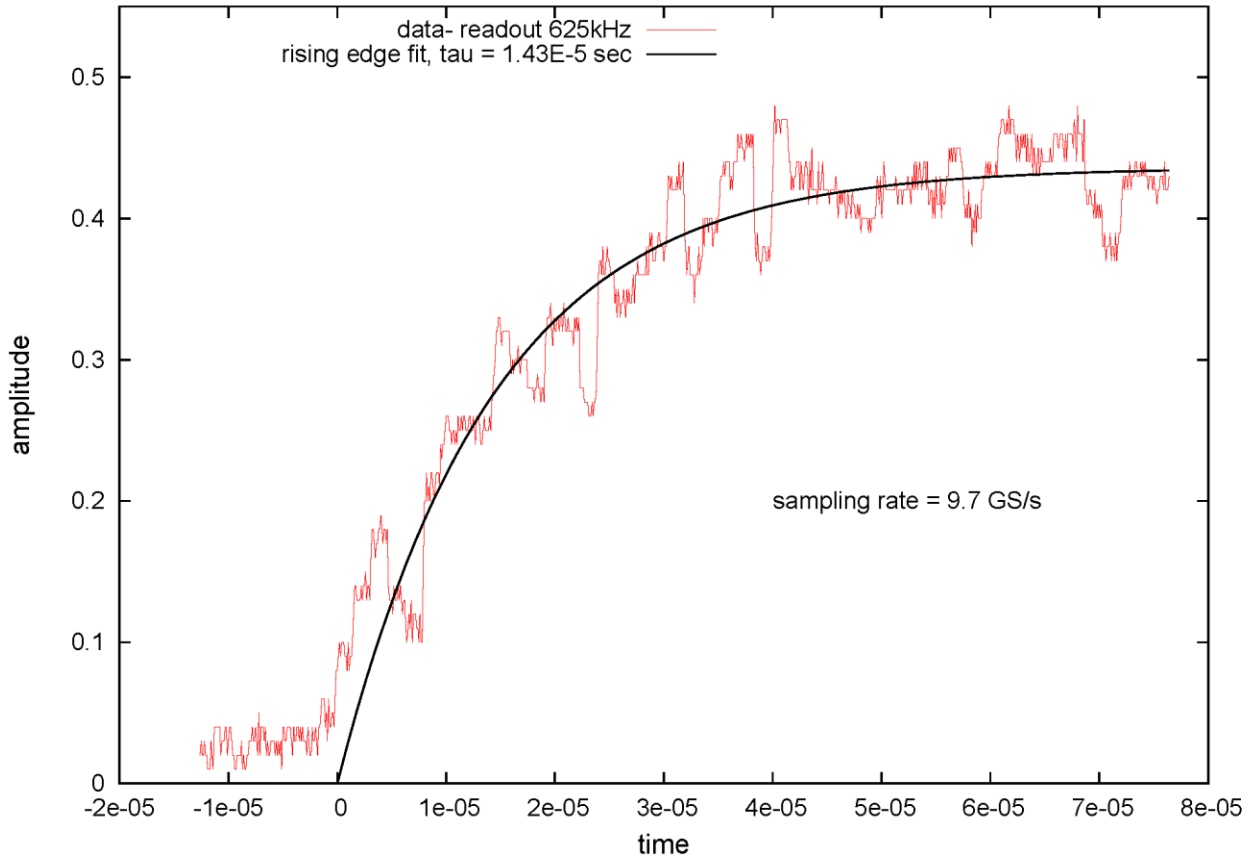
Anticipated 3 dB bandwidth due to the sampling network is:
$1/(2\pi \times 150\Omega \times 100fF)$= **10 GHz**

Add parasitics of the open switches
Post layout simulation provides **1.6 GHz**

Bonding wire + pads + test card:
L=25nH, C=3pF
$1/ [2\pi \times \sqrt{(25 \times 3e\text{-}12)}]$=**580 MHz**

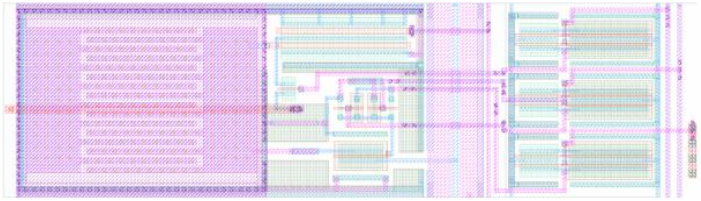
Flip-chip version card developed

Analog bandwidth

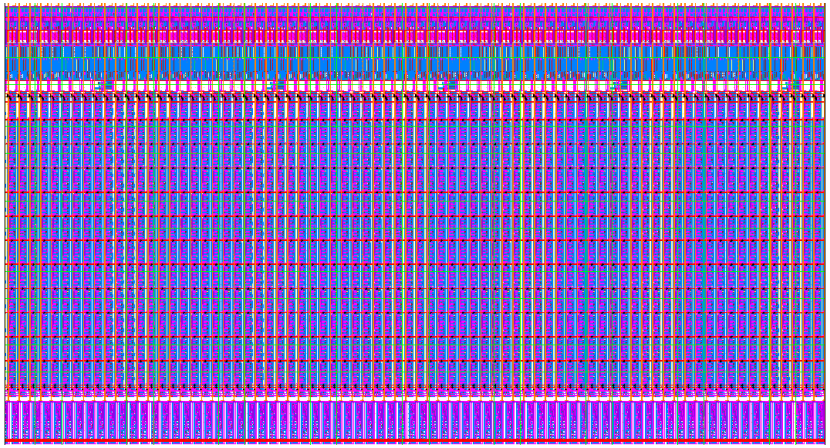


Sampling of an edge clock at 9.7GS/s. Analog bandwidth is 14.3 μs x 625kHz/9.7GHz = 180 MHz

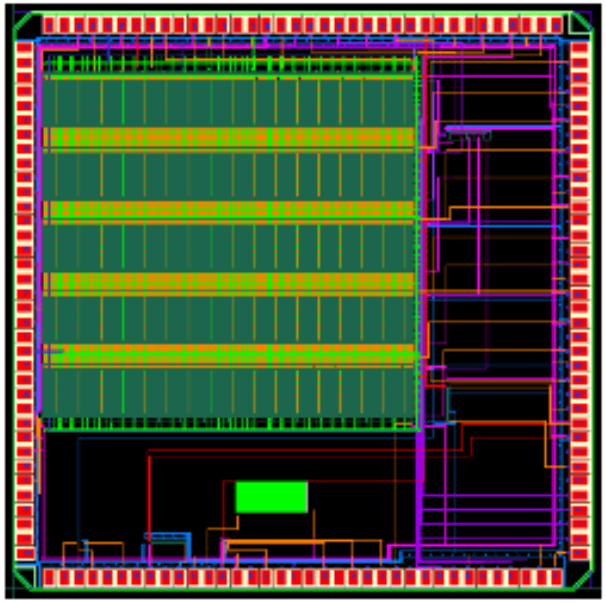
Layout (first version)



One sampling cell

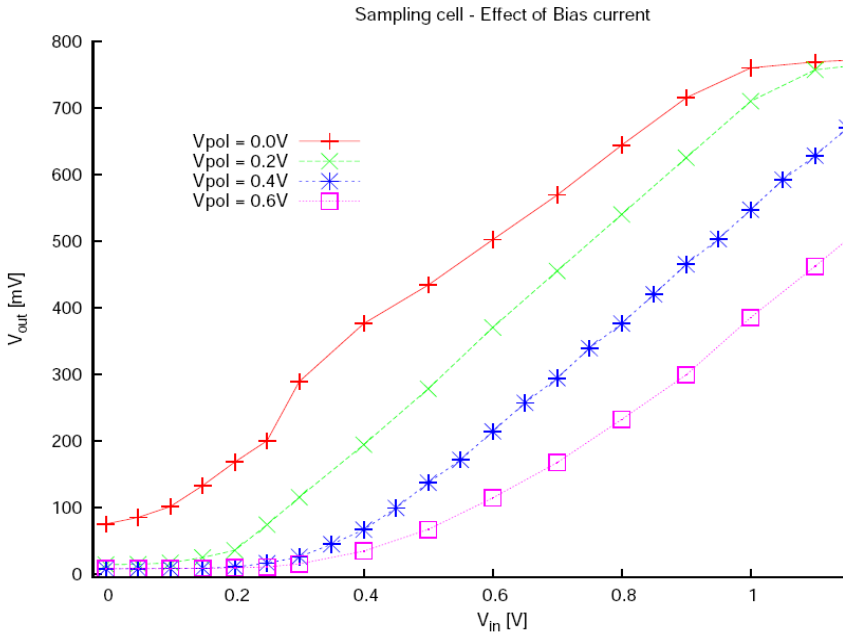


One channel

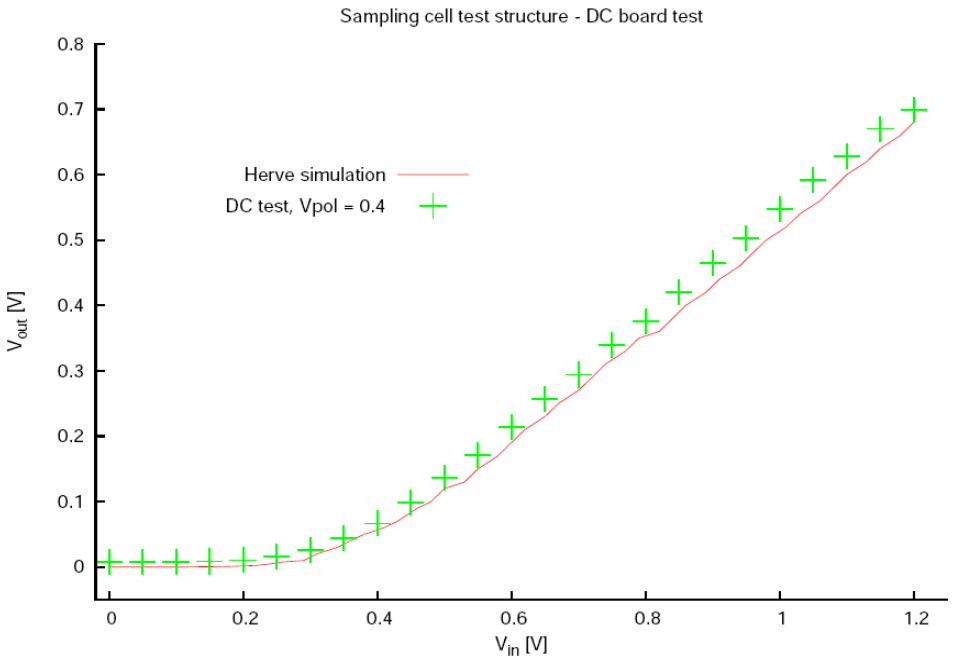


CMOS 130nm IBM 4 x 4 mm^2

Tests: Measured Sampling cell (DC)



Measurements



Simulation/Measurements

Optimum at 0.4V biasing

ADC

Wilkinson:

All cells digitized in one conversion cycle

- Ramp generator
- Comparators
- Counter
- Clocked by the ring oscillator at 1-2 GHz

- Not functional in this chip version, still under debugging
- Chip tested using a buffered analog output

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Conclusion Perspective

- **This 130nm CMOS ASIC:**

  - Sample rate 11.5 GS/s (15 anticipated)
  - Analog bandwidth is 200 MHz (1.6GHz simulated)

  Issues:

  - Analog bandwidth reduced by test card environment
  - ADC to be fixed

- **Next chips (expected December 2010) :**

- ½ Hawaii- ½ Chicago

Hawaii:	**Chicago:**
DAC	Delay line with DLL structure
D Flip Flop	Free running DLL with low Vt transistors
Charge Sensitive Amplifier	Phase detector–Charge pump
LVDS	Ring Oscillator
Ring Oscillator	Two test Transmission lines
Differential storage cell	

- Full 6-channel chip including

Four channels including input channel discriminators

One timing channel

One test channel

References

[1] J.L. Wiza. Micro-channel Plate Detectors. Nucl. Instr. Meth. 162 (1979) 587-601.
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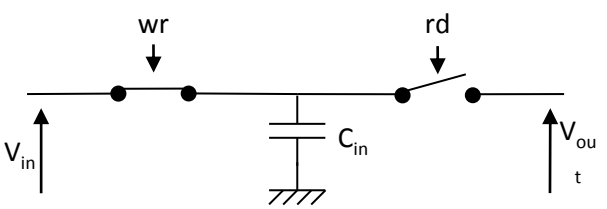
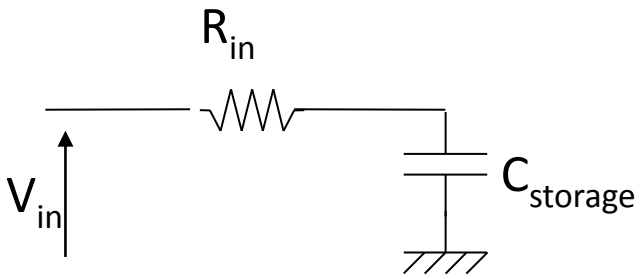
[4] H. Kim et al. Electronics Developments for Fast Timing PET Detectors. Symposium on Radiation and Measurements Applications. June 2-5 (2008), Berkeley CA, USA.
[5] An extensive list of references on timing measurements can be found in: A.Mantyniemi, MS Thesis, Univ. of Oulu, 2004; ISBN 951-42-7460-I; ISBN 951-42-7460-X;
[6] S. Cova et al. Constant Fraction Circuits for Picosecond Photon Timing with Micro-channel Plate Photomultipliers. Review of Scientific Instruments, 64-1 (1993) 118-124.
[7] E. Delagnes, Y. Degerli, P. Goret, P. Nayman, F. Toussenel, and P. Vincent. SAM : A new GHz sampling ASIC for the HESS-II Front-End. Cerenkov Workshop (2005), and NIM A, Volume 567, Issue 1, p. 21-26, 2006
[8] S. Ritt. Design and Performance of the 5 GHz Waveform Digitizer Chip DRS3. Nuclear Instruments and Methods, (2007).
[9] G. Varner, L.L. Ruckman, A. Wong. The First version Buffered Large Analog Bandwidth (BLAB1) ASIC for high Luminosity Colliders and Extensive Radio Neutrino Detectors. Nucl. Inst. Meth. A591 (2008) 534.
[10] G.Bondarenko, B. Dolgoshein et al. Limited Geiger Mode Silicon Photodiodes with very high Gain. Nuclear Physics B, 61B (1998) 347-352.
[11] J-F Genat , G. Varner, F. Tang and H. Frisch. Signal Processing for Pico-second Resolution Timing Measurements. Nuclear Instruments and Methods, (2009).
[12] J. Christiansen. An Integrated CMOS 0.15 ns Digital. Timing Generator for *TDC's* and Clock Distribution. Systems, IEEE Trans. Nucl. Sci., Vol. 42, No4 (1995), p. 753

Thanks for your attention !

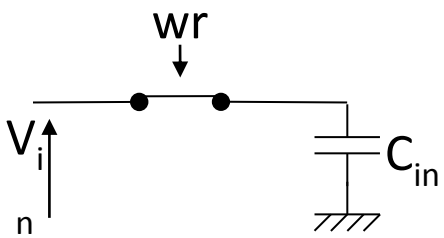
Backup

Sampling Cell





Principle



"Write" state 3 dB analog bandwidth is $1/(2\pi R_{in}C_{storage})$

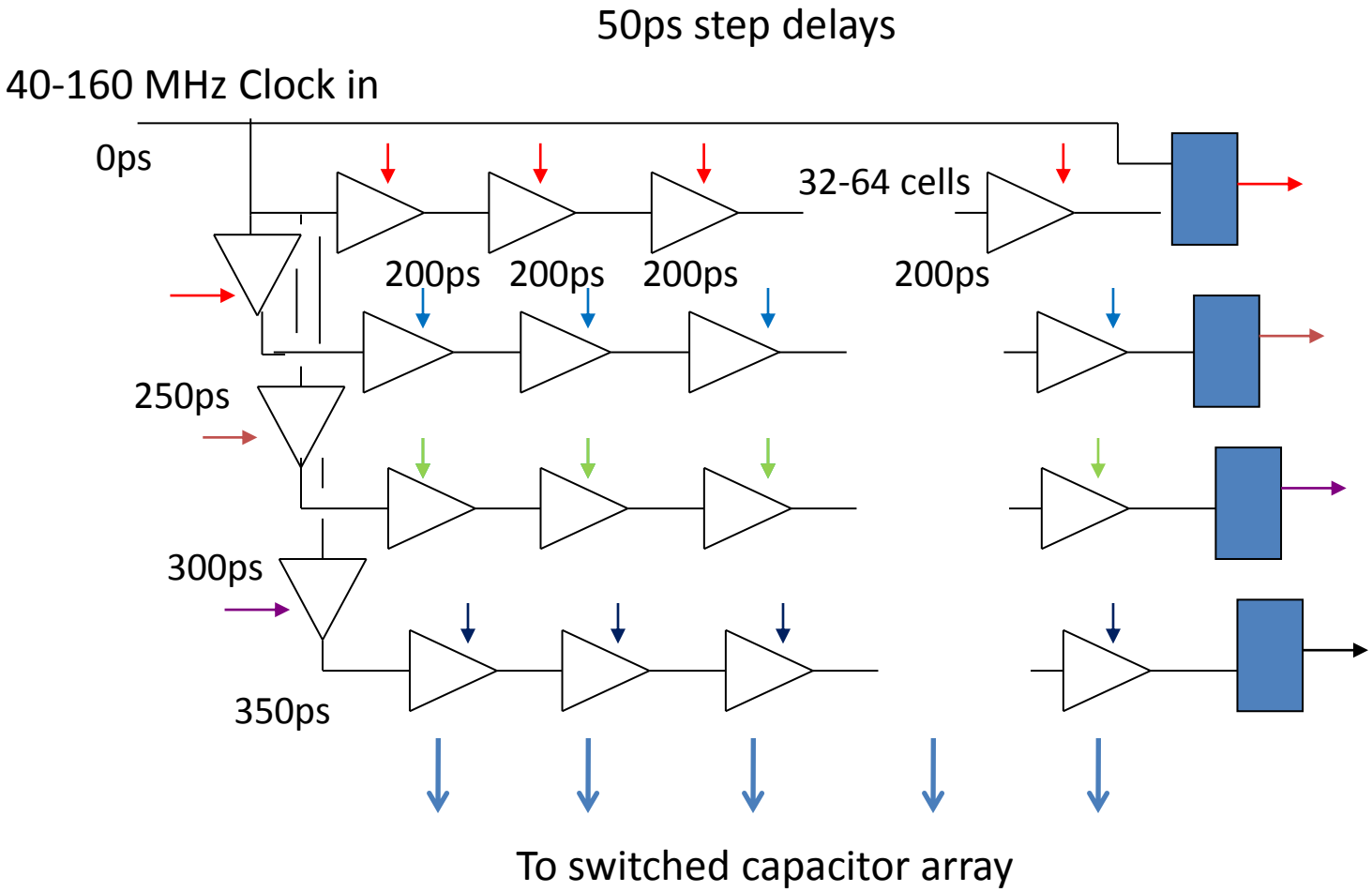
BUT parasitics (bonding wire + stray capacitors due to open switches) induce a much dominant pole !

- Flip-chip test card under development

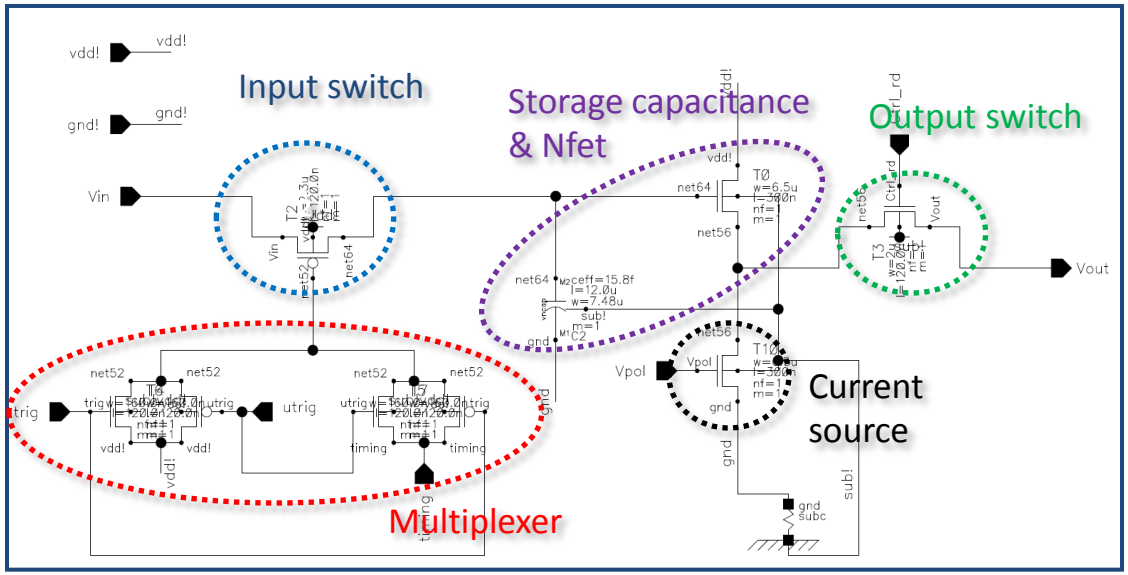
- "Sampling window" N switches closed x sampling period
  Analog bandwidth does not depend upon N

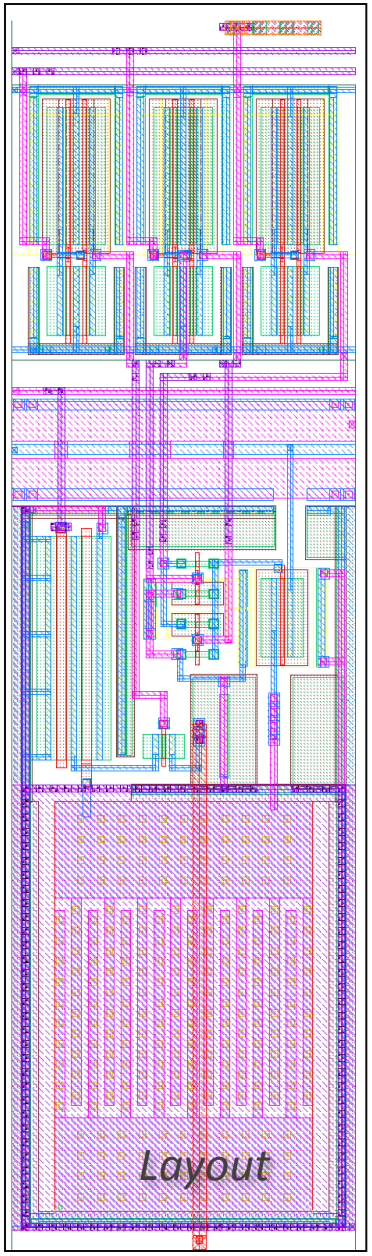
- Thermal kT/C switching noise = 250μV = one 12-bit ADC count
- Digital noise presumably higher. Fixed pattern noise due to Vt spreads of buffers

5-15 GHz Timing Generator [12]



Sampling Cell version 1 (Herve Grabas)



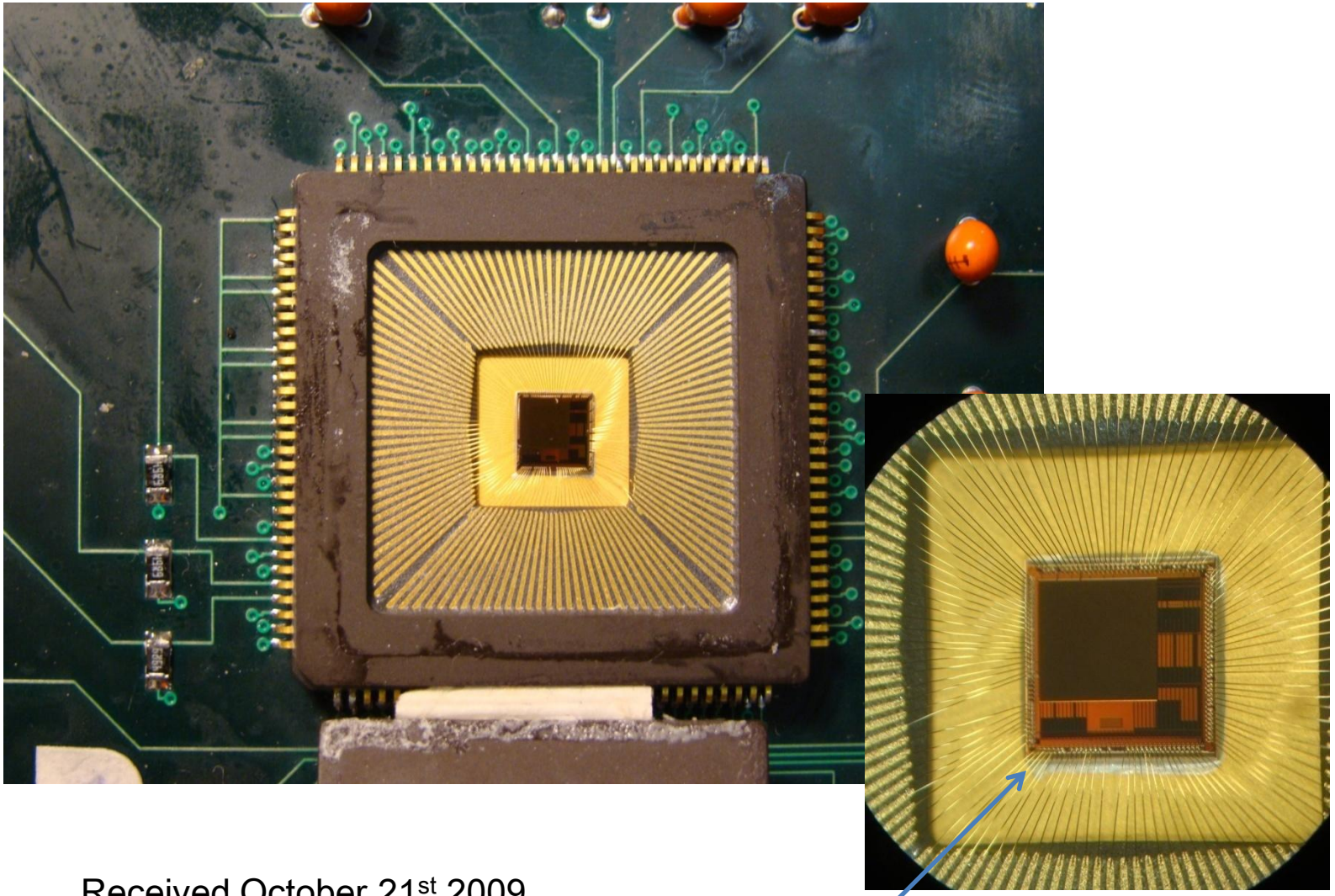


Sampling Capacitance 100 fF
Switch resistance: 100 Ω
Analog bandwidth 1-2GHz

Tests (first version)

- First tests of packaged chips (presented here)
  - DC power vs biases,
  - Sampling cell response vs input
  - ADC's comparator
  - Leakages (voltage droop)
  - Digital Readout
- Fine tests to come… (chip is just being bump-bonded to PCB)
  - Analog bandwidth
  - Resolution, signal-to-noise
  - Sampling cell response vs sampling window
  - Crosstalk
  - Max sampling rate
  - Full ADC
  - Linearities, dynamic range, readout speed

First version



Received October 21st 2009

Die to be bump-bonded on PCB

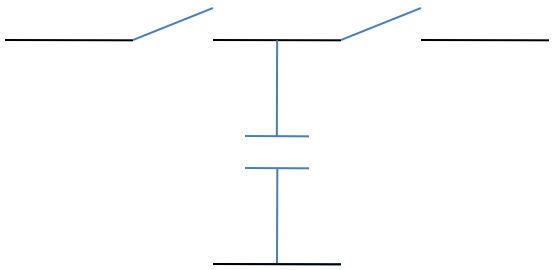
Tests: Sampling cell Leakages

1 - input LOW, write switch CLOSED

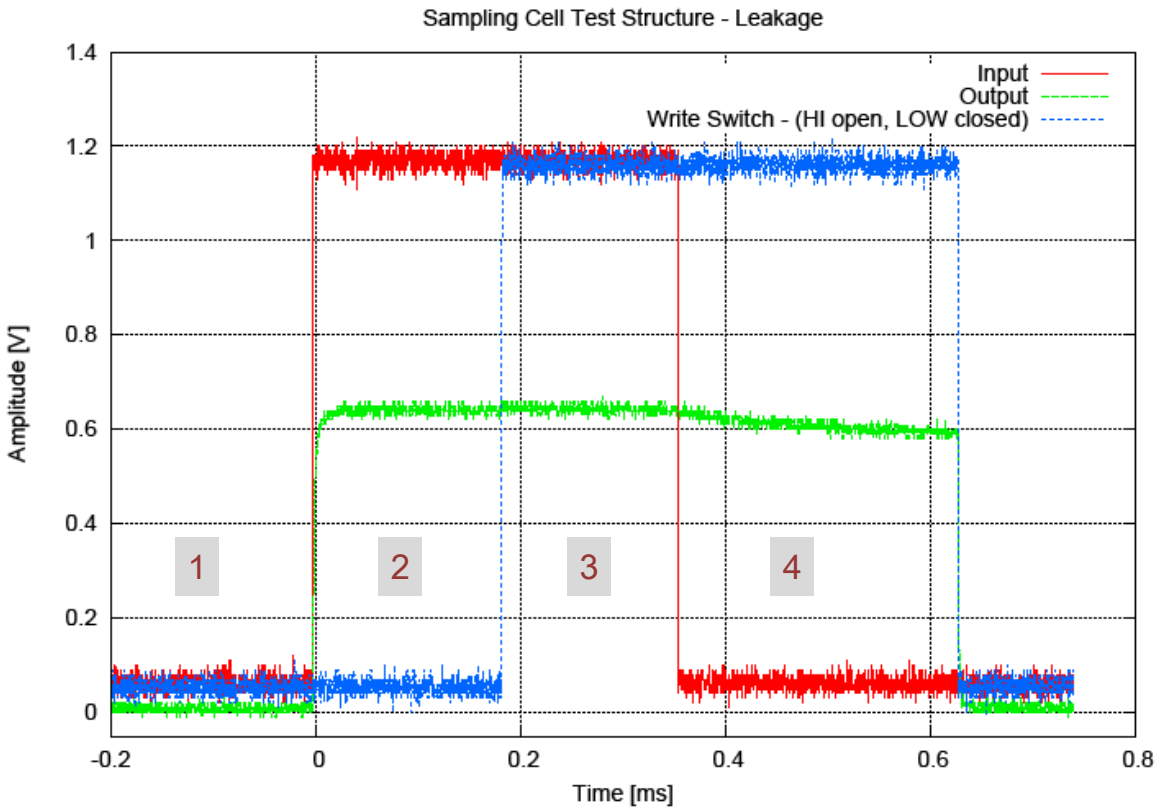
2 - input HI, switch CLOSED

3 - input HI, switch OPEN

4 - input LOW, switch OPEN



Write switch Read switch



Sampling Chips

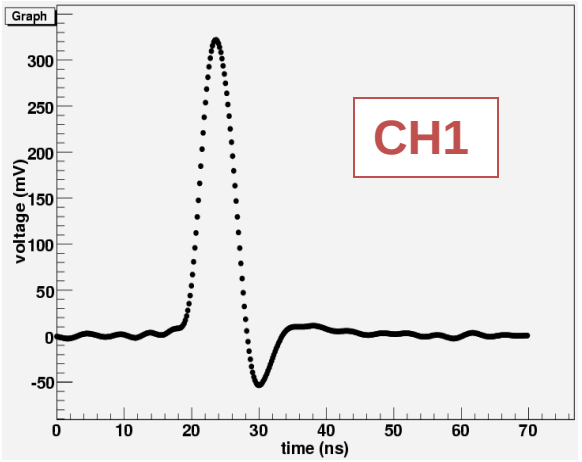
	Sampling GS/s	Bandwidth GHz	Dyn. range bits	Depth	PLL	ADC bits	Trigger	Techno
G. Varner (Hawaii) [9]	6	1.0	10	1024	no	12	experience	.25μm
S. Ritt (PSI) [8]	6	.8	11.5	256	3.9ps	no	no	.25μm
D. Breton/E. Delagnes (Orsay/Saclay) [7]	2.5	.5	13.4	250	20ps	no	no	.35μm

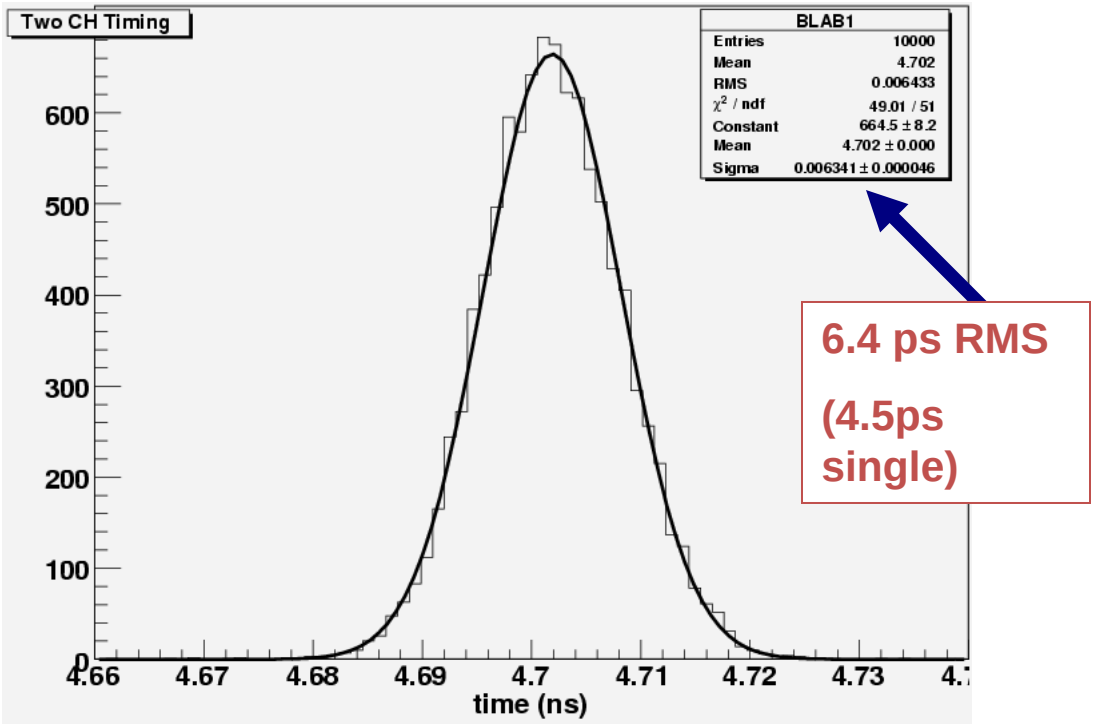
ASIC Deep Sub-Micron (< .13μm) CMOS processes allow today:

Sampling: 10-20 GHz
Bandwidth: > 1.5 GHz
Dyn. Range: 10 bit

Existing ASICs: Labrador 3 [9]

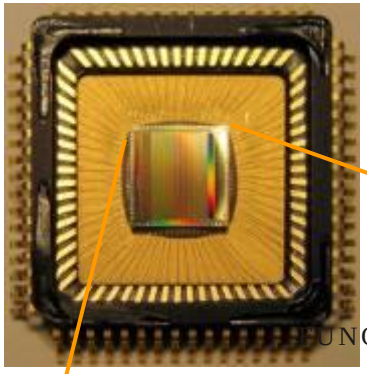
Gary Varner
U-Hawaii



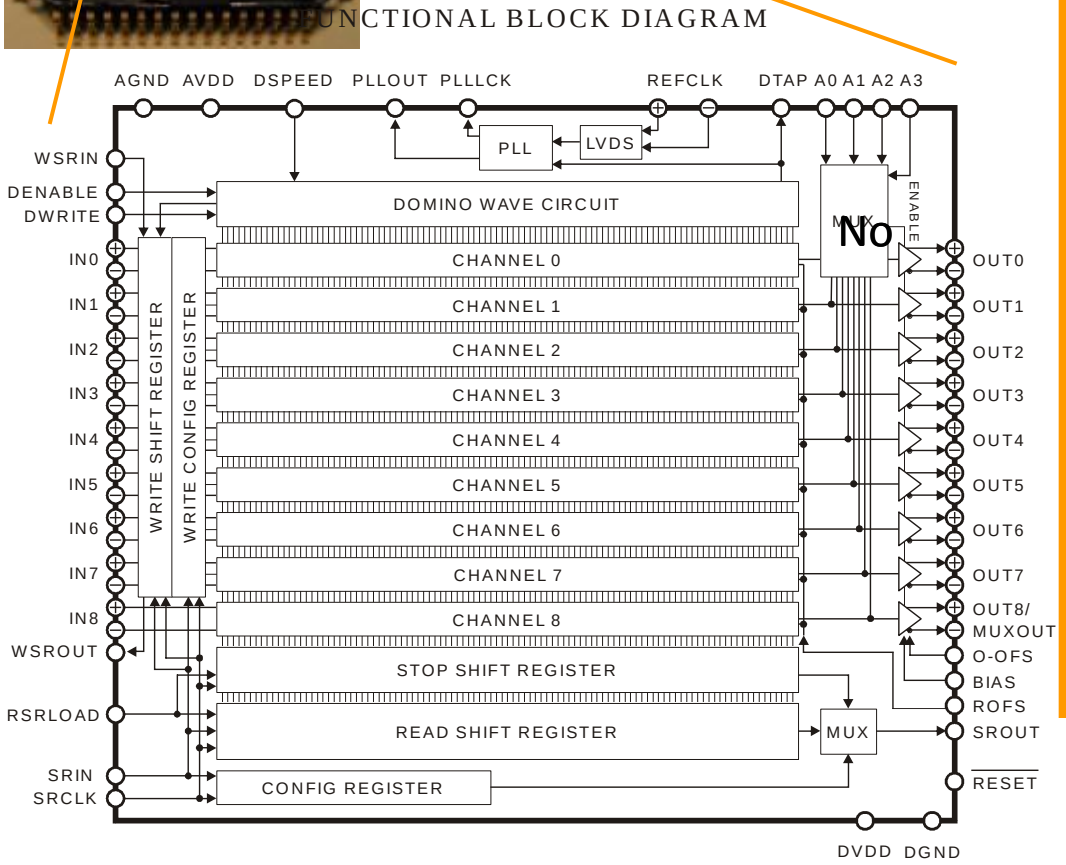


250nm CMOS

Waveform Digitizing Chip DRS4 [8]



Stefan Ritt
Paul Scherrer Institute
Switzerland

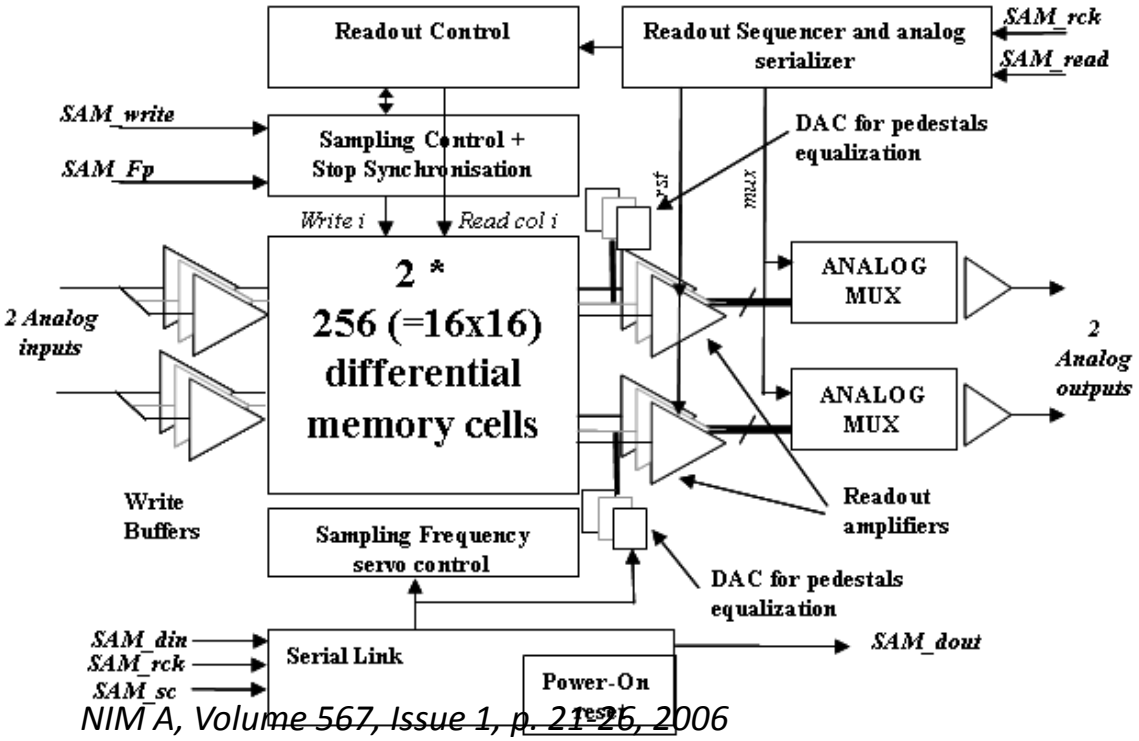


- UMC 0.25 μm rad. hard
- 9 chn. each 1024 bins, cascadable up to 8192
- Sampling speed 0.2 … 5 GS/s
- Bandwidth 950 MHz
- 17.5 mW/chn @ 2.5V
- On-chip PLL stabilization
- Readout speed using ext. ADC: 30 ns * $n_{samples}$
- SNR: 69 dB calibrated
- Aperture jitter: 4 ps at 5 GS/s calibrated

250nm CMOS

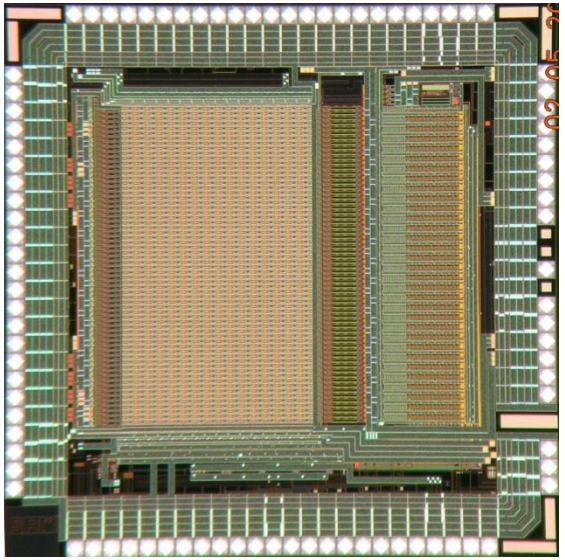
The SAM (Swift Analog Memory) ASIC [7]

D. Breton/E. Delagnes
Orsay/Saclay



NIM A, Volume 567, Issue 1, p. 21-26, 2006

- **2 differential channels**
- **256 cells/channel**
- **BW > 450 MHz**
- **Sampling Freq 400MHz->3.2GHz**
- **High Readout Speed > 16 MHz**
- **Smart Read pointer**
- **Few external signals**
- **Many modes configurable by a serial link.**
- **Auto-configuration @ power on**
- **AMS 0.35 µm => low cost for medium size prod**



6000 ASICs manufactured, tested and delivered in Q2 2007